MF423-07

EPSON

SED1200 Series

LCD Controller/Drivers

Technical Manual

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

NOTICE

Note the following precautions when using semiconductor devices.

[Precautions for light]

Due to the solar battery principle, the characteristics of the semiconductor devices generally change when the devices are irradiated. This IC, therefore, may malfunction when exposed to light.

Since this IC is not completely lightproof, follow the precautions below when using a substrate or product on which it is mounted.

(1) Design and mount the substrate or product so as to block out any light from reaching the IC during actual use.
(2) For the inspection process, design the environments so as to block out any light from reaching the IC.
(3) When blocking out light, take all surfaces of the IC chip into account.

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LCD Controller/Drivers

Selection Guide

■ LCD controller-drivers for small-sized displays

Built-in character generators together with segment and common drivers simplify the task of displaying microprocessor messages on small LCDs.

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (characters)	Micropro-cessor interface	Extension display output	Package	Comment
SED1200D0A	2.5–5.5	3.5–5.5	1/8,1/16	50	16	20	4-bit parallel	–	Al pad chip	JIS character
SED1200D0B										ASCII character
SED1200F0A									QFP1-80pin	JIS character
SED1200F0B										ASCII character
SED1200F1B									QFP14-80pin	
SED1210D0A				40		40	4 or 8-bit parallel	Serial	Al pad chip	JIS character
SED1210D0B										ASCII character
SED1210F0A									QFP5-80pin	JIS character
SED1210F0B										ASCII character
SED1220DXB	2.4–3.6	4.0–7.0	1/18,1/26	62	26	36	4 or 8-bit parallel or Serial	–	Au bump chip	LCD static drive allowed Three standard characters (JIS, ASCII, Cellular)
SED1220TXX									TCP	
SED1221DXB					18				Au bump chip	
SED1221TXX									TCP	
SED1220DXA									Al pad chip	
SED122ADXB									Au bump chip	
SED122ATXX									TCP	
SED1225DXB	1.7–3.6	3.0–6.0	1/18,1/26	64	26	36	4 or 8-bit parallel or Serial	–	Au bump chip	
SED1225TXB									TCP	
SED1278D	4.5–5.5	3.0–5.5	1/18,1/11, 1/16	40	16	80	4 or 8-bit parallel	Serial	Al pad chip	Six standard characters (0A/0B/0C/0E/0G/0H)
SED1278F									QFP5-80pin	
SED1280F							Serial		QFP5-100pin	Three standard character (0A/0B/0C)
SED1230D	2.4–3.6	4.0–12.0	1/30	65	30	48	4 or 8-bit parallel or Serial	–	Au bump chip	Built-in power circuit for LCD Three standard characters (JIS, ASCII, Cellular) SED1230/31/32/33 LCD static drive allowed SED1234/35 LCD dynamic drive only.
SED1230T									TCP	
SED1231D			1/23		23				Au bump chip	
SED1231T									TCP	
SED1232D			1/16		16				Au bump chip	
SED1232T									TCP	
SED1233D				80					Au bump chip	
SED1233T									TCP	
SED1234D			1/30	62	30				Al pad chip	
SED1235D			1/16		16				Al pad chip	
SED1240DXB	1.8–5.5	5.0–16.0	1/34	80	34	80			Au bump chip	
SED1240TXX									TCP	
SED1241DXB			1/26		26				Au bump chip	
SED1241TXX									TCP	
SED1242DXB			1/18		18				Au bump chip	
SED1242TXX									TCP	

SED1200 Series
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SED1200 Series

OVERVIEW

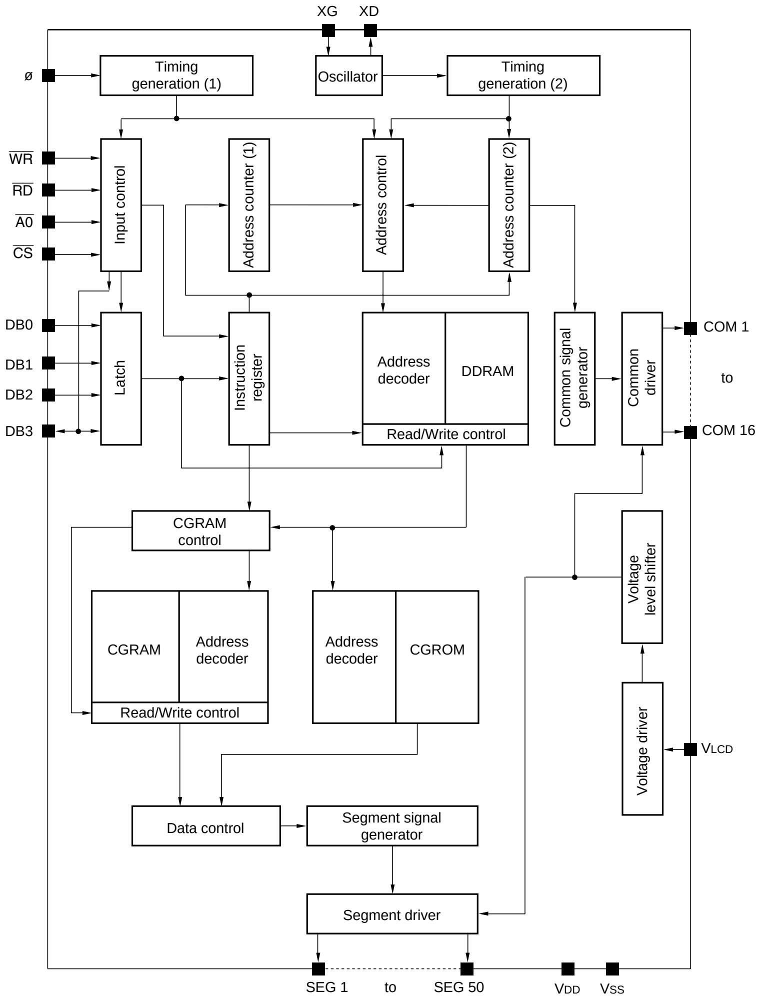
The SED1200 is a Liquid Crystal Display (LCD) character display controller-driver, capable of directly driving displays as large as 2 lines of 10 5×8 pixel characters, with a minimum of external components.

The SED1200 has an internal character generator (CG) consisting of 160 JIS ASCII characters in ROM and four user definable characters in RAM. The internal CG, a versatile set of cursor and display control commands, mean that the system CPU is only responsible for the display data and commands, and not for the LCD display itself.

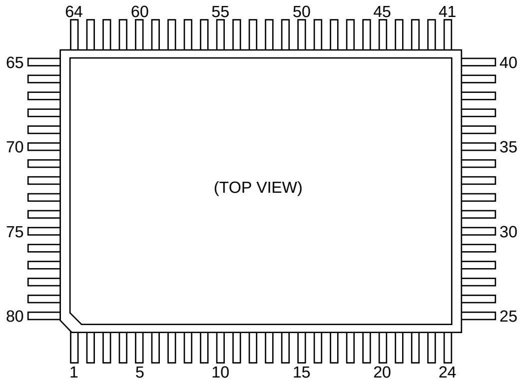
FEATURES

- Internal display RAM to hold 20 8-bit character codes.
- Internal character generator
  - CGROM: 160 JIS ASCII characters.
  - CGRAM: 4 user programmable 5×8 pixel characters
  - Font: 5×7 pixel characters plus the underline cursor.
  - JIS character set using SED1200F0A/SED1200D0A
  - ASCII character set using SED1200F0B/SED1200D0B
- Internal LCD driver circuitry
  - 50 segment driver lines
  - 16 common driver lines
  - Total size: Two lines of 10 characters each (maximum). One line of 20 characters (LCD panel dependent)
- CPU interface
  - 4-bit CPU data bus
  - 13 display control commands
- Low external component count
  - Built in RC oscillator (using one external feedback resistor)
  - Built in LCD driver voltage-divider network.
- Implemented using low power CMOS technology
  - TTL compatible CPU interface
- Power supply
  - Logic: 2.5 V to 5.5 V
  - LCD: 3.5 V to 5.5 V
- 80 pin QFP package SED1200F and chip (SED1200D)

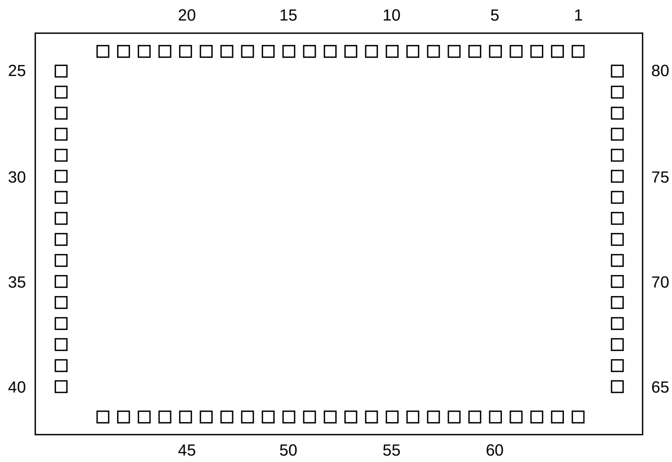
BLOCK DIAGRAM



PINOUT



SED1200F Package Outline



SED1200D Die Outline

TABLE 1. SED1200 Pinout

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	SEG17	21	COM4	41	COM10	61	SEG37
2	SEG16	22	COM5	42	COM11	62	SEG36
3	SEG15	23	COM6	43	COM12	63	SEG35
4	SEG14	24	COM7	44	COM13	64	SEG34
5	SEG13	25	COM8	45	COM14	65	SEG33
6	SEG12	26	A0	46	COM15	66	SEG32
7	SEG11	27	$\overline{CS}$	47	COM16	67	SEG31
8	SEG10	28	$\overline{RD}$	48	SEG50	68	SEG30
9	SEG9	29	$\overline{WR}$	49	SEG49	69	SEG29
10	SEG8	30	Φ	50	SEG48	70	SEG28
11	SEG7	31	X_D	51	SEG47	71	SEG27
12	SEG6	32	X_G	52	SEG46	72	SEG26
13	SEG5	33	DB3	53	SEG45	73	SEG25
14	SEG4	34	DB2	54	SEG44	74	SEG24
15	SEG3	35	DB1	55	SEG43	75	SEG23
16	SEG2	36	DB0	56	SEG42	76	SEG22
17	SEG1	37	V_{SS}	57	SEG41	77	SEG21
18	COM1	38	V_{LCD}	58	SEG40	78	SEG20
19	COM2	39	V_{DD}	59	SEG39	79	SEG19
20	COM3	40	COM9	60	SEG38	80	SEG18

PIN DESCRIPTION

CPU Interface

$\overline{CS}$ Active low chip select input.
$\overline{RD}$ Active low read enable input.
$\overline{WR}$ Active low write strobe.
A0 Selects between instruction and display data access.
A0 = H: Display data
A0 = L: Instruction
D0–D2 Active high CPU data inputs.
D3 Active high CPU data input/output.
Φ Clock input for command execution.

LCD Interface

COM1–COM16 LCD common driver outputs.
SEG1–SEG50 LCD segment driver outputs.

Oscillator

OSC1, OSC2 Terminals for the oscillator external feedback resistor, R_f. If an externally generated clock is used, it is connected to OSC1; OSC2 is left open.

Power Supply

V_{DD} Logic power supply
V_{LCD} LCD power supply
V_{SS} System ground (0 V).

COMMAND DESCRIPTION

Command Summary

TABLE 2. SED1200 Command Summary

COMMAND NAME	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A0	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
SET CURSOR DIRECTION	0	0	1	0	0	0	0	0	0	1	0	D/I	D0 = 1 ... Decrement D0 = 0 ... Increment
CURSOR ADDRESS –1/+1	0	0	1	0	0	0	0	0	0	1	1	–1/+1	D0 = 1 ... Cursor address –1 D0 = 0 ... Cursor address +1
CURSOR FONT SELECT	0	0	1	0	0	0	0	0	1	0	0	A/U	D0 = 1 ... All dots blinking D0 = 0 ... Underline
CURSOR BLINK ON/OFF	0	0	1	0	0	0	0	0	1	0	1	ON/OFF	D0 = 1 ... ON D0 = 0 ... OFF
DISPLAY ON/OFF	0	0	1	0	0	0	0	0	1	1	0	ON/OFF	D0 = 1 ... ON D0 = 0 ... OFF
CURSOR ON/OFF	0	0	1	0	0	0	0	0	1	1	1	ON/OFF	D0 = 1 ... ON D0 = 0 ... OFF
SYSTEM RESET	0	0	1	0	0	0	0	1	0	0	0	0	Data RAM & CGRAM are not affected
LINE SELECT	0	0	1	0	0	0	0	1	0	0	1	2/1	D0 =1 ... 2 line display (1/16 duty) D0 = 0 ... 1 line display (1/8 duty)
SET CGRAM ADDRESS	0	0	1	0	0	0	1	0	(LOWER ADDRESS)				Upper address fixed at 0H
SET CGRAM DATA	0	0	1	0	0	1	0	(CGRAM DATA)					
SET CURSOR ADDRESS	0	0	1	0	1	2nd/1st (N DIGIT-1)							D6 = 1 ... 2nd line N digit address D6 = 0 ... 1st line N digit address
SET CHARACTER CODE	0	0	1	1	(CHARACTER CODE)								
BUSY FLAG CHECK	0	1	0	0	BF	*	*	*	BF	*	*	*	High impedance

Write Commands

SET CURSOR DIRECTION

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	D

Sets the way in which the cursor address register changes as character data is written to the SED1200 by the CPU, and hence the direction of cursor movement.

D = 0: Address register increment direction
D = 1: Address register decrement direction

CURSOR ADDRESS –1/+1

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	D

Adds one to, or subtracts one from, the current contents of the cursor address register, and hence moves the cursor.

D = 0: ADDRESS = ADDRESS + 1
D = 1: ADDRESS = ADDRESS – 1

CURSOR FONT SELECT

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	D

D = 0: Underline cursor
D = 1: All dots blinking

CURSOR BLINK ON/OFF

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	D

Controls flashing of the underline cursor.
D = 0: Flashing stopped
D = 1: Cursor flashing

DISPLAY ON/OFF

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	D

D = 0: Display Blanked
D = 1: Display on
Note: This command does not affect the contents of the display data RAM.

CURSOR ON/OFF

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	D

Controls the display of the cursor.
D = 0: Cursor off.
D = 1: Cursor on.

SYSTEM RESET

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0

Initializes the SED1200 to the following defaults.
1. CURSOR DIRECTION: Increment
2. CURSOR FONT: Underline
3. CURSOR BLINK: Off
4. DISPLAY: Off
5. CURSOR: Off
6. LINE SELECT: One line display
7. CURSOR ADDRESS: Address 0 (Line 1, character 0)

Note: SYSTEM RESET does not affect the contents of the display data RAM, or the CGRAM.

LINE SELECT

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	D

Selects the number of displayed lines, and hence the LCD drive duty cycle.
D = 0: 1 line display (1/8 duty cycle)
D = 1: 2 line display (1/16 duty cycle)
Note: The number of lines which can be displayed depends on the LCD panel used.

SET CURSOR ADDRESS

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	L	P_5	P_4	P_3	P_2	P_1	P_0

Presets the contents of the cursor address register, and hence the position of the cursor.
L = 0: Line 1 select
L = 1: Line 2 select
P_5–P_0: Position of character in selected line.

SET CHARACTER CODE

A0 = 1

D7	D6	D5	D4	D3	D2	D1	D0
C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

Writes the character code given by C_7–C_0 into the character data RAM at the location pointed to by the contents of the cursor address register. The contents of the cursor address register are then modified as specified by the last SET CURSOR DIRECTION instruction.

SET CGRAM ADDRESS

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	*	*	A_1	A_0

Presets the contents of the CGRAM address register to the position of one of the four user definable characters. The address is specified by A_1 and A_0.

SET CGRAM DATA

Loads the bit pattern D_4–D_0 into the CGRAM location specified by the current contents of the CGRAM address register. The contents of the CGRAM Address Register are incremented following each write of a SET CGRAM DATA instruction by the CPU.

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	D_4	D_3	D_2	D_1	D_0

See section 4.3, Loading CGRAM.

Read Commands

BUSY FLAG CHECK

Reading yields the status of the SED1200F.

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
BF	*	*	*	BF	*	*	*

BF = 0: SED1200 READY
BF = 1: SED1200 BUSY
Bits D2–D0 are tristate during reads of the Busy Flag.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{DD}	–0.3 to +7.0	V
Supply voltage (2)	V_{LCD}	V_{DD}–7.0 to V_{DD}+0.3	V
Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	–0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	–10 to +70	°C
Storage temperature	T_{stg}	–40 to +125	°C
Soldering temperature and time	T_{sol}	260, 10	°C, s

Electrical Specifications

DC Characteristics

V_{DD} = 5 V

V_{SS} = 0 V, T_a = –10 to +70°C

Parameter	Symbol	Condition		Rating			Unit	Pin
				min	typ	max		
Logic supply voltage	V_{DD}			4.5	5.0	5.5	V	V_{DD}
Liquid crystal display supply voltage	V_{LCD}			V_{DD}–5.5	—	V_{DD}–3.5	V	V_{LCD}
Oscillator feedback resistor	R_f	V_{DD} = 5.0 V, f_{OSC} = 100 kHz		240	310	380	kΩ	X_G, X_D
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 4.5 to 5.5 V		—	100	300	kHz	X_G, X_D
Operating frequency (2)	Φ	V_{DD} = 4.5 to 5.5 V		—	—	3.2	MHz	Φ
External clock duty		V_{DD} = 4.5 to 5.5 V		45	50	55	%	X_G, Φ
External clock rise time	t_r	V_{DD} = 4.5 to 5.5 V		—	—	50	ns	X_G, Φ
External clock fall time	t_f	V_{DD} = 4.5 to 5.5 V		—	—	50	ns	X_G, Φ
H-level input voltage (1)	V_{IH1}	V_{DD} = 4.5 to 5.5 V		2.0	—	V_{DD}	V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB3, Φ
L-level input voltage (1)	V_{IL1}	V_{DD} = 4.5 to 5.5 V		0	—	0.8	V	
H-level input voltage (2)	V_{IH2}	V_{DD} = 4.5 to 5.5 V		0.8 V_{DD}	V_{DD}	V_{DD}	V	X_G
L-level input voltage (2)	V_{IL2}	V_{DD} = 4.5 to 5.5 V		0	0	0.2 V_{DD}	V	
H-level input leakage current	I_{LIH}	V_{DD} = 5.5 V, V_{IH} = 5.5 V		—	—	|–1.0|	µA	Φ, X_G, DB0 to DB3
L-level input leakage current	I_{LIL}	V_{DD} = 5.5 V, V_{IL} = 0 V		—	—	1.0	µA	
Input pull-up current	I_{IPU}	V_{DD} = 5.0 V, V_{IL} = 0 V		3.0	10	30	µA	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0
H-level output current	I_{OH}	V_{DD} = 4.5 to 5.5 V, V_{OH} = 2.4 V		|–1.0|	—	—	mA	DB3
L-level output current	I_{OL}	V_{DD} = 5.5 V, V_{OL} = 0.4 V		1.6	—	—	mA	
Common driver output current (1)	I_{OH}	V_{DD} level	V_{DD}=4.5 V V_{LCD}=1.0 V Voltage-divider resistor in low impedance state. 1/16 duty 0.5 V voltage drop Measured on one pin with other pins open circuit.	|–20|	—	—	µA	COM1 to COM16
Common driver output current (2)	I_{OL}	V_{LCD} level		20	—	—	µA	COM1 to COM16
Common driver output current (3)	I_{OL}	V_{L1} level		|±8|	—	—	µA	COM1 to COM16
Common driver output current (4)	I_{OL}	V_{L4} level		|±8|	—	—	µA	COM1 to COM16
Segment driver output current (1)	I_{OH}	V_{DD} level		|–12|	—	—	µA	SEG1 to SEG50
Segment driver output current (2)	I_{OL}	V_{LCD} level		12	—	—	µA	SEG1 to SEG50
Segment driver output current (3)	I_{OL}	V_{L2} level		|±4|	—	—	µA	SEG1 to SEG50
Segment driver output current (4)	I_{OL}	V_{L3} level		|±4|	—	—	µA	SEG1 to SEG50
Voltage-divider resistor (1)	R_{d1}	Normal conditions		30	130	300	kΩ	
Voltage-divider resistor (2)	R_{d2}	Low impedance state		3.0	13	30	kΩ	
Voltage-divider resistor low impedance duty	t_{Rd1}/t_{Rd2}	1/8 Duty		—	11/400	—	—	
		1/16 Duty		—	11/200	—	—	
Command execution time	t_{comd}	From $\overline{WR}$ rising edge to the end of internal processing		—	—	16/Φ (MHz)	µs	
Average operating current	I_{DD}	V_{DD} = 5.0 V, V_{LCD} = 0 V, f_{OSC} = 100 kHz, Φ = 1 MHz, $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = 5.0 V, output open		—	80	150	µA	V_{DD}

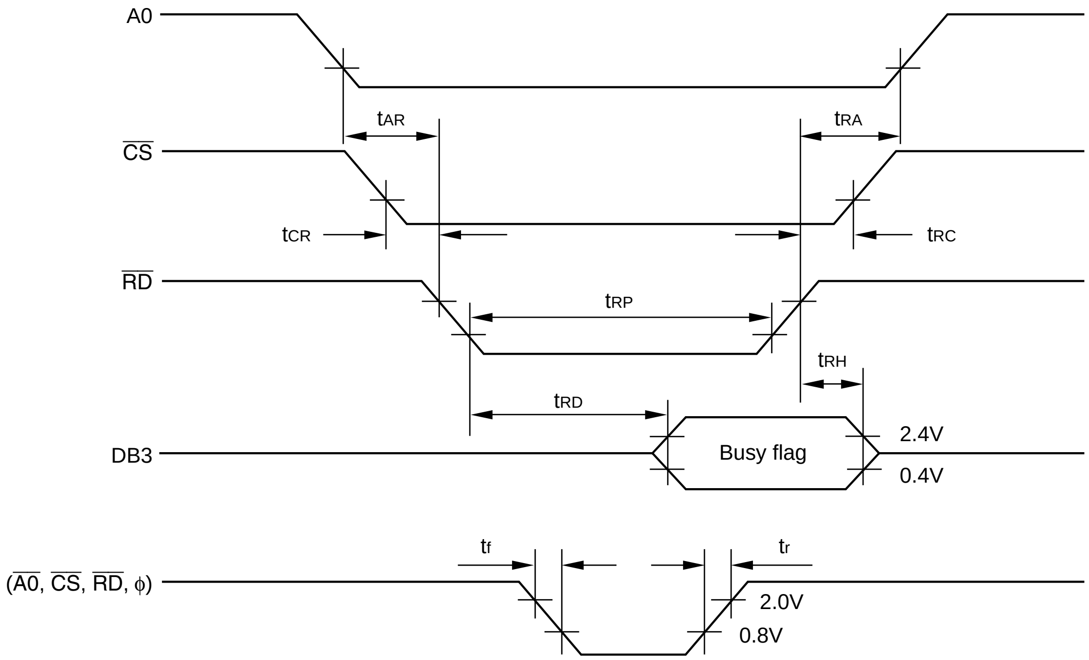
V_{DD} = 3 V

V_{SS} = 0 V, Ta = –10 to 70°C

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit	Pin
Logic supply voltage	V_{DD}		2.5	3.5	4.5	V	V_{DD}
Liquid crystal display supply voltage	V_{LCD}		V_{DD}–5.5	—	V_{DD}–3.5	V	V_{LCD}
Oscillator feedback resistor	R_f	V_{DD} = 3.0 V, f_{OSC} = 100 kHz	210	290	370	kΩ	X_G, X_D
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 2.5 V	—	—	300	kHz	X_G, X_D
Operating frequency (2)	Φ	V_{DD} = 2.5 V	—	—	1.0	MHz	Φ
External clock duty		V_{DD} = 2.5v	—	50	—	%	OSC1, Φ
External clock rise time	t_r	V_{DD} = 2.5 V	—	—	50	ns	OSC1, Φ
External clock fall time	t_f	V_{DD} = 2.5 V	—	—	50	ns	OSC1, Φ
H-level input voltage (1)	V_{IH1}	V_{DD} = 2.5 V	0.8 V_{DD}	—	V_{DD}	V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB3, Φ
L-level input voltage (1)	V_{IL1}	V_{DD} = 2.5 V	0	—	0.2 V_{DD}	V	
H-level input voltage (2)	V_{IH2}	V_{DD} = 2.5V	0.8 V_{DD}	—	—	V	X_G
L-level input voltabe (2)	V_{IL2}	V_{DD} = 2.5 V	—	—	0.2 V_{DD}	V	
H-level input leakage current	I_{LIH}	V_{DD} = 4.5 V	—	—	|–1.0|	µA	Φ, X_G, DB0 to DB3
L-level input leakage current	I_{LIL}	V_{DD} = 4.5 V	—	—	1.0	µA	
Input pull-up current	I_{IPU}	V_{DD} = 3.5 V	1.0	4.0	15	µA	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0
H-level output current	I_{OH}	V_{DD} = 2.5 V, V_{OH} = 2.0 V	200	—	—	µA	DB3
L-level output current	I_{OL}	V_{DD} = 2.5 V, V_{OL} = 0.5 V	200	—	—	µA	
Common driver output current (1)	I_{OH}	V_{DD} level (all driver rows: V_{DD}–V_{LCD} = 3.5 V Voltage-divider resistor in low impedance state. 1/16 duty 0.5 V voltage drop Measured on one pin with other pins open circuit.)	|-20|	—	—	µA	COM1 to COM16
Common driver output current (2)	I_{OL}	V_{LCD} level	20	—	—	µA	
Common driver output current (3)	I_{OL}	V_{L1} level	|±8|	—	—	µA	
Common driver output current (4)	I_{OL}	V_{L4} level	|±8|	—	—	µA	
Segment drivrer output current (1)	I_{OH}	V_{DD} level	|–12|	—	—	µA	SEG1 to SEG50
Segment drivrer output current (2)	I_{OL}	V_{LCD} level	12	—	—	µA	
Segment drivrer output current (3)	I_{OL}	V_{L2} level	|±4|	—	—	µA	
Segment drivrer output current (4)	I_{OL}	V_{L3} level	|±4|	—	—	µA	
Voltage-divider resistor (1)	R_{d1}	Normal conditions	—	130	—	kΩ	
Voltage-divider resistor (2)	R_{d2}	Low impedance state	—	13	—	kΩ	
Voltage-divider resistor low impedance duty	t_{Rd1}/t_{Rd2}	1/8 Duty	—	11/400	—	—	
		1/16 Duty	—	11/200	—	—	
Command execution time	t_{comd}	From $\overline{WR}$ rise time to the end of internal processing	—	—	16/Φ (MHz)	µs	
Average operating current	I_{DD}	V_{DD}–V_{SS} = 3.5 V V_{DD}–V_{LCD} = 1.5 V f_{OSC} = 100 kHz, Φ = 500 kHz $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = V_{DD}, output open	—	60	—	µA	V_{DD}

AC Characteristics

MPU Read Timing



V_{DD} = 4.5 to 5.5 V, Ta = –10 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
Setup time for A0 → $\overline{RD}$	t_{AR}	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	0	—	—	ns
$\overline{RD}$ delay output time	t_{RD}	—	—	250	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	20	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	20	—	—	ns
Data hold time	t_{RH}	10	—	—	ns
Read pulsewidth	t_{RP}	350	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

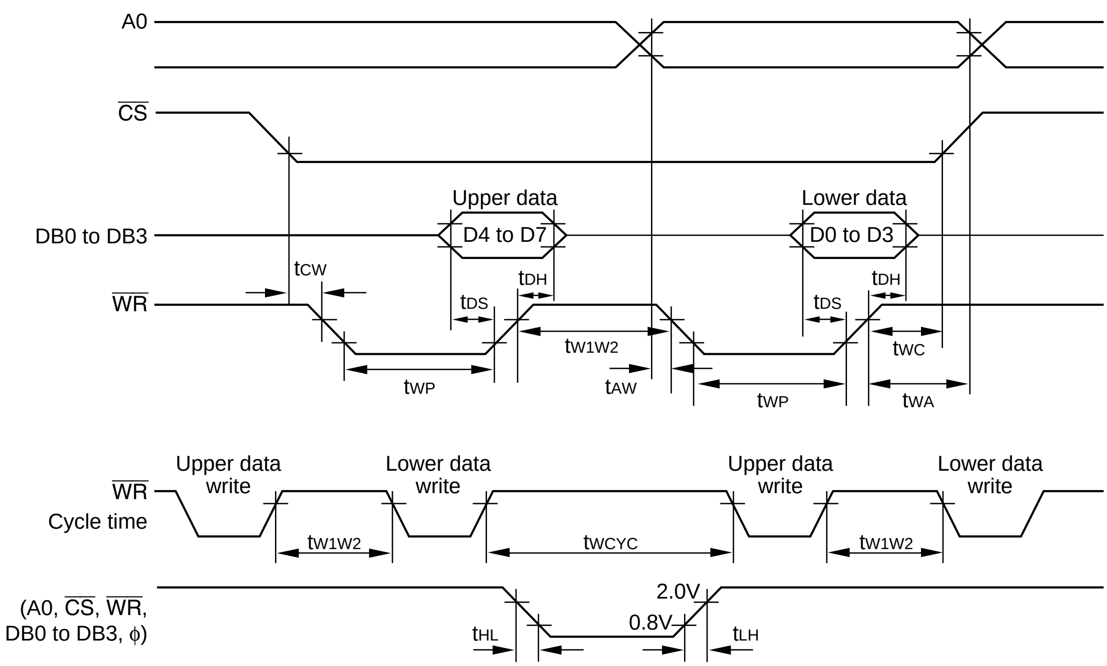
Note: Load on pin DB3 is C_L = 100 pF.

VDD = 2.5 to 4.5 V, Ta = –10 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
Setup time for A0 → $\overline{RD}$	t_{AR}	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	0	—	—	ns
$\overline{RD}$ delay output time	t_{RD}	—	—	350	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	0	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	0	—	—	ns
Data hold time	t_{RH}	10	—	—	ns
Read pulsewidth	t_{RP}	400	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

Note: Load on pin DB3 is CL = 100 pF.

MPU Write Timing



V_{DD} = 5 V, Ta = –10 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
A0 → $\overline{WR}$ setup time	t_{AW}	0	—	—	ns
$\overline{CS}$ → $\overline{WR}$ setup time	t_{CW}	0	—	—	ns
Data setup time	t_{DS}	120	—	—	ns
$\overline{WR}$ → A0 hold time	t_{WA}	20	—	—	ns
$\overline{WR}$ → $\overline{CS}$ hold time	t_{WC}	20	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
Write pulsewidth	t_{WP}	200	—	—	ns
Upper write pulse rising edge to lower write pulse falling edge time.	t_{W1W2}	200	—	—	ns
Lower write pulse rising edge to upper write pulse falling edge time.	t_{WCYC}	16/Φ (MHz)	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

V_{DD} = 3 V, Ta = –10 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
A0 → $\overline{WR}$ setup time	t_{AW}	0	—	—	ns
$\overline{CS}$ → $\overline{WR}$ setup time	t_{CW}	0	—	—	ns
Data setup time	t_{DS}	120	—	—	ns
$\overline{WR}$ → A0 hold time	t_{WA}	0	—	—	ns
$\overline{WR}$ → $\overline{CS}$ hold time	t_{WC}	0	—	—	ns
Data hold time	t_{DH}	100	—	—	ns
Write pulsewidth	t_{WP}	200	—	—	ns
Upper write pulse rising edge to lower write pulse falling edge time.	t_{W1W2}	200	—	—	ns
Lower write pulse rising edge to upper write pulse falling edge time.	t_{WCYC}	16/Φ (MHz)	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

OPERATION

Data Input/Output

Because the command codes are 8-bits wide and the SED1200's data bus is only 4-bits wide, the command codes must be split into two nibbles (4-bits), which are written separately.

Nibble	High-order				Low-order			
Data Bus Bit	D3	D2	D1	D0	D3	D2	D1	D0
Command Bit	D7	D6	D5	D4	D3	D2	D1	D0

The high-order nibble is written first, and is latched internally by the SED1200. When the low-order nibble is written, the eight bits of data are shifted into either the character registers or the command register, depending on the level of A0 during the low-nibble write cycle.

When the busy flag is read, only one read cycle is required.

New commands must not be written to the SED1200 if the device is executing one currently, so the busy flag should be checked before commands are written. It is not necessary to check the busy flag between writes of the upper and lower nibbles of commands. If the busy flag is not going to be checked between writes of individual commands then the MPU must wait long enough to allow for command execution to complete. The maximum time taken by the SED1200 to execute a command is 16/ Φ, where Φ is the system clock frequency.

System Initialization

Figure 1 is a flow chart of a possible SED1200 initialization sequence. Note that busy flag checks, and busy/wait loops have been omitted for the sake of brevity.

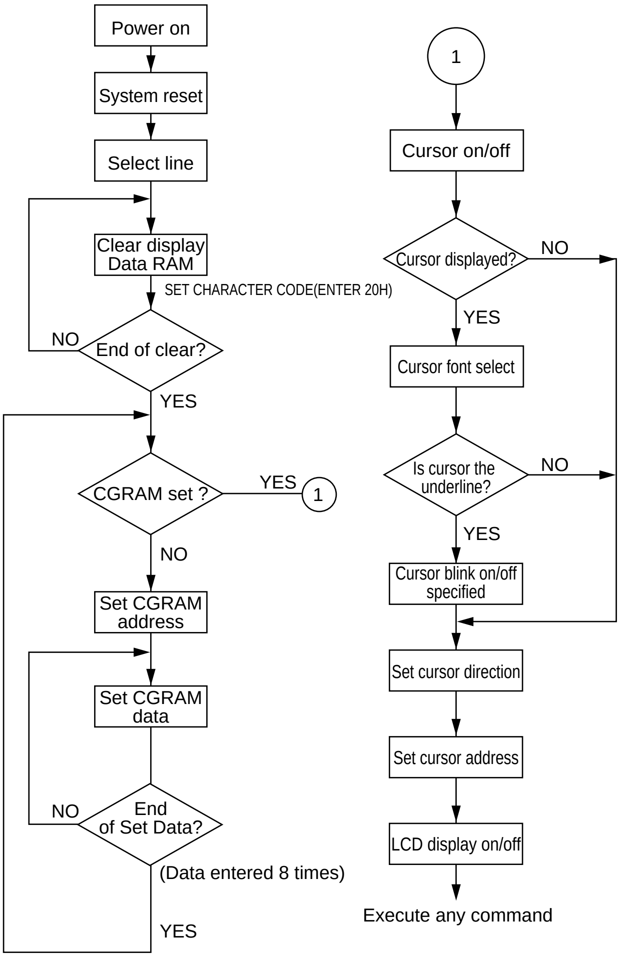


Figure 1. Initialization Flow Chart

Loading CGRAM

The character generator RAM is loaded with a character bit pattern using a combination of one SET CGRAM ADDRESS command and eight SET CGRAM DATA commands. For example, to load the character shown in figure 2 into the area of CGRAM corresponding to character code 01H, the sequence shown in table 3 is used.

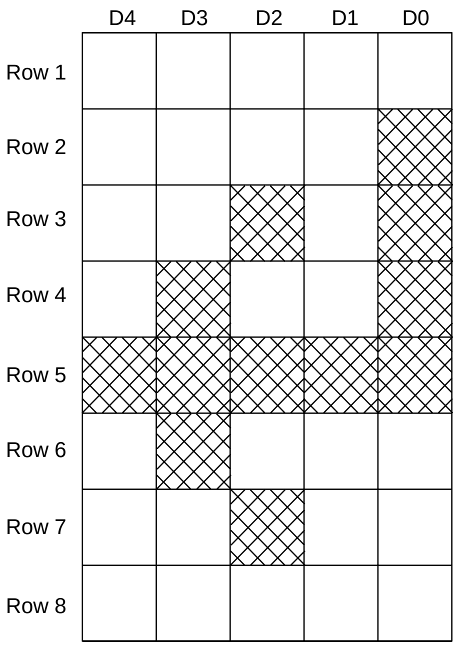


Figure 2. User Defined Character

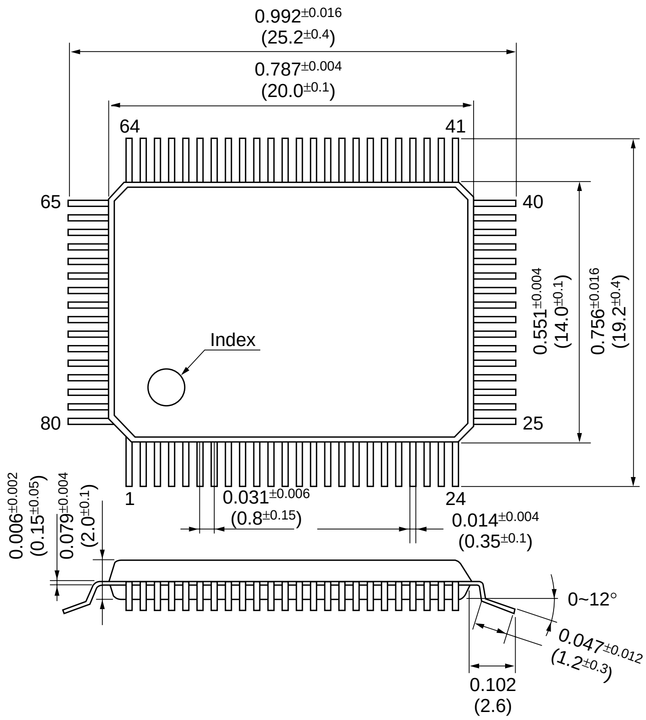
TABLE 3. Loading User Defined Character

Step	A0	$\overline{WR}$	Data	Action
1	0	0	21H	Set address of CGRAM 01
2	0	0	40H	Data for Row 1
3	0	0	41H	Data for Row 2
4	0	0	45H	Data for Row 3
5	0	0	49H	Data for Row 4
6	0	0	5FH	Data for Row 5
7	0	0	48H	Data for Row 6
8	0	0	44H	Data for Row 7
9	0	0	40H	Data for Row 8

Notes:
1. These steps do not include busy flag checks.
2. Row 8 maybe used by the underline cursor.

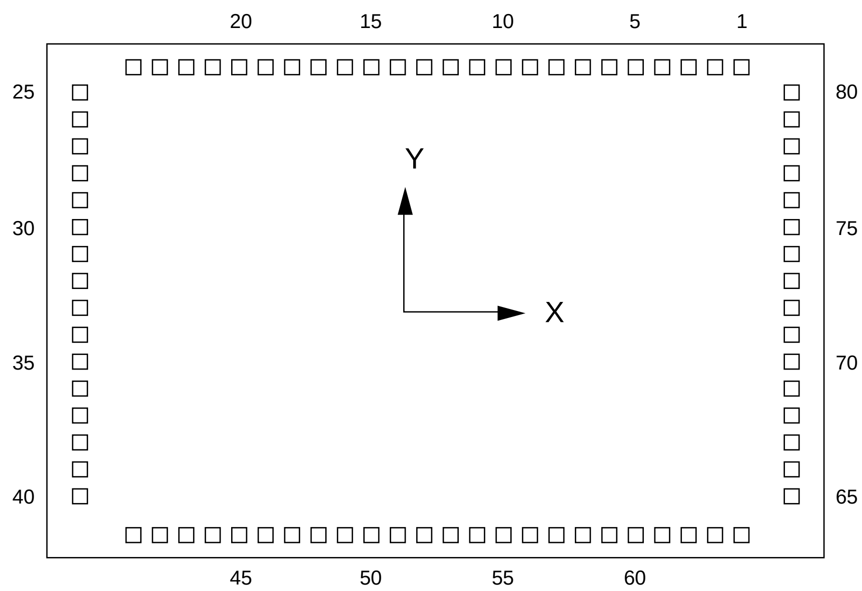
Mechanical Specifications

SED1200F Package Dimensions



SED1200D Package Dimensions

Chip size:	5.86 mm × 3.41 mm
Chip thickness:	0.40 mm ± 0.03 mm
Pad size:	0.90 mm × 0.90 mm
Pad pitch:	0.19 mm



Pad Number	Pad Name	X (μm)	Y (μm)	Pad Number	Pad Name	X (μm)	Y (μm)
1	SEG17	2123	1552	41	COM10	–2220	–1552
2	SEG16	1932	1552	42	COM11	–2029	–1552
3	SEG15	1742	1552	43	COM12	–1839	–1552
4	SEG14	1551	1552	44	COM13	–1648	–1552
5	SEG13	1361	1552	45	COM14	–1458	–1552
6	SEG12	1170	1552	46	COM15	–1267	–1552
7	SEG11	980	1552	47	COM16	–1077	–1552
8	SEG10	789	1552	48	SEG50	–886	–1552
9	SEG9	599	1552	49	SEG49	–696	–1552
10	SEG8	408	1552	50	SEG48	–505	–1552
11	SEG7	218	1552	51	SEG47	–315	–1552
12	SEG6	27	1552	52	SEG46	–124	–1552
13	SEG5	–163	1552	53	SEG45	66	–1552
14	SEG4	–354	1552	54	SEG44	257	–1552
15	SEG3	–544	1552	55	SEG43	447	–1552
16	SEG2	–735	1552	56	SEG42	638	–1552
17	SEG1	–925	1552	57	SEG41	828	–1552
18	COM1	–1116	1552	58	SEG40	1019	–1552
19	COM2	–1306	1552	59	SEG39	1209	–1552
20	COM3	–1497	1552	60	SEG38	1400	–1552
21	COM4	–1687	1552	61	SEG37	1590	–1552
22	COM5	–1878	1552	62	SEG36	1781	–1552
23	COM6	–2068	1552	63	SEG35	1971	–1552
24	COM7	–2259	1552	64	SEG34	2162	–1552
25	COM8	–2778	1429	65	SEG33	2777	–1385
26	A0	–2778	1238	66	SEG32	2777	–1195
27	$\overline{CS}$	–2778	1048	67	SEG31	2777	–1004
28	$\overline{RD}$	–2778	857	68	SEG30	2777	–814
29	$\overline{WR}$	–2778	667	69	SEG29	2777	–623
30	Φ	–2778	476	70	SEG28	2777	–433
31	OSC2	–2778	286	71	SEG27	2777	–242
32	OSC1	–2778	95	72	SEG26	2777	–52
33	D3	–2778	–95	73	SEG25	2777	139
34	D2	–2778	–286	74	SEG24	2777	329
35	D1	–2778	–476	75	SEG23	2777	520
36	D0	–2778	–667	76	SEG22	2777	710
37	V_{SS}	–2778	–857	77	SEG21	2777	901
38	V_{LCD}	–2778	–1048	78	SEG20	2777	1091
39	V_{DD}	–2778	–1238	79	SEG19	2777	1282
40	COM9	–2778	–1429	80	SEG18	2777	1472

APPLICATION NOTES

Display Oscillator

The SED1200 has an internal oscillator to generate the timing signals required for the LCD display.
If the internal oscillator is used, connect the feedback resistor Rf as shown in figure 3. The feedback resistor leads must be kept as short as possible to reduce stray capacitance and the possibility of crosstalk between the oscillator and adjoining signals.

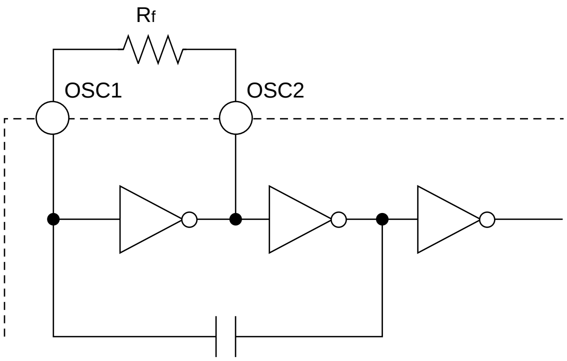


Figure 3. Using the Internal Oscillator

If an external clock is used, connect it to OSC1, as shown in figure 4.

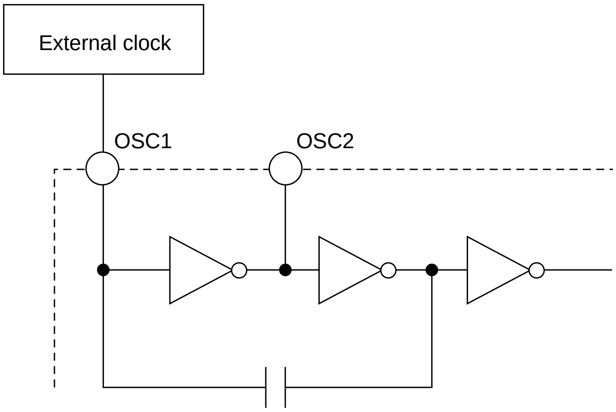


Figure 4. Using an External Clock

The relationship between the oscillator frequency and the LCD drive frame frequency is

$f_{FR} = f_{OSC}/1600$
For example if f_{OSC} = 100 kHz, f_{FR} = 62.5 Hz

Command Clock (Φ)

When the system MPU issues a command to the SED1200, the timing for the execution of the command is derived from Φ, the command clock. This would normally be the system MPU clock.
The maximum execution time for a command is 16/Φ. For example if Φ= 1 MHz, the maximum execution time for a command is 16 µs.

LCD Drive Waveforms

The SED1200 has an internal low source-impedance voltage-driver network, of the form shown in figure 5. The switches S_{Wd} are closed to switch the segment data.

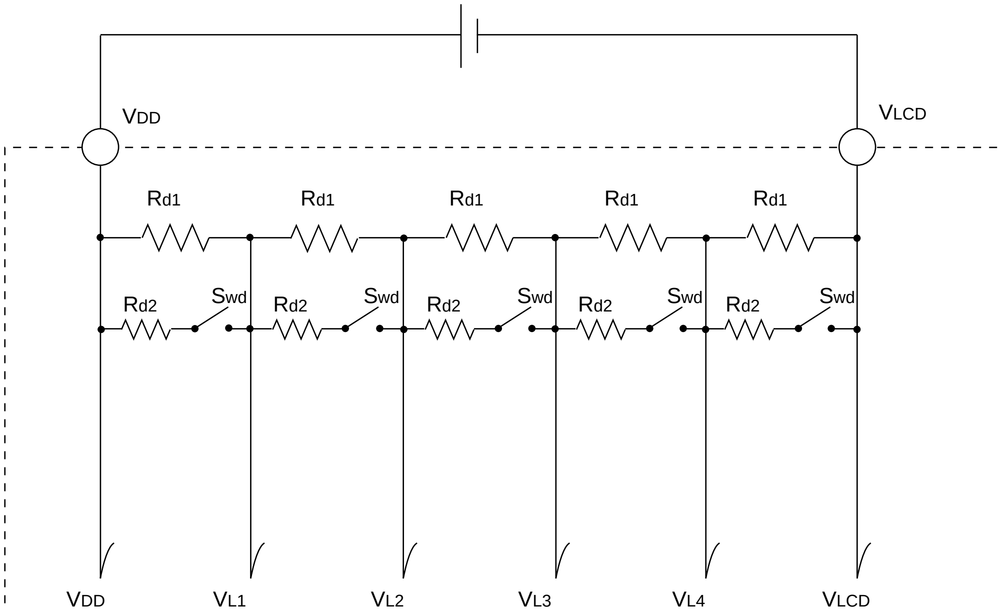
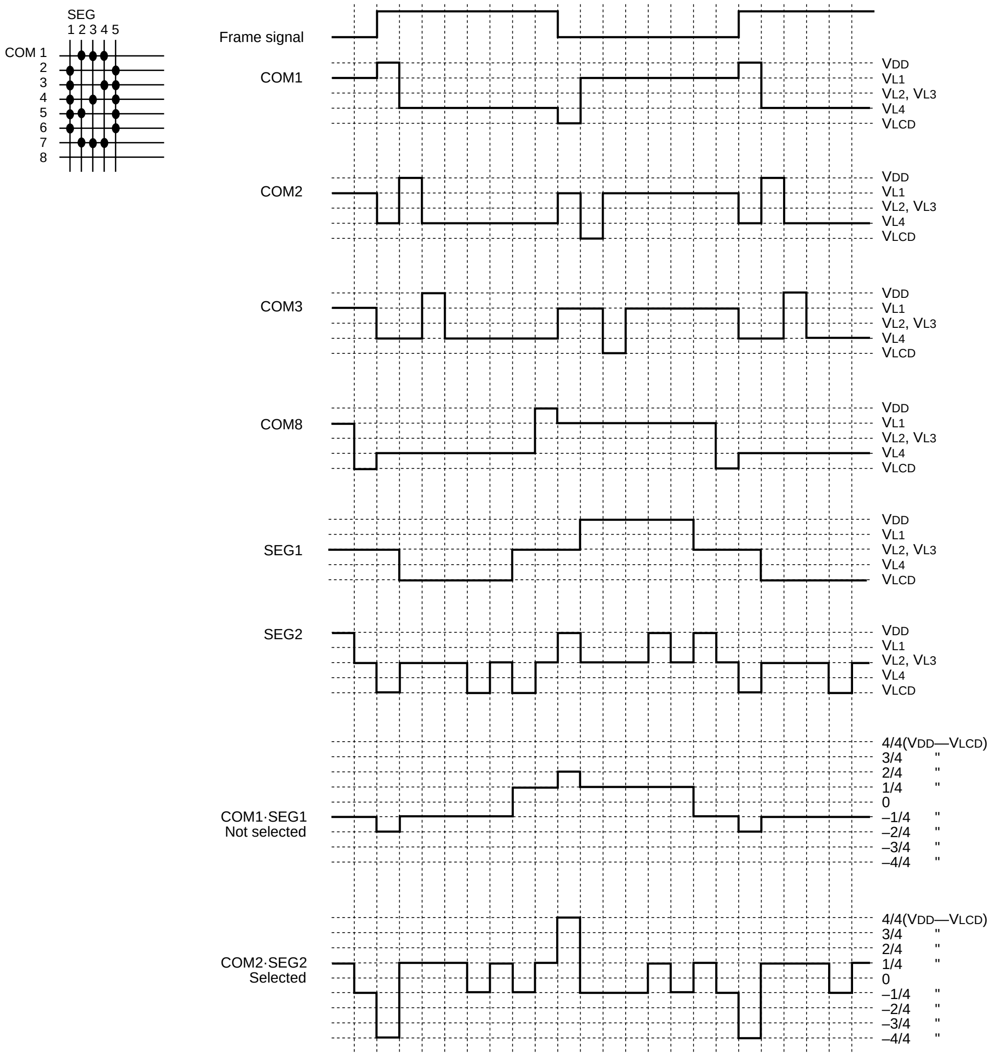
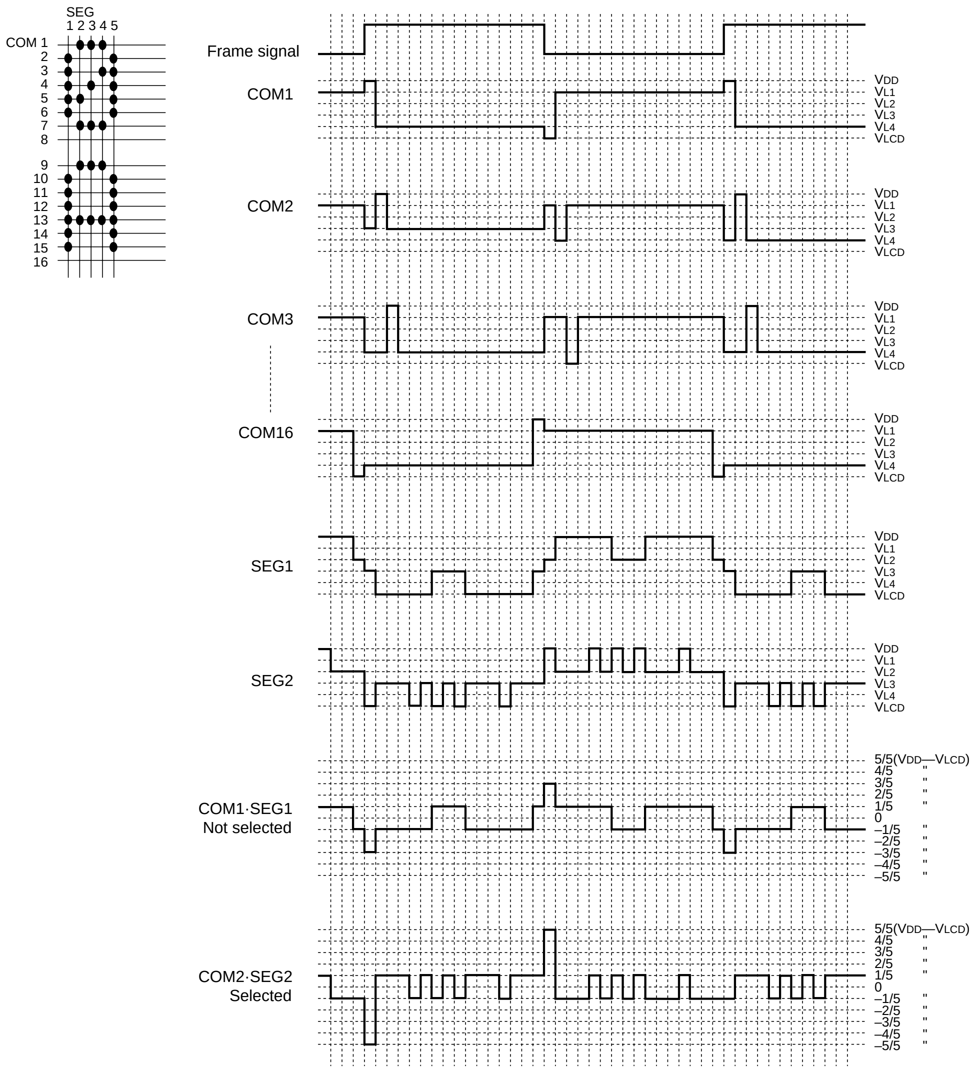


Figure 5. Internal Voltage Divider

• LCD Drive Waveform – 1 Line Display (1/8 Duty Cycle)

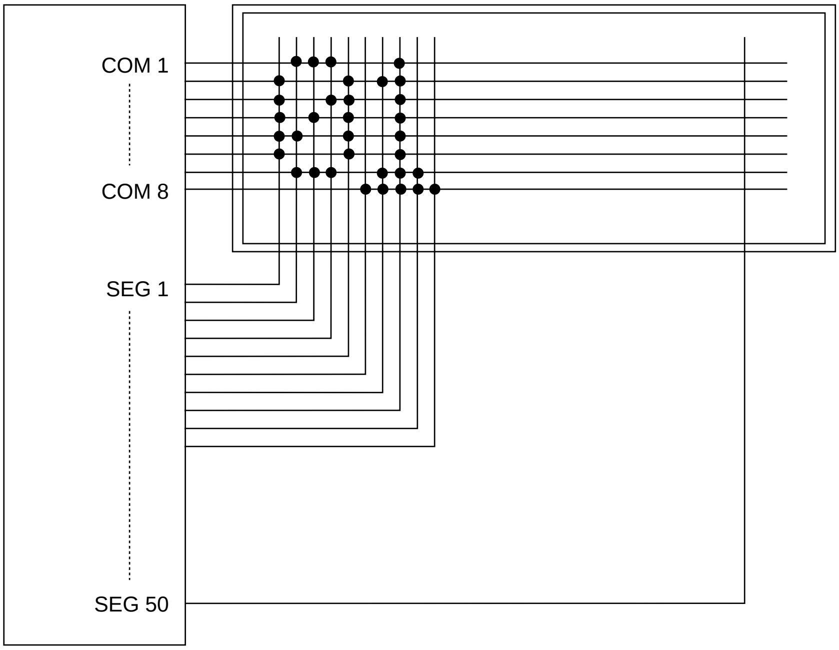


• LCD Drive Waveform – 2 Line Display (1/16 Duty Cycle)

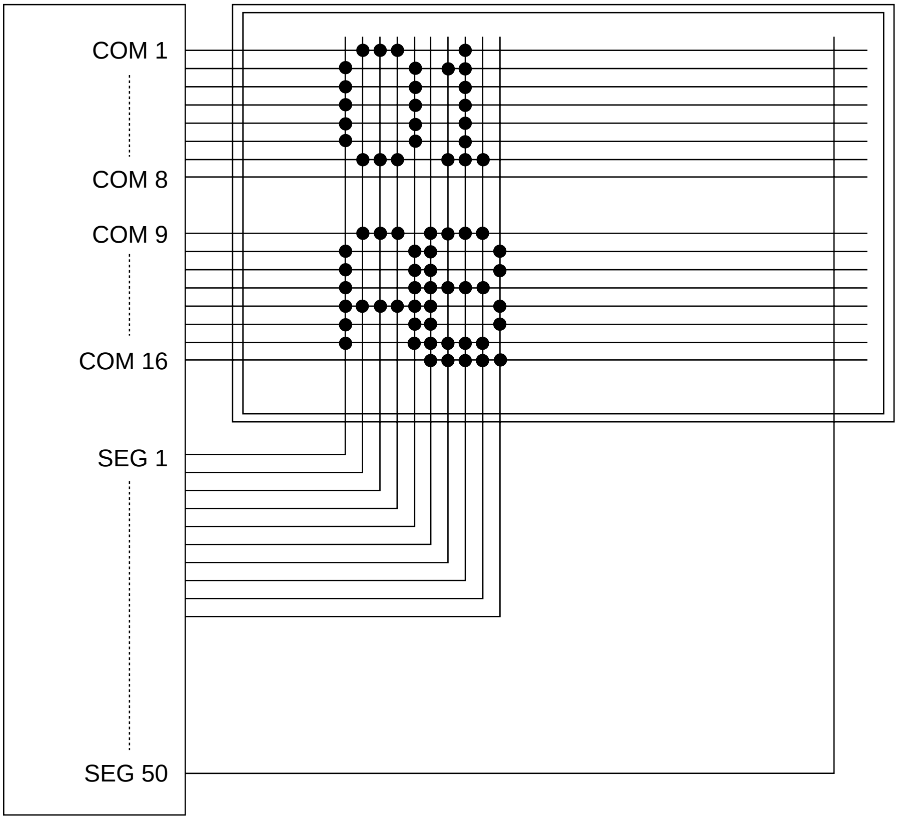


LCD Display Interface

- 10 Characters on 1 line (1/8 duty)

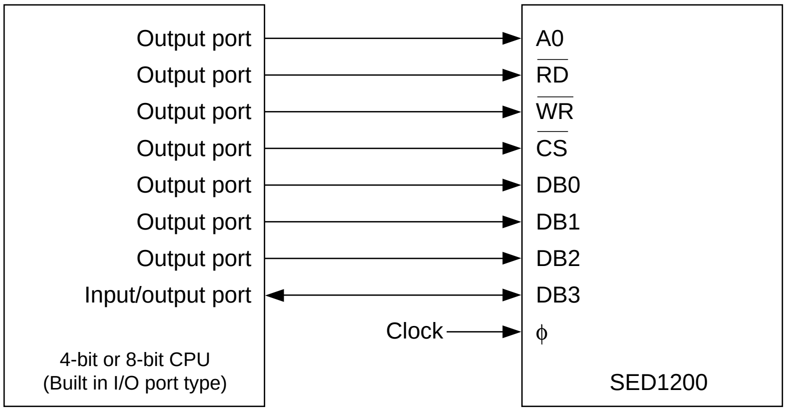


- 10 Characters on 2 lines (1/16 duty)

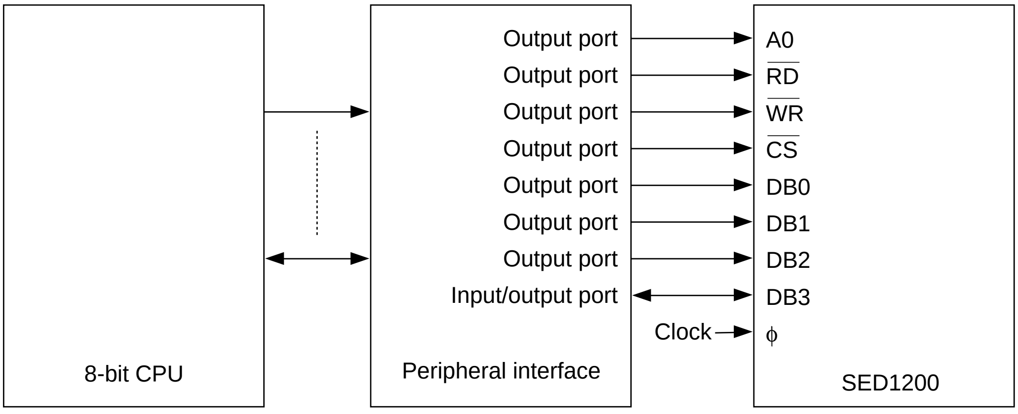


CPU Interface

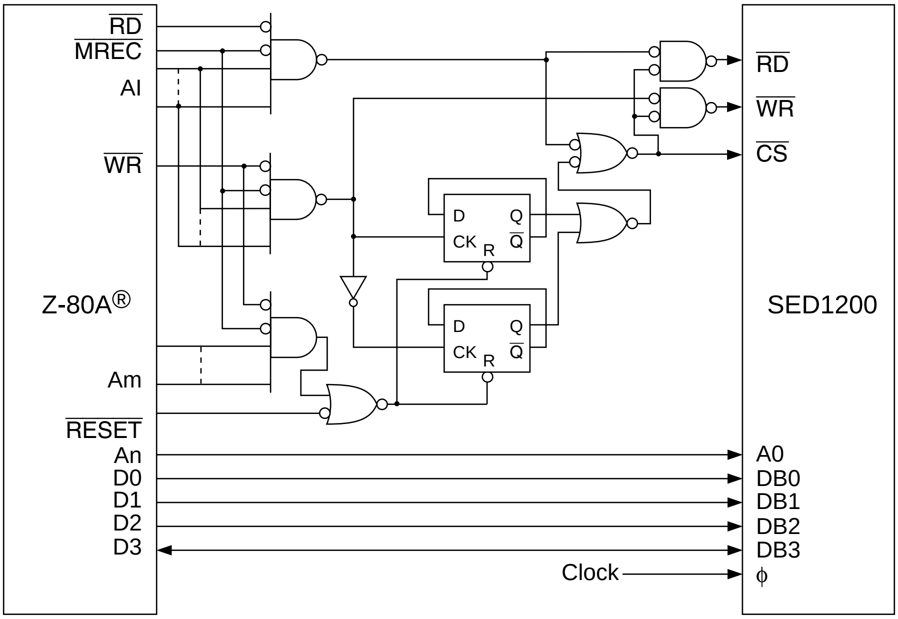
- 4-bits CPU with internal I/O port



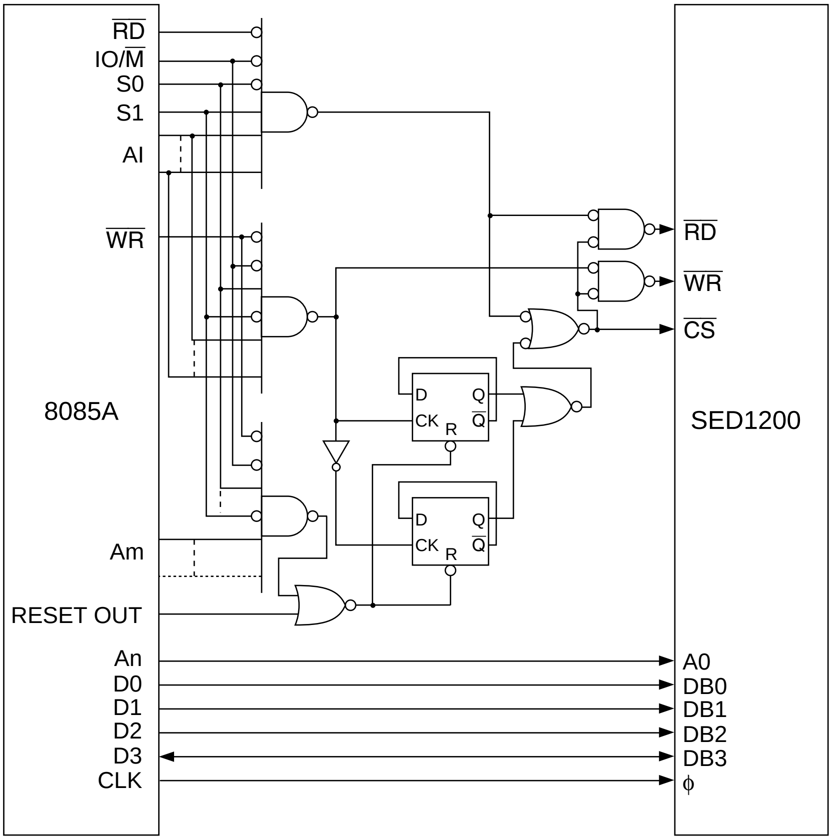
- 8-bit CPU with external I/O port



- Interface with Z-80A type CPU



• Interface with 8085A type CPU



APPENDIX A: CHARACTER CODES AND FONTS

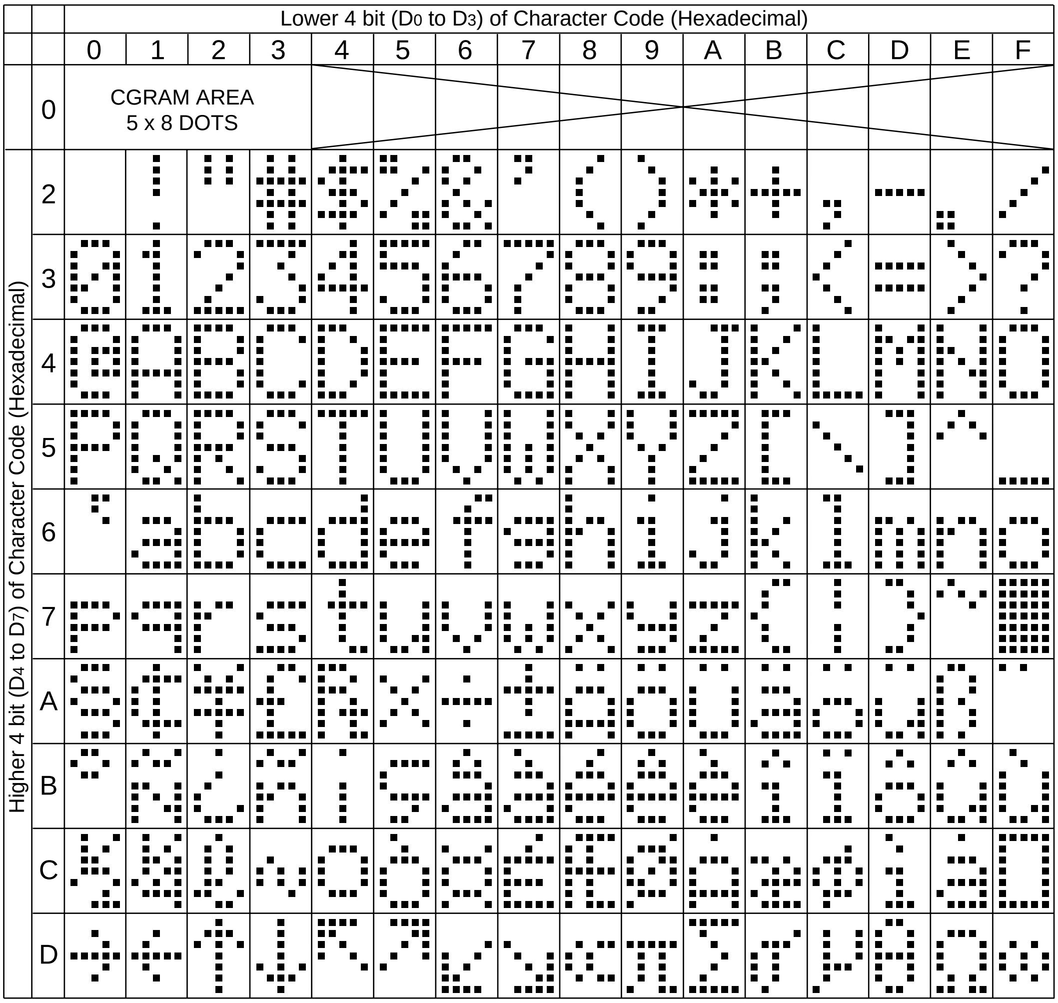
SED1200F0A/SED1200D0A

Lower 4 bit (D_0 to D_3) of Character Code (Hexadecimal); Higher 4 bit (D_4 to D_7) of Character Code (Hexadecimal)

Higher \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CGRAM AREA 5 x 8 DOTS															
2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	¥	]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	→	←
A		。	「	」	、	・	ヲ	ァ	ィ	ゥ	ェ	ォ	ャ	ュ	ョ	ッ
B	ー	ア	イ	ウ	エ	オ	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ
C	タ	チ	ツ	テ	ト	ナ	ニ	ヌ	ネ	ノ	ハ	ヒ	フ	ヘ	ホ	マ
D	ミ	ム	メ	モ	ヤ	ユ	ヨ	ラ	リ	ル	レ	ロ	ワ	ン	゛	゜

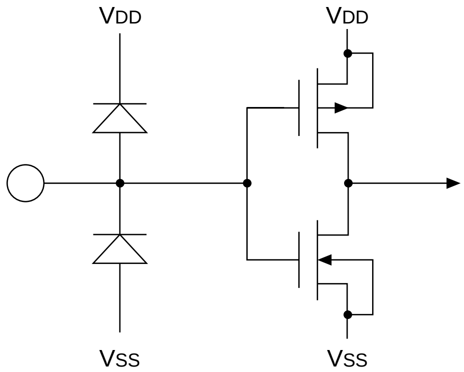
SED1200 Series

SED1200F0B/SED1200D0B

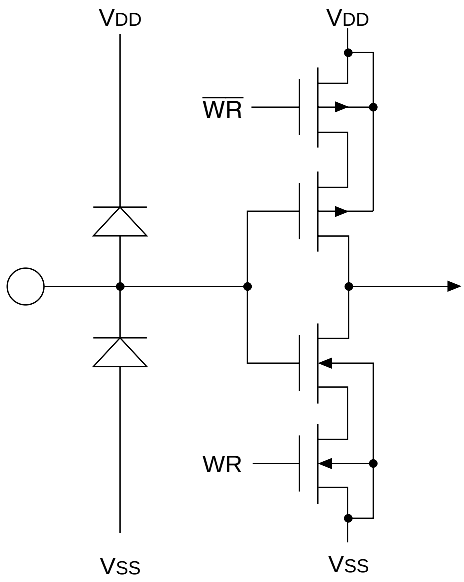


APPENDIX B: I/O TERMINAL STRUCTURE

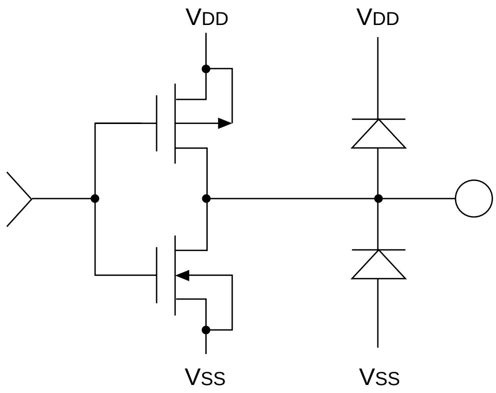
- Input Terminal (No pull-up)
  Terminals used: Φ, OSC1



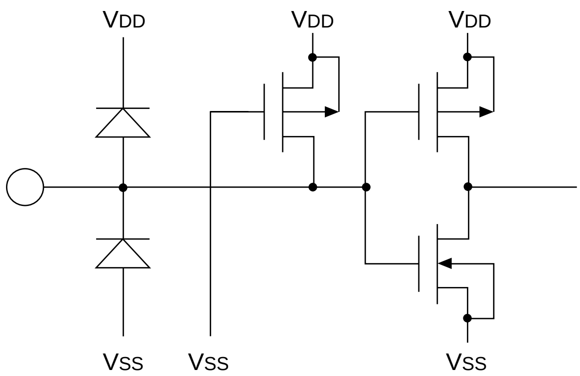
- Input Terminal (No pull-up)
  Terminals used: D0 to D2



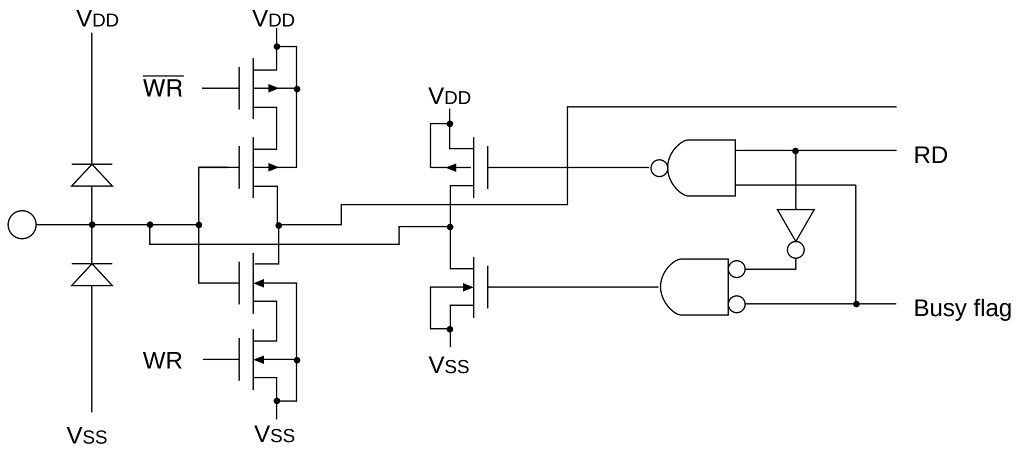
- Output Terminal (No pull-up)
  Terminals used: OSC2



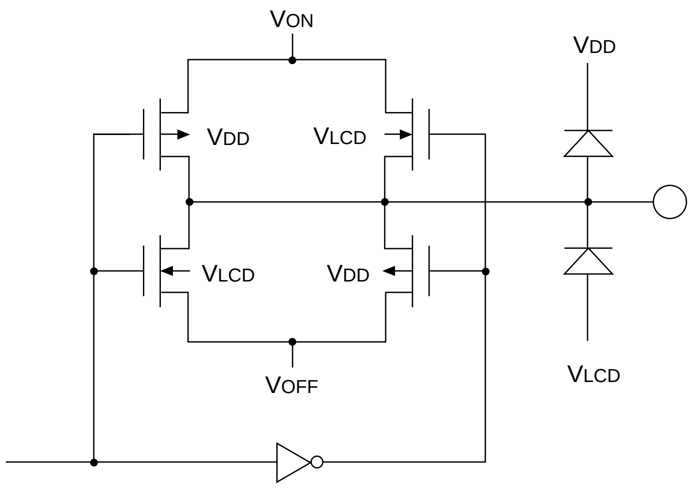
- Input Terminal (Pull-up)
  Terminals used: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0



- I/O Terminal (No pull-up)
  Terminals used: D3



- LCD Drive Terminal (No pull-up)
  Terminals used: SEG1 to SEG50, COM1 to COM16



SED1210
LCD Controller/Drivers

Technical Manual

Contents

OVERVIEW

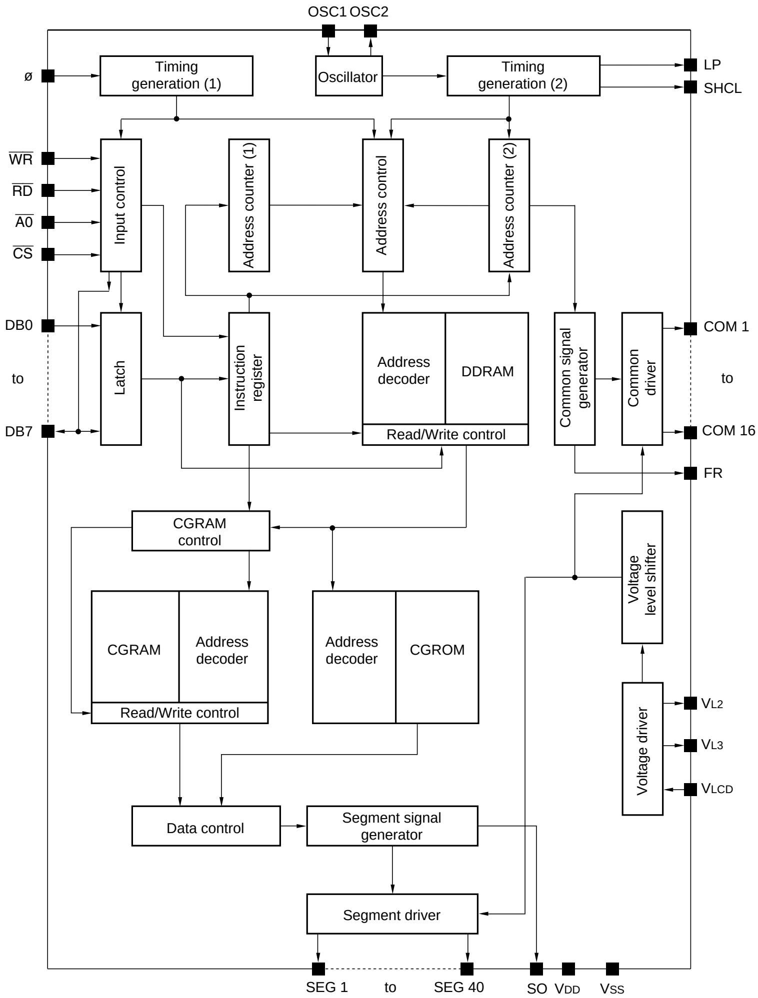
The SED1210F is a Liquid Crystal Display (LCD) character display controller/driver, capable of directly driving displays of up to 16 characters. If an external expansion driver is used, displays of up to 40 characters can be generated.

The SED1210F has an internal character generator (CG) consisting of 160 JIS ASCII characters in ROM and four user definable characters in RAM. The internal CG, combined with a versatile set of cursor and display control commands, means that the system CPU is only responsible for the display data and commands, and not for the LCD display itself.

FEATURES

- Internal display RAM to hold 40 8-bit character codes.
- Internal character generator
  - CGROM: 160 JIS ASCII characters.
  - CGRAM: 4 user programmable 5×8 pixel characters
  - Font: 5×7 pixel characters plus the underline cursor, of 5×8 pixel characters alone.
  - JIS character set using SED1210F0A
  - ASCII character set using SED1210F0B
- Internal LCD driver circuitry
  - 40 segment driver outputs
  - 16 common driver outputs
  - Total size: 2 lines of 20 characters each (maximum). One line of 40 characters (using an SED1181F for external expansion)
- CPU interface
  - 8-bit CPU data bus
  - 13 display control commands
- Low external component count
  - Built in RC oscillator (using one external feedback resistor)
  - Built in LCD driver voltage-divider network.
- Implemented using low power CMOS technology
  - TTL compatible CPU interface
- Power supply
  - Logic: 2.5 V to 5.5 V
  - LCD: 3.5 V to 5.5 V
- 80-pin QFP package (plastic)

BLOCK DIAGRAM



PINOUT

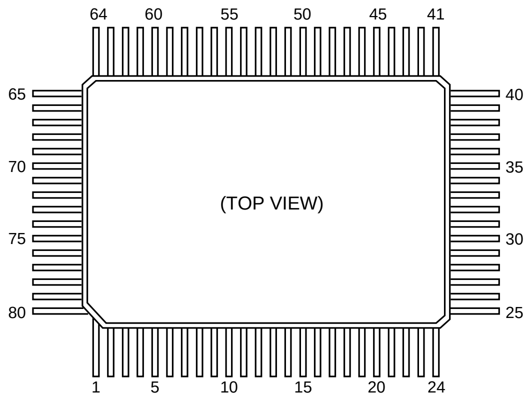


TABLE 1. SED1210F Pinout

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	SEG17	21	COM4	41	COM10	61	SEG37
2	SEG16	22	COM5	42	COM11	62	SEG36
3	SEG15	23	COM6	43	COM12	63	SEG35
4	SEG14	24	COM7	44	COM13	64	SEG34
5	SEG13	25	COM8	45	COM14	65	SEG33
6	SEG12	26	A0	46	COM15	66	SEG32
7	SEG11	27	$\overline{CS}$	47	COM16	67	SEG31
8	SEG10	28	$\overline{RD}$	48	SO	68	SEG30
9	SEG9	29	$\overline{WR}$	49	LP	69	SEG29
10	SEG8	30	Φ	50	SHCL	70	SEG28
11	SEG7	31	OSC2	51	FR	71	SEG27
12	SEG6	32	OSC1	52	D3	72	SEG26
13	SEG5	33	D7	53	D2	73	SEG25
14	SEG4	34	D6	54	D1	74	SEG24
15	SEG3	35	D5	55	D0	75	SEG23
16	SEG2	36	D4	56	V_{L2}	76	SEG22
17	SEG1	37	V_{SS}	57	V_{L3}	77	SEG21
18	COM1	38	V_{LCD}	58	SEG40	78	SEG20
19	COM2	39	V_{DD}	59	SEG39	79	SEG19
20	COM3	40	COM9	60	SEG38	80	SEG18

PIN DESCRIPTION

CPU Interface

$\overline{\text{CS}}$	Active low chip select input.
$\overline{\text{RD}}$	Active low read enable input.
$\overline{\text{WR}}$	Active low write strobe.
A0	Selects between instruction and display data access. A0 = H: Display data A0 = L: Instruction
DB0–DB6	Active high CPU data inputs.
DB7	Active high CPU data input/output.
Φ	Clock input for command execution.

LCD Interface

COM1–COM16	LCD command driver outputs.
SEG1–SEG40	LCD segment driver outputs.
SO	Serial segment data output
LP	Latch output to segment driver
SHCL	Shift clock output to segment
FR	Frame output to segment driver

Oscillator

OSC1, OSC2	Terminals for the oscillator external feedback resistor, R_f. If an externally generated clock is used, it is connected to OSC1; OSC2 is left open.

Power Supply

V_{DD}	Logic power supply input
V_{LCD}	LCD power supply input
V_{SS}	System ground (0 V) input
V_{L2}, V_{L3}	LCD driver voltage outputs

COMMAND DESCRIPTION

Command Summary

TABLE 2. SED1210F Command Summary

COMMAND NAME	$\overline{\text{CS}}$	$\overline{\text{WR}}$	$\overline{\text{RD}}$	$\overline{\text{A0}}$	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
SET CURSOR DIRECTION	0	0	1	0	0	0	0	0	0	1	0	D/I	D0 = 1 ... Decrement D0 = 0 ... Increment
CURSOR ADDRESS –1/+1	0	0	1	0	0	0	0	0	0	1	1	–1/+1	D0 = 1 ... Cursor address –1 D0 = 0 ... Cursor address +1
CURSOR FONT SELECT	0	0	1	0	0	0	0	0	1	0	0	A/U	D0 = 1 ... All dots blinking D0 = 0 ... Underline
CURSOR BLINK ON/OFF	0	0	1	0	0	0	0	0	1	0	1	ON/OFF	D0 = 1 ... ON D0 = 0 ... OFF
DISPLAY ON/OFF	0	0	1	0	0	0	0	0	1	1	0	ON/OFF	D0 = 1 ... ON D0 = 0 ... OFF
CURSOR ON/OFF	0	0	1	0	0	0	0	0	1	1	1	ON/OFF	D0 = 1 ... ON D0 = 0 ... OFF
SYSTEM RESET	0	0	1	0	0	0	0	1	0	0	0	0	DATA RAM & CGRAM are not affected
LINE SELECT	0	0	1	0	0	0	0	1	0	0	1	2/1	D0 = 1 ... 2 line display (1/16 duty) D0 = 0 ... 1 line display (1/8 duty)
SET CGRAM ADDRESS	0	0	1	0	0	0	1	0	(LOWER ADDRESS)				Upper address fixed at 0H
SET CGRAM DATA	0	0	1	0	0	1	0	(CGRAM DATA)					
SET CURSOR ADDRESS	0	0	1	0	1	2nd/1st (N DIGIT-1)							D6 = 1 ... 2nd line N digit address D6 = 0 ... 1st line N digit address
SET CHARACTER CODE	0	0	1	1	(CHARACTER CODE)								
BUSY FLAG CHECK	0	1	0	0	BF	*	*	*	*	*	*	*	* High impedance

Write Commands

SET CURSOR DIRECTION

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	D

Sets the way in which the cursor address register changes as character data is written to the SED1210F by the CPU, and hence the direction of cursor movement.

D = 0: Address register increment direction
D = 1: Address register decrement direction

CURSOR ADDRESS –1/+1

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	D

Adds one to, or subtracts one from, the current contents of the cursor address register, and hence moves the cursor.

D = 0: ADDRESS = ADDRESS + 1
D = 1: ADDRESS = ADDRESS – 1

CURSOR FONT SELECT

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	D

D = 0: Underline cursor
D = 1: All dots blinking

CURSOR BLINK ON/OFF

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	D

Controls flashing of the underline cursor.
D = 0: Blinking stopped
D = 1: Cursor blinking

DISPLAY ON/OFF

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	D

D = 0: Display off
D = 1: Display on
Note: This command does not affect the contents of the display data RAM.

CURSOR ON/OFF

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	D

Controls the display of the cursor.
D = 0: Cursor off.
D = 1: Cursor on.

SYSTEM RESET

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0

Initializes the SED1210F to the following defaults.
CURSOR DIRECTION: Increment
CURSOR FONT: Underline
CURSOR BLINK: Off
DISPLAY: Off
CURSOR: Off
LINE SELECT: One line display
CURSOR ADDRESS: Address 0 (Line 1, character 0)
Note: SYSTEM RESET does not affect the contents of the display data RAM, or the CGRAM.

LINE SELECT

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	D

Selects the number of displayed lines, and hence the LCD drive duty cycle.
D = 0: 1 line display (1/8 duty cycle)
D = 1: 2 line display (1/16 duty cycle)
Note: The number of lines which can be displayed depends on the LCD panel used.

SET CURSOR ADDRESS

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	L	P_5	P_4	P_3	P_2	P_1	P_0

Presets the contents of the cursor address register, and hence the position of the cursor.
L = 0: Line 1 select
L = 1: Line 2 select
P_5–P_0: Position of character in selected line.

SET CHARACTER CODE

A0 = 1

D7	D6	D5	D4	D3	D2	D1	D0
C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

Writes the character code given by C_7–C_0 into the character data RAM at the location pointed to by the cursor address register. The contents of the cursor address register are then modified as specified by the last SET CURSOR DIRECTION instruction.

SET CGRAM ADDRESS

$\overline{WR}$ = 0, A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	*	*	A_1	A_0

Presets the contents of the CGRAM address register to the position of one of the four user definable characters. The address is specified by A_1 and A_0.

SET CGRAM DATA

Loads the bit pattern D_4–D_0 into the CGRAM location specified by the current contents of the CGRAM address register. The contents of the CGRAM address register are incremented following each write of a SET CGRAM DATA instruction by the CPU.

A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	D_4	D_3	D_2	D_1	D_0

See Loading CGRAMs.

Read Commands

BUSY FLAG CHECK

Reading yields the status of the SED1210F.

$\overline{RD}$ = 0, A0 = 0

D7	D6	D5	D4	D3	D2	D1	D0
BF	*	*	*	*	*	*	*

BF = 0: SED1210F READY
BF = 1: SED1210F BUSY
Bits D_6–D_0 are tristate during reads of the Busy Flag.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = GND = 0 V and Ta = 25°C unless otherwise specified

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to +7.0	V
Supply voltage (2)	V_{LCD}	V_{DD}–7.0 to V_{DD}+0.3	V
Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	–0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	–20 to +70	°C
Storage temperature	T_{stg}	–60 to +150	°C
Soldering temperature and time	T_{sol}	260, 10	°C, s

Note: Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these condition is not implied.

Electrical Specifications

DC Characteristics

V_{DD} = 5 V

V_{SS} = 0 V, Ta = –20 to +70°C

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit	Pin
Liquid crystal display supply voltage	V_{LCD}		V_{DD}–5.5	—	V_{DD}–3.5	V	V_{LCD}
Oscillator feedback resistor	R_f	V_{DD} = 5.0 V, f_{OSC} = 100 kHz	240	310	380	kΩ	OSC1, OSC2
Oscillator frequency	fosc	V_{DD} = 5.0V V, Rf = 300 kΩ	—	100	—	kHz	OSC1, OSC2
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 4.5V	—	—	300	kHz	OSC1
Operating frequency (2)	Φ	V_{DD} = 4.5 to 5.5 V	—	—	3.2	MHz	Φ
External clock duty		V_{DD} = 4.5 to 5.5 V	45	50	55	%	OSC1, Φ
External clock rise time	t_r	V_{DD} = 4.5 to 5.5 V	—	—	50	ns	OSC1, Φ
External clock fall time	t_f	V_{DD} = 4.5 to 5.5 V	—	—	50	ns	OSC1, Φ
H-level input voltage (1)	V_{IH1}	V_{DD} = 4.5 to 5.5 V	2.0	—	V_{DD}	V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB7, Φ, A0
L-level input voltage (1)	V_{IL1}	V_{DD} = 4.5 to 5.5 V	0	—	0.8	V	
H-level input voltage (2)	V_{IH2}	V_{DD} = 4.5 to 5.5 V	0.8 V_{DD}	V_{DD}	V_{DD}	V	OSC1
L-level input voltage (2)	V_{IL2}	V_{DD} = 4.5 to 5.5 V	0	0	0.2 V_{DD}	V	OSC1
H-level input leakage current	I_{LIH}	V_{DD} = 5.5 V, V_{IH} = 5.5 V	—	—	|–1.0|	µA	Φ, OSC1, DB0 to DB7
L-level input leakage current	I_{LIL}	V_{DD} = 5.5 V, V_{IL} = 0 V	—	—	1.0	µA	
Input pull-up current	I_{IPU}	V_{DD} = 5.0 V, V_{IL} = 0 V	3.0	10	30	µA	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0
H-level output current (1)	I_{OH1}	V_{DD} = 4.5 to 5.5 V, V_{OH} = 2.4 V	|–1.0|	—	—	mA	DB7
L-level output current (1)	I_{OL1}	V_{DD} = 4.5 to 5.5 V, V_{OL} = 0.4 V	1.6	—	—	mA	DB7
H-level output current (2)	I_{OH2}	V_{DD} = 4.5 V, V_{OH} = 4.0 V	200	—	—	µA	FR, LP
L-level output current (2)	I_{OL2}	V_{DD} = 4.5 V, V_{OL} = 0.5V	200	—	—	µA	XSCL, SO
Common driver output current (1)	I_{OH}	V_{DD} level; V_{DD}–V_{LCD} = 3.5 V Dividing resistor in low impedance state. 1/16 duty. 0.5 V voltage drop. Measured on one pin with other pins open circuit.	|–20|	—	—	µA	COM1 to COM16
Common driver output current (2)	I_{OL}	V_{LCD} level	20	—	—	µA	COM1 to COM16
Common driver output current (3)	I_{OL}	V_{L1} level	|±8|	—	—	µA	COM1 to COM16
Common driver output current (4)	I_{OL}	V_{L4} level	|±8|	—	—	µA	COM1 to COM16
Segment driver output current (1)	I_{OH}	V_{DD} level	|–12|	—	—	µA	SEG1 to SEG40
Segment driver output current (2)	I_{OL}	V_{LCD} level	12	—	—	µA	SEG1 to SEG40
Segment driver output current (3)	I_{OL}	V_{L2} level	|±4|	—	—	µA	SEG1 to SEG40
Segment driver output current (4)	I_{OL}	V_{L3} level	|±4|	—	—	µA	SEG1 to SEG40
Driver current	I_{OH}	V_{DD}–V_{LCD} = 3.5V	—	2	—	µA	V_{L2}, V_{L3}
	I_{CL}	0.5 V voltage drop	—	2	—	µA	
Voltage-divider resistor (1)	R_{d1}	Normal conditions	30	130	300	kΩ	
Voltage-divider resistor (2)	R_{d2}	Low impedance state	3.0	13	30	kΩ	
Voltage-divider resistor low impedance duty	t_{Rd1}/t_{Rd2}	1/8 Duty	—	11/400	—	—	
		1/16 Duty	—	11/200	—	—	
Command execution time	t_{comd}	From $\overline{WR}$ rising edge to the end of internal processing	—	—	16/Φ	µs	
Average operating current	I_{DD}	V_{DD} = 5.0 V, V_{LCD} = 0 V, f_{OSC} = 100 kHz, Φ = 1 MHz, $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = 5.0 V, output open	—	80	150	µA	V_{DD}

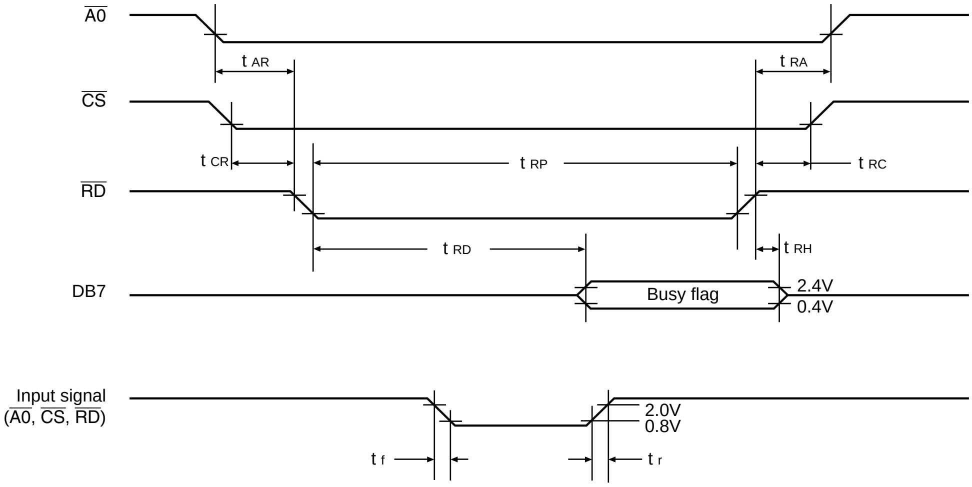
V_{DD} = 3 V

V_{SS} = 0 V, Ta = –20 to 70°C

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit	Pin
Liquid crystal display supply voltage	V_{LCD}		3.5	—	5.5	V	V_{LCD}
Oscillator feedback resistor	R_f	V_{DD} = 3.0 V, f_{OSC} = 100 kHz	210	290	370	kΩ	OSC1, OSC2
Oscillator frequency	f_{OSC}	V_{DD} = 3.0 V, R_f = 300 kΩ	—	100	—	kHz	OSC1, OSC2
Operating frequency (1) oscillator or external clock frequency	f_{OSC}	V_{DD} = 2.5 V	—	—	300	kHz	OSC1
Operating frequency (2)	Φ	V_{DD} = 2.5 to 4.5 V	—	—	1	MHz	Φ
External clock duty		V_{DD} = 2.5 to 4.5 V	—	50	—	%	OSC1, Φ
External clock rise time	t_r	V_{DD} = 2.5 to 4.5 V	—	—	50	ns	OSC1, Φ
External clock fall time	t_f	V_{DD} = 2.5 to 4.5 V	—	—	50	ns	OSC1, Φ
H-level input voltage (1)	V_{IH1}	V_{DD} = 2.5 to 4.5 V	0.8 V_{DD}	—	—	V	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0 DB0 to DB7, Φ
L-level input voltage (1)	V_{IL1}	V_{DD} = 2.5 to 4.5 V	—	—	0.2 V_{DD}	V	
H-level input voltage (2)	V_{IH2}	V_{DD} = 2.5 to 4.5 V	0.8 V_{DD}	—	—	V	OSC1
L-level input voltabe (2)	V_{IL2}	V_{DD} = 2.5 to 4.5 V	—	—	0.2 V_{DD}	V	
H-level input leakage current	I_{LIH}	V_{DD} = 4.5 V	—	—	—	µA	Φ, OSC1, DB0 to DB7
L-level input leakage current	I_{LIL}	V_{DD} = 4.5 V	—	—	—	µA	
Input pull-up current	I_{IPU}	V_{DD} = 3.5 V	—	—	—	µA	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0
H-level output current (1)	I_{OH1}	V_{DD} = 2.5 V, V_{OH} = 2.0 V	200	—	—	µA	DB7
L-level output current (1)	I_{OL1}	V_{DD} = 2.5 V, V_{OL} = 0.5 V	200	—	—	µA	
H-level output current (2)	I_{OH2}	V_{DD} = 2.5 V, V_{OH} = 2.0 V	200	—	—	µA	FR, LP
L-level output current (2)	I_{OL2}	V_{DD} = 2.5 V, V_{OL} = 0.5 V	200	—	—	µA	XSCL, SO
Common driver output current (1)	I_{OH}	V_{DD} level; V_{DD}-V_{LCD} = 3.5 V Diving resistor in low impedance state. 1/16 duty 0.5 V voltage drop. Measured on one pin with other pins open circuit.	|-20|	—	—	µA	COM1 to COM16
Common driver output current (2)	I_{OL}	V_{LCD} level	20	—	—	µA	
Common driver output current (3)	I_{OL}	V_{L1} level	|±8|	—	—	µA	
Common driver output current (4)	I_{OL}	V_{L4} level	|±8|	—	—	µA	
Segment drivrer output current (1)	I_{OH}	V_{DD} level	|–12|	—	—	µA	SEG1 to SEG40
Segment drivrer output current (2)	I_{OL}	V_{LCD} level	12	—	—	µA	
Segment drivrer output current (3)	I_{OL}	V_{L2} level	|±4|	—	—	µA	
Segment drivrer output current (4)	I_{OL}	V_{L3} level	|±4|	—	—	µA	
Driver current (1)	I_{OH}	V_{DD}–V_{LCD} = 3.5 V 0.5 V voltage drop	—	2	—	µA	V_{L2}, V_{L3}
Driver current (2)	I_{OL}		—	2	—	µA	
Voltage-divider resistor (1)	R_{d1}	Normal conditions	—	130	—	kΩ	
Voltage-divider resistor (2)	R_{d2}	Low impedance state	—	13	—	kΩ	
Voltage-divider resistor low impedance duty	t_{Rd1}/t_{Rd2}	1/8 Duty	—	11/400	—	—	
		1/16 Duty	—	11/200	—		
Command execuiton time	t_{comd}	From $\overline{WR}$ rise time to the end of internal processing	—	—	16/Φ	µs	
Average operating current	I_{DD}	V_{DD}–V_{SS} = 3.5 V V_{DD}–V_{LCD} = 5 V Φ = 500 kHz $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = V_{DD} Rf = 300 kΩ	—	60	—	µA	V_{DD}

AC Characteristics

MPU Read Timing



V_{DD} = 5 V, Ta = –20 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
Setup time for A0 → $\overline{RD}$	t_{AR}	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	0	—	—	ns
$\overline{RD}$ delay output time*	t_{RD}	—	—	200	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	20	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	20	—	—	ns
Data hold time	t_{RH}	10	—	—	ns
Read pulsewidth	t_{RP}	300	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

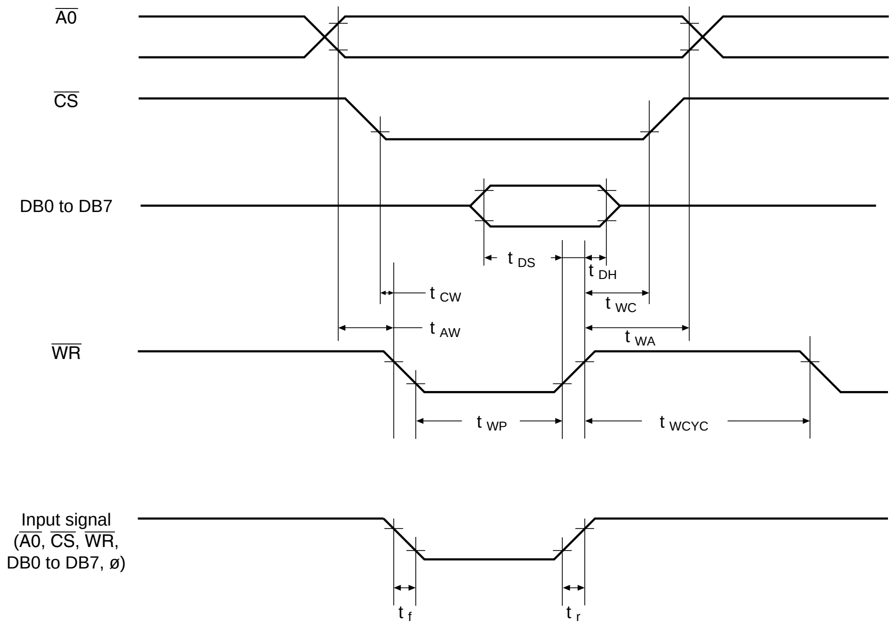
Note: Load on pin DB7 is C_L = 100 pF.

VDD = 3 V, Ta = –20 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
Setup time for A0 → $\overline{RD}$	t_{AR}	0	—	—	ns
Setup time for $\overline{CS}$ → $\overline{RD}$	t_{CR}	0	—	—	ns
$\overline{RD}$ delay output time*	t_{RD}	—	—	350	ns
Hold time for $\overline{RD}$ → A0	t_{RA}	0	—	—	ns
Hold time for $\overline{RD}$ → $\overline{CS}$	t_{RC}	0	—	—	ns
Data hold time	t_{RH}	10	—	—	ns
Read pulsewidth	t_{RP}	400	—	—	ns
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

Note: Load on pin DB7 is CL = 100 pF.

MPU Write Timing



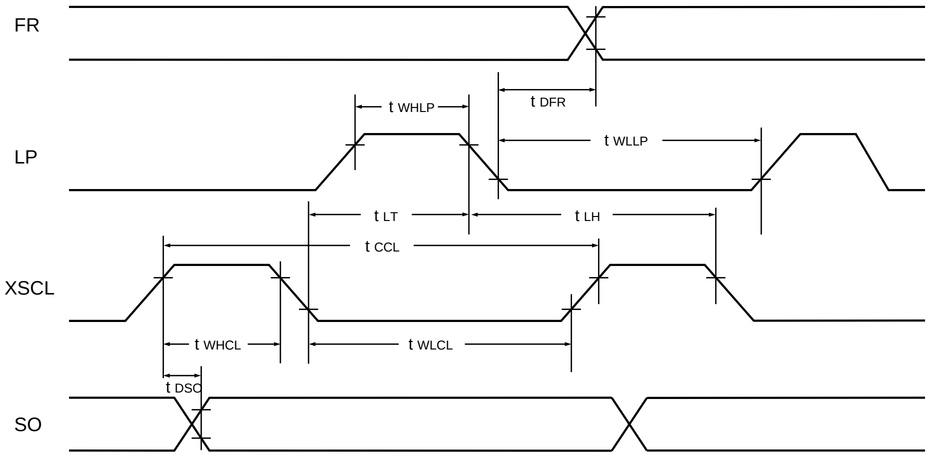
V_{DD} = 5 V, Ta = –20 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
A0 → $\overline{WR}$ setup time	t_{AW}	0	—	—	ns
$\overline{CS}$ → $\overline{WR}$ setup time	t_{CW}	0	—	—	ns
Data setup time	t_{DS}	120	—	—	ns
$\overline{WR}$ → A0 hold time	t_{WA}	20	—	—	ns
$\overline{WR}$ → $\overline{CS}$ hold time	t_{WC}	20	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
Write pulsewidth	t_{WP}	200	—	—	ns
Write cycle	t_{WCYC}	16/Φ	—	—	µs
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

V_{DD} = 3 V, Ta = –20 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
A0 → $\overline{WR}$ setup time	t_{AW}	0	—	—	ns
$\overline{CS}$ → $\overline{WR}$ setup time	t_{CW}	0	—	—	ns
Data setup time	t_{DS}	120	—	—	ns
$\overline{WR}$ → A0 hold time	t_{WA}	0	—	—	ns
$\overline{WR}$ → $\overline{CS}$ hold time	t_{WC}	0	—	—	ns
Data hold time	t_{DH}	100	—	—	ns
Write pulsewidth	t_{WP}	200	—	—	ns
Write cycle	t_{WCYC}	16/Φ	—	—	µs
Input fall time	t_f	—	—	50	ns
Input rise time	t_r	—	—	50	ns

X-driver Control Timing

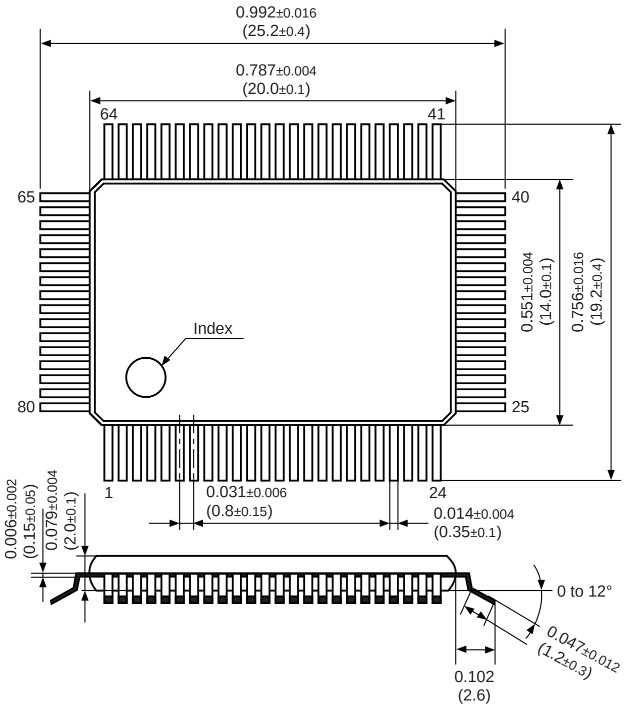


VDD = 2.5 to 5.5 V, Ta = –20 to 70°C.

Parameter	Symbol	Rating			Unit
		min	typ	max	
Shift clock cycle	t_{CCL}	3.3	10	—	µs
Shift clock “H” pulsewidth	t_{WHCL}	1.0	—	—	µs
Shift clock “L” pulsewidth	t_{WLCL}	1.0	—	—	µs
Delay time for XSCL → SO output	t_{DSO}	—	—	1	µs
Latch pulse “H” pulsewidth	t_{WHLP}	1.0	—	—	µs
Latch pulse “L” pulsewidth	t_{WLLP}	300	—	—	ns
Latch time	t_{LT}	500	—	—	ns
Latch hold time	t_{LH}	500	—	—	ns
Delay time for frame signal	t_{DFR}	—		500	ns

Note: Load capacitance C_L = 15 pF

Mechanical Specifications



OPERATION

Data Input/Output

New commands must not be written to the SED1210F if it is currently executing the last one, so the busy flag should be checked before commands are written.
If the busy flag is not going to be checked between writes of individual commands then the MPU must wait long enough to allow for command execution to complete. The maximum time taken by the SED1210F to execute a command is given by 16/Φ, where Φ is the system command clock frequency.

System Initialization

Figure 1 shows a flow chart of a possible SED1210F initialization sequence. Note that busy flag checks, and busy/wait loops have been omitted for the sake of brevity.

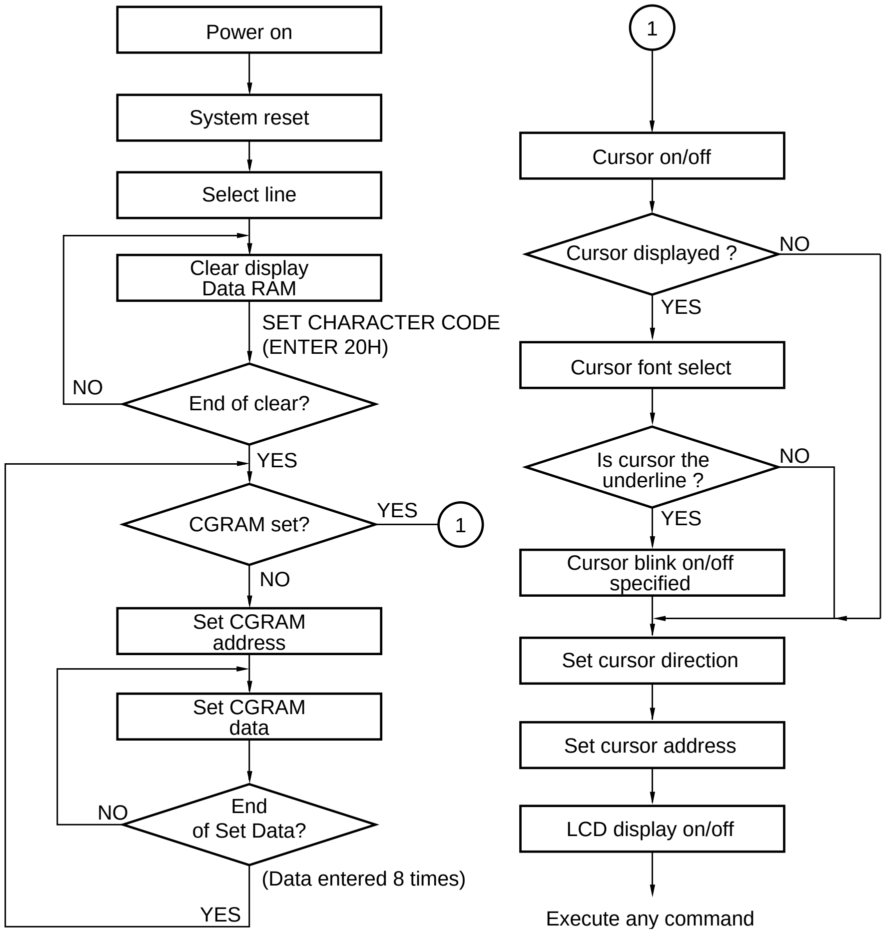


Figure 1. SED1210F Initialization

Loading CGRAM

The character generator RAM is loaded with a character bit pattern using a combination of one SET CGRAM ADDRESS command and eight SET CGRAM DATA commands. For example, to load the character shown in figure 2 into the area of CGRAM corresponding to character code 01H, the sequence shown below would be used.

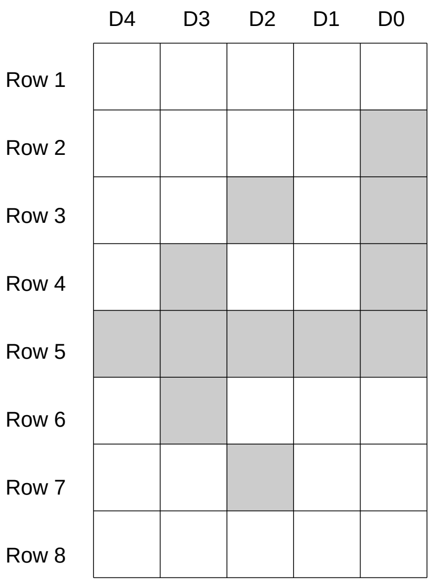


Figure 2. User Defined Characters

Step	A0	$\overline{WR}$	Data	Action
1	0	0	21H	Set address of CGRAM 01
2	0	0	40H	Data for Row 1
3	0	0	41H	Data for Row 2
4	0	0	45H	Data for Row 3
5	0	0	49H	Data for Row 4
6	0	0	5FH	Data for Row 5
7	0	0	48H	Data for Row 6
8	0	0	44H	Data for Row 7
9	0	0	40H	Data for Row 8

Notes:
1. These steps do not include any BUSY FLAG CHECK commands.
2. Row 8 may be used by the underline cursor.

SED1210

APPLICATION NOTES

Display Oscillator

The SED1210F has an internal oscillator to generate the timing signals required for the LCD display.
If the internal oscillator is used, connect the feedback resistor R_f as shown in figure 3. The feedback resistor leads must be kept as short as possible to reduce stray capacitance and the possibility of crosstalk between the oscillator and adjoining signals.

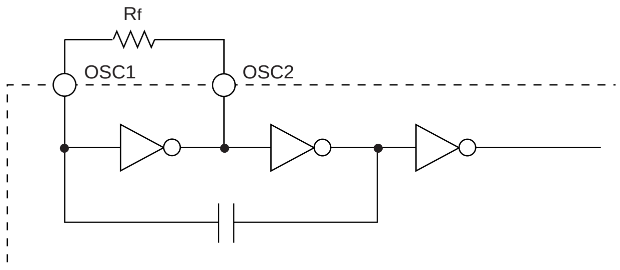


Figure 3. Using the Internal Oscillator

If an external clock is used, connect it to OSC1 as shown in figure 4.

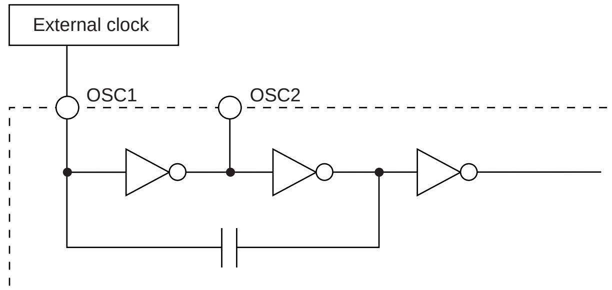


Figure 4. Using an External Clock

The relationship between the oscillator frequency and the LCD drive frame frequency is

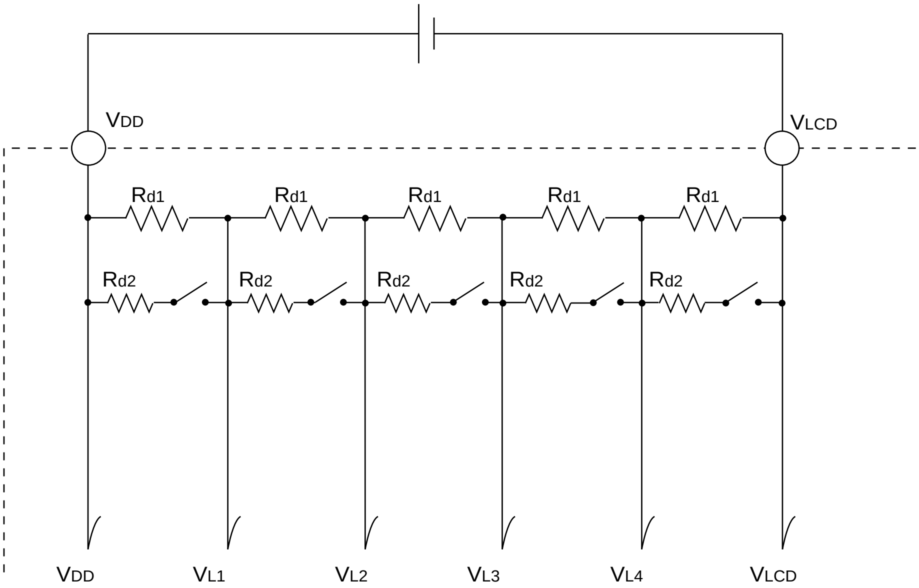
$f_{FR} = f_{OSC}/1600$
For example if f_{OSC} = 100 kHz, f_{FR} = 62.5 Hz

Command Clock (Φ)

When the system MPU issues a command to the SED1210F, the timing for the execution of the command is derived from Φ, the command clock. This would normally be the system MPU clock.
The maximum execution time for a command is given by 16/Φ. For example if Φ = 1 MHz, the maximum execution time for a command is 16 μs.

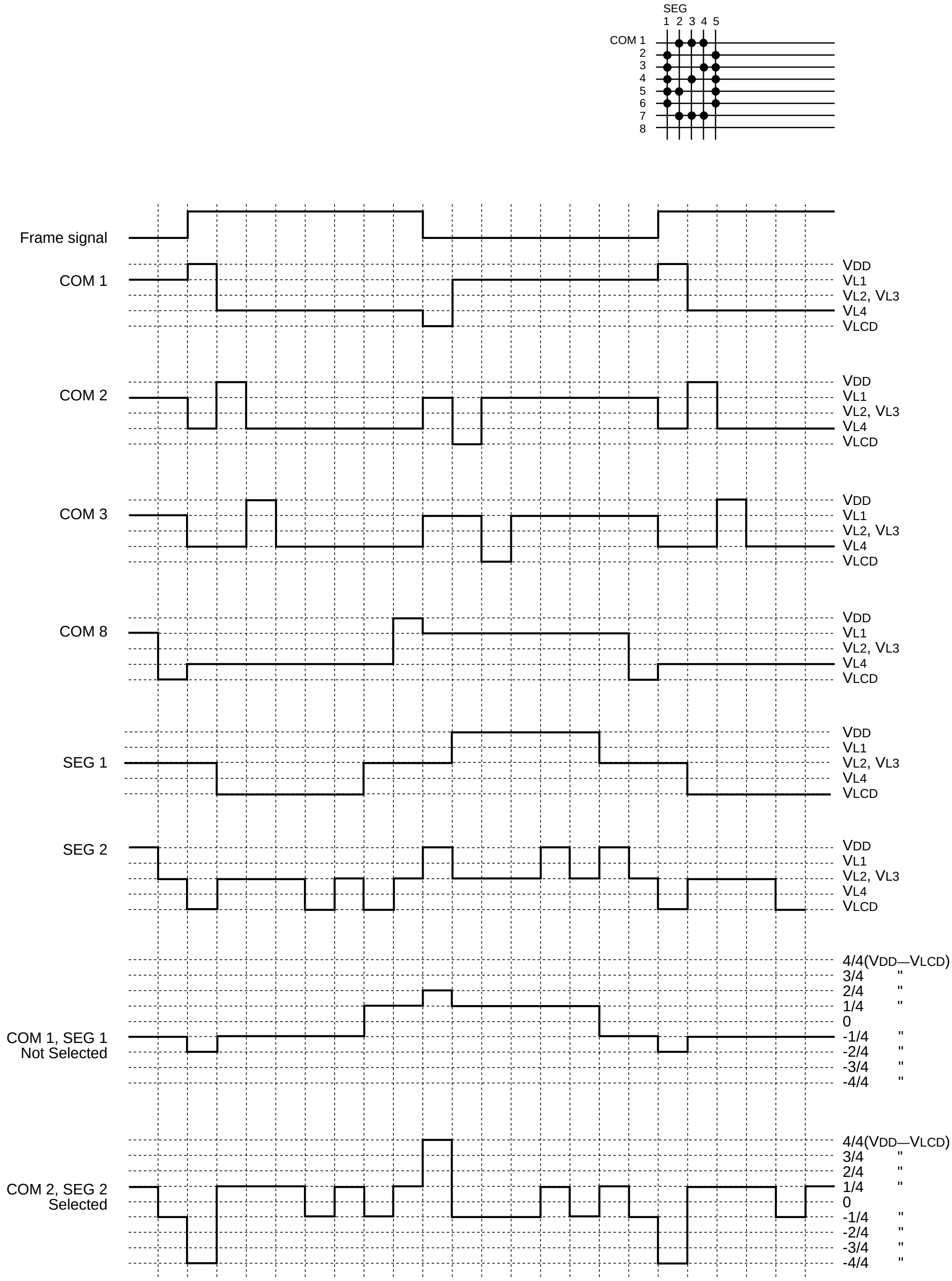
LCD Drive Waveforms

The SED1210F has an internal low source-impedance voltage-driver shown in the figure below. The switches are closed to switch the segment data.

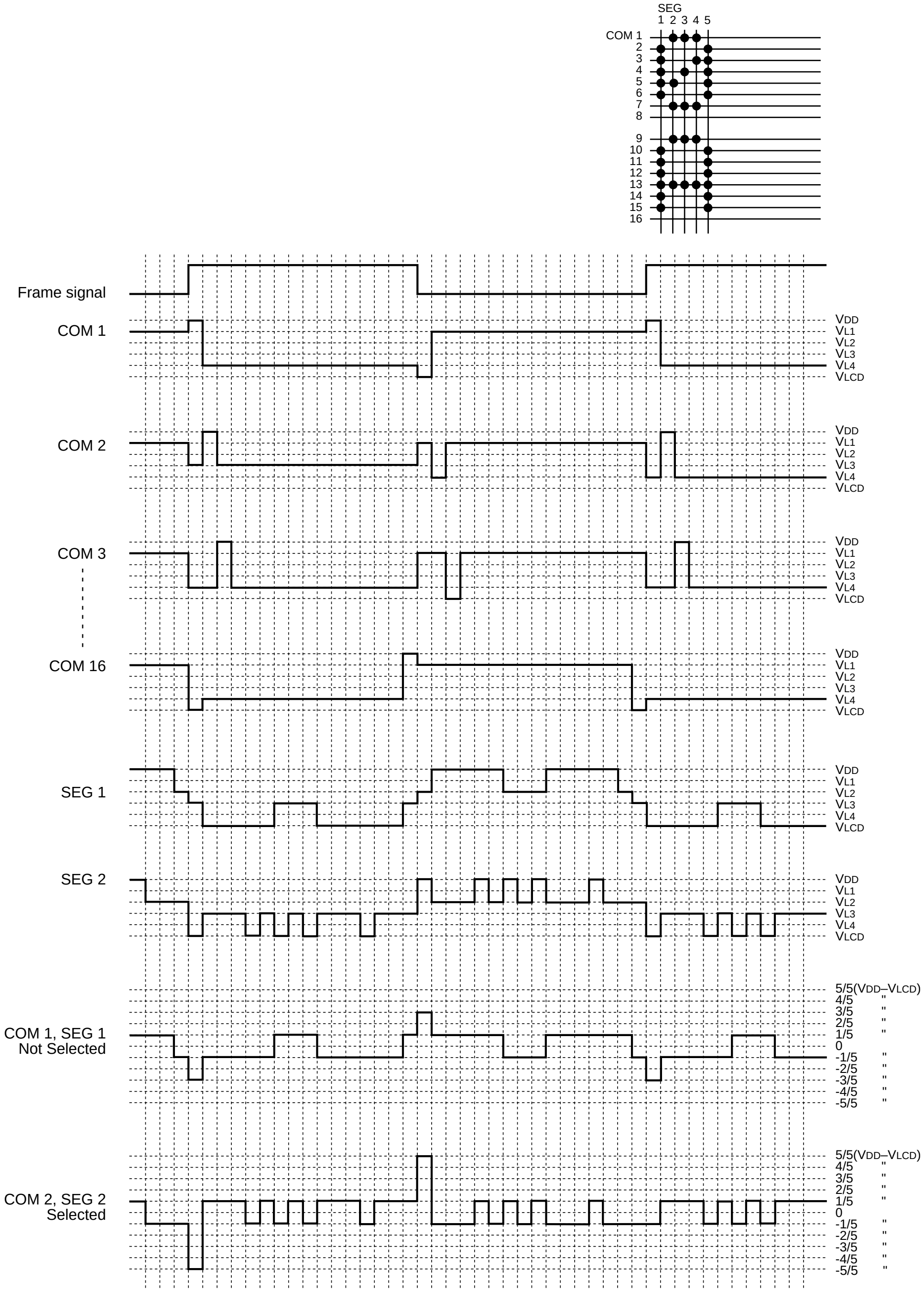


Examples of drive waveforms are shown below.

- LCD Drive Waveform – 1 Line Display (1/8 Duty Cycle)

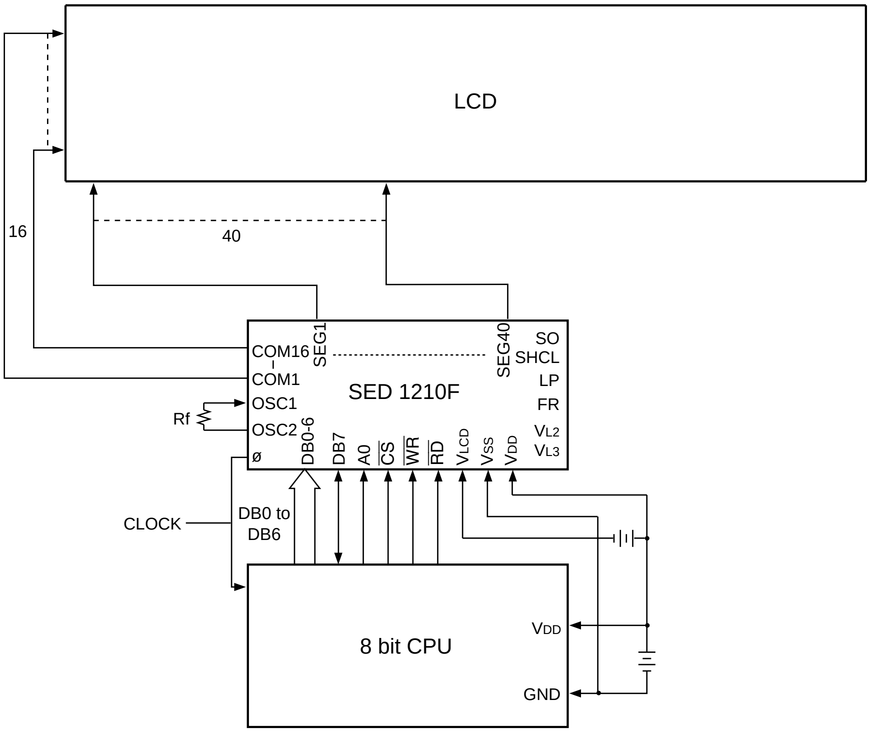


• LCD Drive Waveform – 2 Line Display (1/16 Duty Cycle)

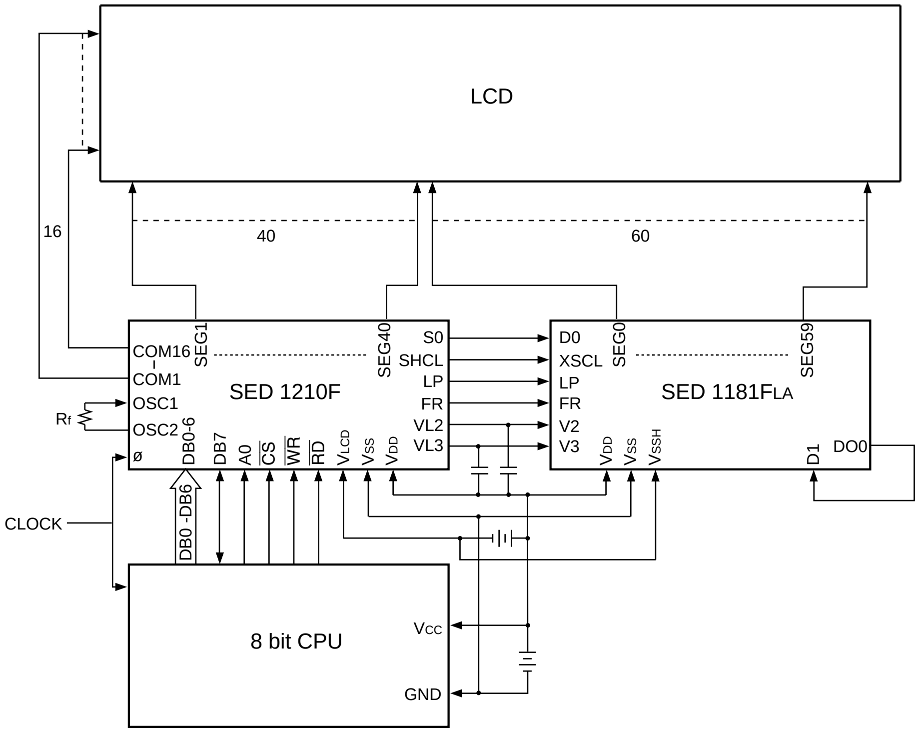


LCD Display Interface

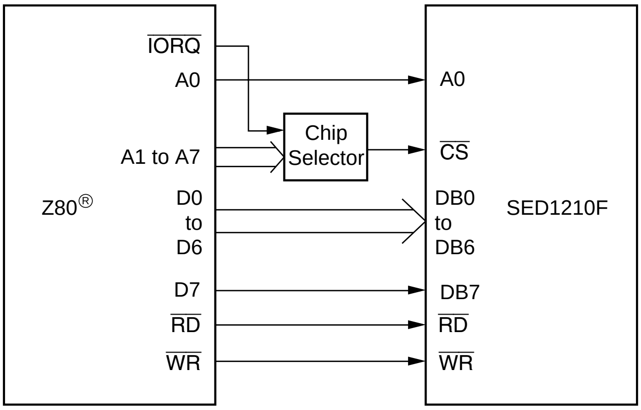
- 8 Characters/2 line



- 20 Characters/2 lines



- Interface with 8-bit CPU



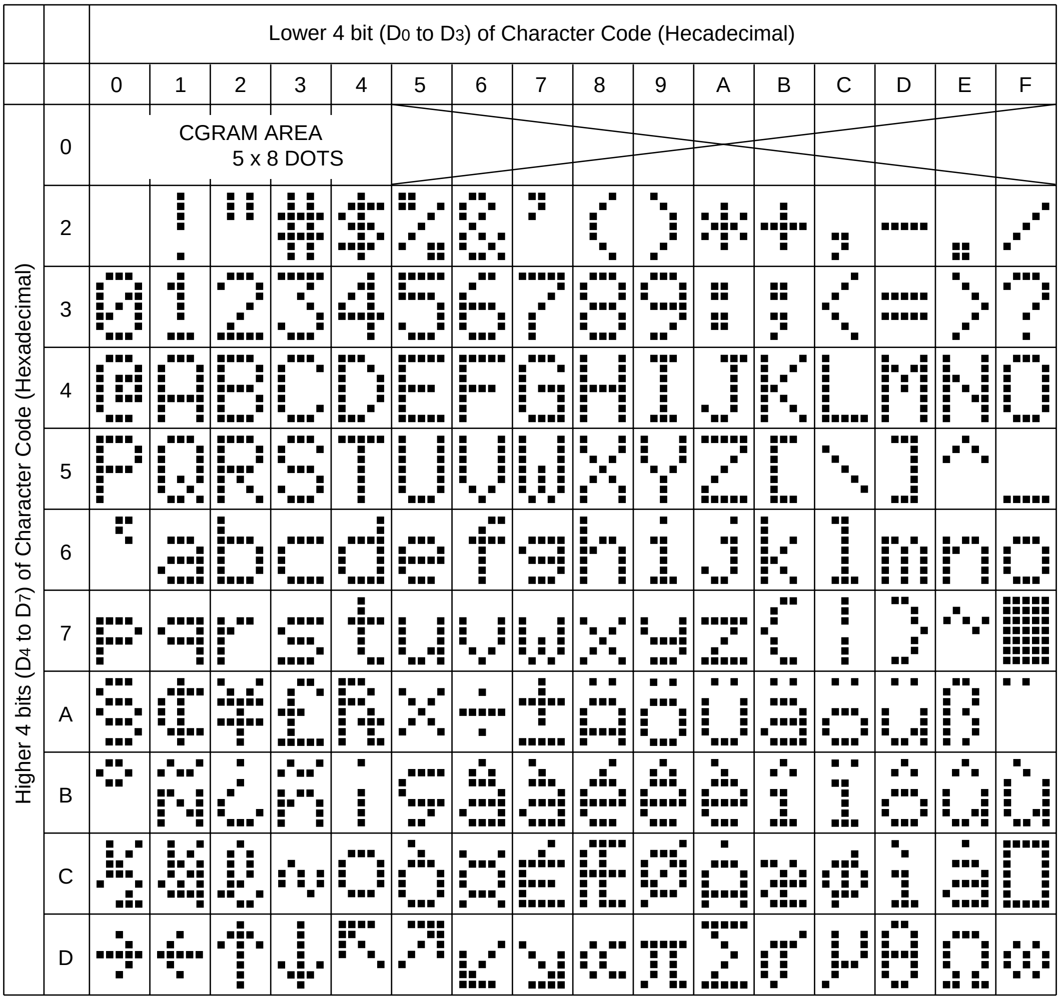
Z80 is a registered trademark of Zilog Corporation.

APPENDIX A: CHARACTER CODES AND FONTS

SED1210F0A

Higher 4 bits (D_4 to D_7) of Character Code (Hexadecimal)	Lower 4 bit (D_0 to D_3) of Character Code (Hecadecimal)															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CGRAM AREA 5 x 8 DOTS															
2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	¥	]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	→	←
A		｡	｢	｣	､	･	ｦ	ｧ	ｨ	ｩ	ｪ	ｫ	ｬ	ｭ	ｮ	ｯ
B	ｰ	ｱ	ｲ	ｳ	ｴ	ｵ	ｶ	ｷ	ｸ	ｹ	ｺ	ｻ	ｼ	ｽ	ｾ	ｿ
C	ﾀ	ﾁ	ﾂ	ﾃ	ﾄ	ﾅ	ﾆ	ﾇ	ﾈ	ﾉ	ﾊ	ﾋ	ﾌ	ﾍ	ﾎ	ﾏ
D	ﾐ	ﾑ	ﾒ	ﾓ	ﾔ	ﾕ	ﾖ	ﾗ	ﾘ	ﾙ	ﾚ	ﾛ	ﾜ	ﾝ	ﾞ	ﾟ

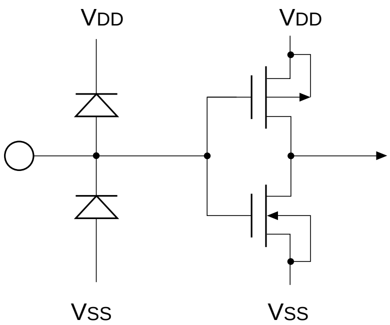
SED1210F0B


Lower 4 bit (D0 to D3) of Character Code (Hecadecimal)
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 bits (D4 to D7) of Character Code (Hexadecimal)
0 2 3 4 5 6 7 A B C D
CGRAM AREA
5 x 8 DOTS

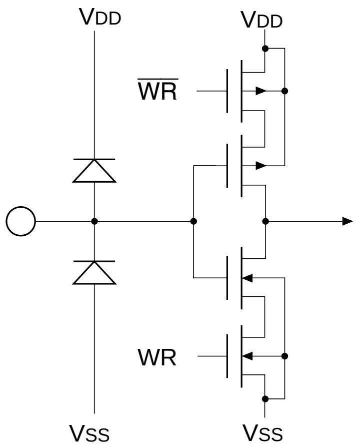
APPENDIX B: I/O TERMINAL STRUCTURE

I/O Terminal Structure Input

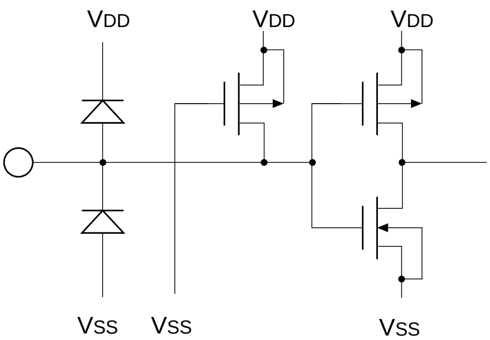
- Input Terminal (No pull-up)
  Terminals used: Φ, OSC1



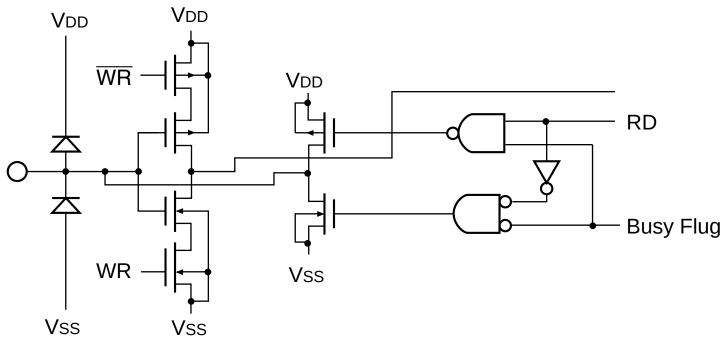
- Input Terminal (No pull-up)
  Terminals used: DB0 to DB6



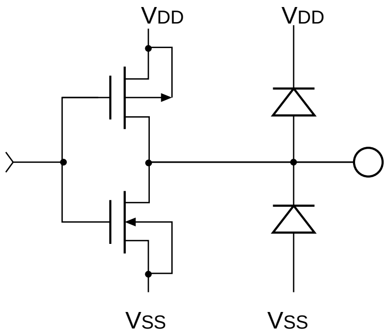
- Input Terminal (Pull-up)
  Terminals used: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0



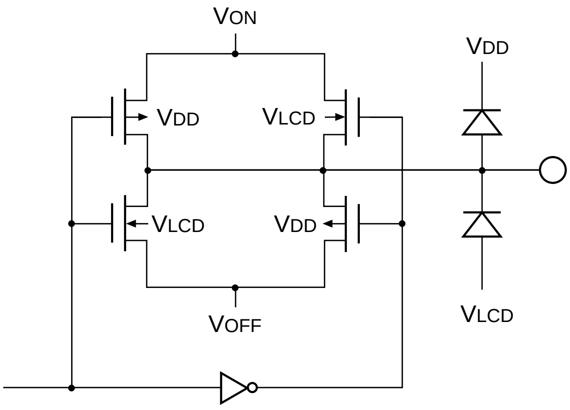
- I/O Terminal (No pull-up)
  Terminals used: DB7



- Output Terminal (No pull-up)
  Terminals used: OSC2, SO, SHCL, LP, FR



- LCD Drive Terminal (No pull-up)
  Terminals used: SEG1 to SEG40, COM1 to COM16



SED1220
LCD Controller/Drivers

Technical Manual

Contents

OVERVIEW

SED1220 is a dot matrix LCD controller/driver for character display. Using 4bits data, 8bits data or serial data being provided from the micro computer, it displays up to 36 characters, 4 user defined characters and up to 120 symbols.

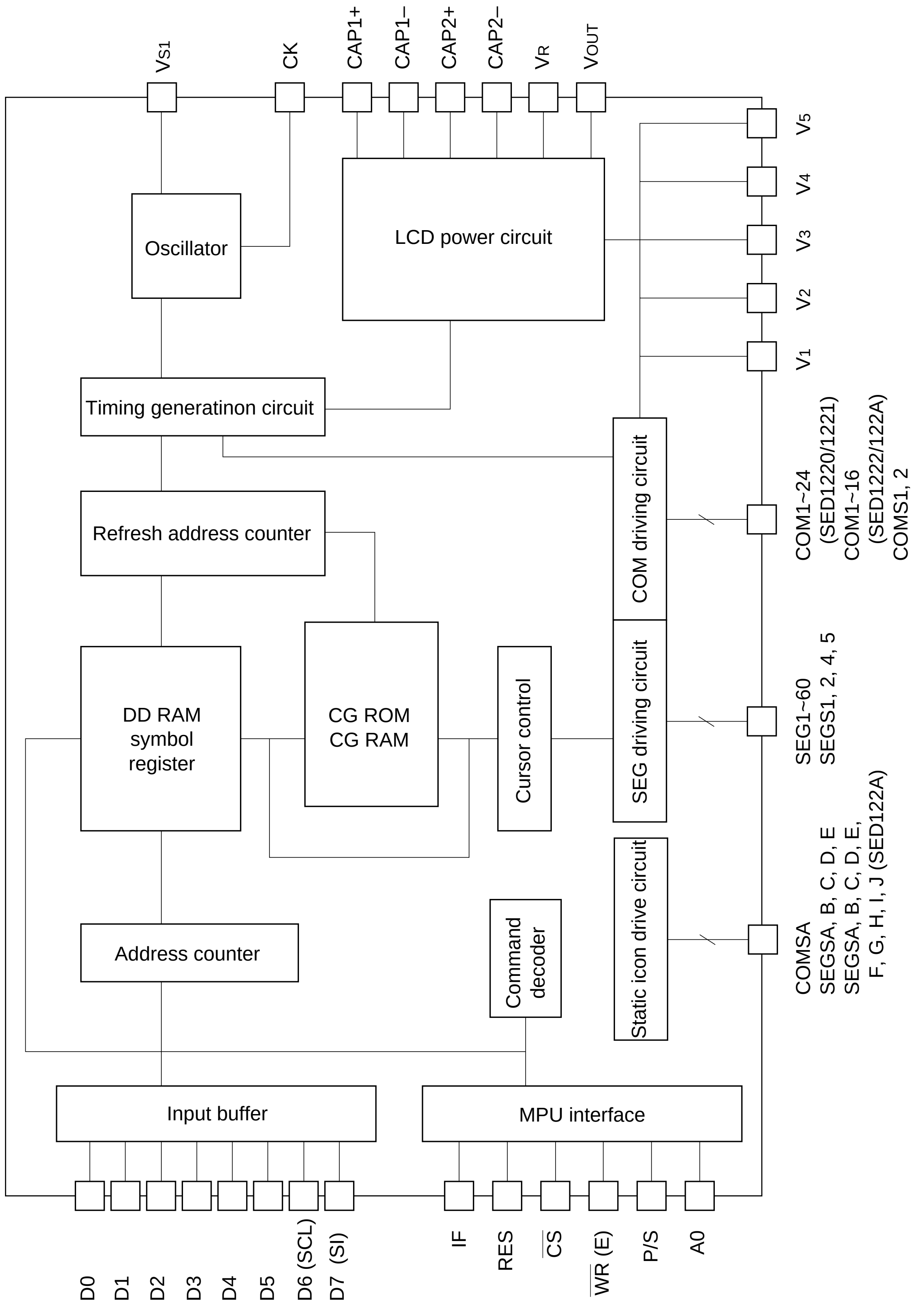
Up to 256 types of built-in character generator ROMs are prepared. Each character font is consisted of 5 × 8 dots. It also contains the RAM for displaying 4 user defined characters each font consisting of 5 × 8 dots. It is symbol register allows character display with high degree of freedom. This handy equipment can be operated with minimum power consumption with its low power consumption design, standby and sleeping mode.

FEATURES

- Built-in data display RAM – 36 characters + 4 user defined characters + 120 symbols.
- CG ROM (For up to 256 characters), CG RAM (for 4 characters) and symbol register (for 120 symbols).
- No. of display digit and lines
  < In normal mode >
  ① (12 digits + 4 segments for signal) × 3 lines + 120 symbols + 5 static symbols (SED1220D**)
  ② (12 digits + 4 segments for signal) × 2 lines + 120 symbols + 5 static symbols (SED1221D**)
  ③ 12 digits × 2 lines + 120 symbols + 5 static symbols (SED1222D**)
  ④ (12 digits + 4 segments for signal) × 2 lines + 120 symbols + 10 static symbols (SED122AD**)
  < In standby mode >
  ① 5 static symbols
  ② 5 static symbols
  ③ 5 static symbols
  ④ 10 static symbols
- Built-in CR oscillation circuit (C and R contained)
- Accepts external clock input
- High-speed MPU interface
  Affords interface with both 68/80 system MPUs
  Affords interface through 4 bits and 8 bits
- Affords serial interface
- Character font consists of 5 × 8 dots
- Duty ratio ① 1/26 (SED1220D**)
  ② 1/18 (SED1221D**, SED1222D**)
- Simplified command setting
- Built-in power circuit for driving liquid crystal
  Power amplifier circuit, power regulation circuit and voltage followers × 4
- Built-in electronic volume function
- Low power consumption
  80 µA max. (In normal operation, including operating current of the power supply).
  20 µA max. (In standby mode for displaying static icon).
  5 µA max. (In sleeping mode when display is turned off).
- Power supply
  V_{DD} - V_{SS} –2.4 V ~ –3.6 V
  V_{DD} - V_5 –4.0 V ~ – 6.0 V
- Temperature range for wide range operation
  Ta = –30 ~ 85°C
- CMOS process
- Shipping style
  Chip (Al pad product) SED1222D*A
  Chip (Au bump product) SED122∗D*B
  TCP SED122∗T**
- This unit does not employ radiation protection design

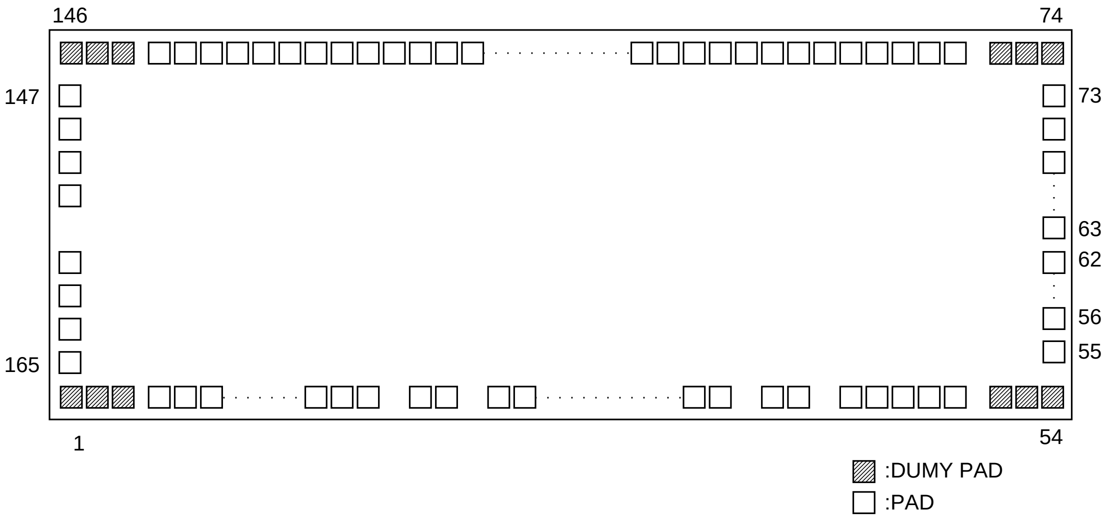
SED1220

BLOCK DIAGRAM



CHIP SPECIFICATION

SED1220D**/1221D**/122AD**



SED122∗D**
↑
Digits prepared for CGROM pattern changes

Chip size:	7.70 × 2.77 mm
Pad pitch:	100 µm (Minimum)
Chip thickness (for reference):	625 ± 25 µm (SED122∗D∗A) (SED122∗D∗B)

1) A1 pad specifications

Pad size on Y side:	75 µm × 135 µm
Pad size on X side:	135 µm × 75 µm

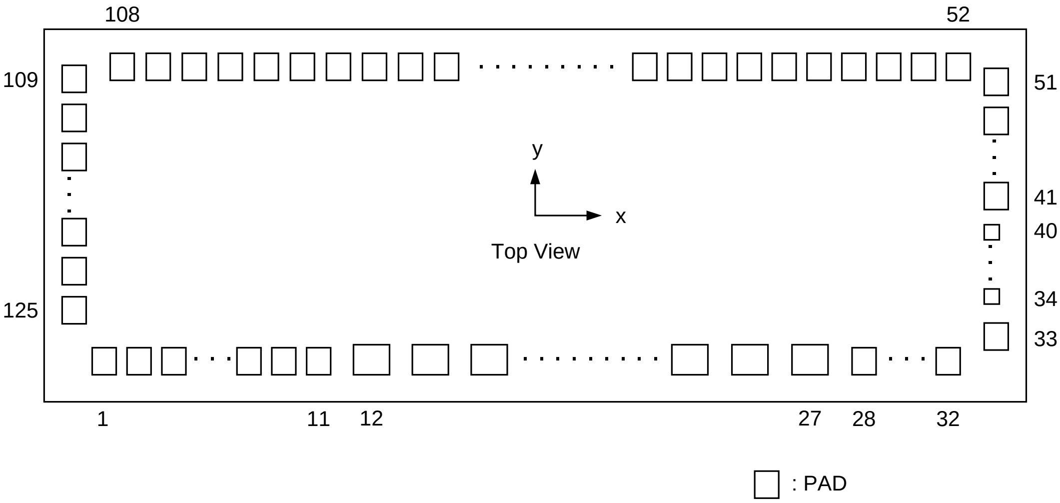
2) Au bump specifications

Bump size on Y side:	69 µm × 129 µm
Bump size on X side:	129 µm × 69 µm
Bump height (for reference)	22.5 µm ± 5.5 µm

<Fuse Pines>

1) Al pad. pad size 86 µm × 75 µm
2) Au bump
   Bump size 80 µm × 69 µm

SED1222D**



SED1222D**
↑
Digits prepared for CGROM pattern changes

Chip size: 7.70 × 2.77 mm
Pad pitch: 124 µm (Minimum)
Chip thickness (for reference): 625 ± 50 µm (SED1222D*A)

1) A1 pad specifications
Pad size on Y side: 90 µm × 96 µm
Pad size on X side: 96 µm × 90 µm (PAD. No. 1 ~ 11, 28 ~ 32, 52 ~ 108)
175 µm ×135 µm (PAD. No. 12 ~ 27)

<Fuse Pines>
1) Al pad. pad size 86 µm × 75 µm

<SED1220D**/1221D**>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	NC	–3700	–1204
2	NC	–3600	
3	NC	–3500	
4	A0	–3252	
5	$\overline{WR}$	–3132	
6	$\overline{CS}$	–3012	
7	D7	–2892	
8	D6	–2772	
9	D5	–2652	
10	D4	–2532	
11	D3	–2412	
12	D2	–2292	
13	D1	–2172	
14	D0	–2052	
15	V_{DD}	–1836	
16	V_{DD}	–1736	
17	V_{SS}	–1556	
18	V_{SS}	–1456	
19	V_5	–1276	
20	V_5	–1176	
21	V_4	–996	
22	V_4	–896	
23	V_3	–716	
24	V_3	–616	
25	V_2	–436	
26	V_2	–336	
27	V_1	–156	
28	V_1	–56	
29	V_0	124	
30	V_0	224	
31	V_R	404	
32	V_R	504	
33	V_{OUT}	684	
34	V_{OUT}	784	
35	CAP2–	964	
36	CAP2–	1064	
37	CAP2+	1244	
38	CAP2+	1344	
39	CAP1–	1524	
40	CAP1–	1624	
41	CAP1+	1804	
42	CAP1+	1904	
43	V_{SS}	2084	
44	V_{SS}	2184	
45	V_{DD}	2364	
46	V_{DD}	2464	
47	CK	2693	
48	VS1	2821	
49	P/S	2949	
50	I/F	3077	
51	RES	3205	
52	NC	3500	
53	NC	3600	
54	NC	3700	–1204

PAD		COORDINATES	
No.	Name	X	Y
55	V_{DD}	3670	–910
56	(FSA)	3603	–796
57	(FSB)		–696
58	(FSC)		–596
59	(FS0)		–496
60	(FS1)		–396
61	(FS2)		–296
62	(FS3)	3603	–196
63	V_{DD}	3670	–82
64	COMSA		61
65	COMS1		203
66	COM1		303
67	COM2		403
68	COM3		503
69	COM4		603
70	COM5		703
71	COM6		803
72	COM7		903
73	COM8	3670	1003
74	NC	3700	1204
75	NC	3600	
76	NC	3500	
77	SEGS1	3319	
78	SEGS2	3219	
79	SEG1	3119	
80	SEG2	3019	
81	SEG3	2919	
82	SEG4	2819	
83	SEG5	2719	
84	SEG6	2619	
85	SEG7	2519	
86	SEG8	2419	
87	SEG9	2319	
88	SEG10	2219	
89	SEG11	2119	
90	SEG12	2019	
91	SEG13	1919	
92	SEG14	1819	
93	SEG15	1719	
94	SEG16	1619	
95	SEG17	1519	
96	SEG18	1419	
97	SEG19	1319	
98	SEG20	1219	
99	SEG21	1119	
100	SEG22	1019	
101	SEG23	919	
102	SEG24	819	
103	SEG25	719	
104	SEG26	619	
105	SEG27	519	
106	SEG28	419	
107	SEG29	319	
108	SEG30	219	1204

(FS*) : Being fuse adjusting pins, maintain them on floating state.
CK pins : Should be V_{DD} when not being used.

SED1220

PAD		COORDINATES	
No.	**Name**	**X**	**Y**
109	SEG31	119	1204
110	SEG32	19	↑
111	SEG33	–81	
112	SEG34	–181	
113	SEG35	–281	
114	SEG36	–381	
115	SEG37	–481	
116	SEG38	–581	
117	SEG39	–681	
118	SEG40	–781	
119	SEG41	–881	
120	SEG42	–981	
121	SEG43	–1081	
122	SEG44	–1181	
123	SEG45	–1281	
124	SEG46	–1381	
125	SEG47	–1481	
126	SEG48	–1581	
127	SEG49	–1681	
128	SEG50	–1781	
129	SEG51	–1881	
130	SEG52	–1981	
131	SEG53	–2081	
132	SEG54	–2181	
133	SEG55	–2281	
134	SEG56	–2381	
135	SEG57	–2481	
136	SEG58	–2581	
137	SEG59	–2681	
138	SEG60	–2781	
139	SEGS4	–2881	
140	SEGS5	–2981	
141	COM24	–3081	
142	COM23	–3181	
143	COM22	–3281	
144	NC	–3500	
145	NC	–3600	↓
146	NC	–3700	1204
147	COM21	–3670	1000
148	COM20	↑	900
149	COM19		800
150	COM18		700
151	COM17		600
152	COM16		500
153	COM15		400
154	COM14		300
155	COM13		200
156	COM12		100
157	COM11		0
158	COM10		–100
159	COM9		–200
160	COMS2		–300
161	SEGSA		–433
162	SEGSB		–533
163	SEGSC		–633
164	SEGSD	↓	–733
165	SEGSE	–3670	–833

<SED1222D**>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	A0	–3312	–1228
2	$\overline{\text{WR}}$	–3180	↑
3	$\overline{\text{CS}}$	–3048	
4	D7	–2916	
5	D6	–2784	
6	D5	–2652	
7	D4	–2520	
8	D3	–2388	
9	D2	–2256	
10	D1	–2124	↓
11	D0	–1992	–1228
12	V_{DD}	–1786	–1204
13	V_{SS}	–1506	↑
14	V_5	–1226	
15	V_4	–946	
16	V_3	–666	
17	V_2	–386	
18	V_1	–106	
19	V_0	174	
20	V_R	454	
21	V_{OUT}	734	
22	CAP2–	1014	
23	CAP2+	1294	
24	CAP1–	1574	
25	CAP1+	1854	
26	V_{SS}	2134	↓
27	V_{DD}	2414	–1204
28	$\overline{\text{CK}}$	2692	–1228
29	VS1	2836	↑
30	P/S	2980	
31	I/F	3124	↓
32	RES	3268	–1228
33	V_{DD}	3694	–919
34	(FSA)	3603	–796
35	(FSB)	↑	–696
36	(FSC)		–596
37	(FS0)		–496
38	(FS1)		–396
39	(FS2)	↓	–296
40	(FS3)	3603	–196
41	V_{DD}	3694	–73
42	COMSA	↑	63
43	COMS1		199
44	COM1		323
45	COM2		447
46	COM3		571
47	COM4		695
48	COM5		819
49	COM6		943
50	COM7	↓	1067
51	COM8	3694	1191
52	SEG1	3472	1228
53	SEG2	3348	1228
54	SEG3	3224	1228

PAD		COORDINATES	
No.	Name	X	Y
55	SEG4	3100	1228
56	SEG5	2976	↑
57	SEG6	2852	
58	SEG7	2728	
59	SEG8	2604	
60	SEG9	2480	
61	SEG10	2356	
62	SEG11	2232	
63	SEG12	2108	
64	SEG13	1984	
65	SEG14	1860	
66	SEG15	1736	
67	SEG16	1612	
68	SEG17	1488	
69	SEG18	1364	
70	SEG19	1240	
71	SEG20	1116	
72	SEG21	992	
73	SEG22	868	
74	SEG23	744	
75	SEG24	620	
76	SEG25	496	
77	SEG26	372	
78	SEG27	248	
79	SEG28	124	
80	SEG29	0	
81	SEG30	–124	
82	SEG31	–248	
83	SEG32	–372	
84	SEG33	–496	
85	SEG34	–620	
86	SEG35	–744	
87	SEG36	–868	
88	SEG37	–992	
89	SEG38	–1116	
90	SEG39	–1240	
91	SEG40	–1364	
92	SEG41	–1488	
93	SEG42	–1612	
94	SEG43	–1736	
95	SEG44	–1860	
96	SEG45	–1984	
97	SEG46	–2108	
98	SEG47	–2232	
99	SEG48	–2356	
100	SEG49	–2480	
101	SEG50	–2604	
102	SEG51	–2728	
103	SEG52	–2852	
104	SEG53	–2976	
105	SEG54	–3100	
106	SEG55	–3224	
107	SEG56	–3348	↓
108	SEG57	–3472	1228

(FS*) : Being fuse adjusting pins, maintain them on floating state.
CK pins : Should be V_{DD} when not being used.

SED1220

PAD		COORDINATES	
No.	Name	X	Y
109	SEG58	–3694	1191
110	SEG59	↑	1067
111	SEG60		943
112	COM16		819
113	COM15		695
114	COM14		571
115	COM13		447
116	COM12		323
117	COM11		119
118	COM10		75
119	COM9		–49
120	COMS2		–173
121	SEGSA		–335
122	SEGSB		–459
123	SEGSC		–583
124	SEGSD	↓	–707
125	SEGSE	–3694	–831

<SED122AD$_{**}$>

Unit: µm

PAD		COORDINATES		PAD		COORDINATES	
No.	Name	X	Y	No.	Name	X	Y
1	NC	–3700	–1204	55	V_{DD}	3670	–910
2	NC	–3600		56	(FSA)	3603	–796
3	NC	–3500		57	(FSB)		–696
4	A0	–3252		58	(FSC)		–596
5	$\overline{WR}$	–3132		59	(FS0)		–496
6	CS	–3012		60	(FS1)		–396
7	D7	–2892		61	(FS2)		–296
8	D6	–2772		62	(FS3)	3603	–196
9	D5	–2652		63	V_{DD}	3670	–82
10	D4	–2532		64	COMSA		61
11	D3	–2412		65	COMS1		203
12	D2	–2292		66	COM1		303
13	D1	–2172		67	COM2		403
14	D0	–2052		68	COM3		503
15	V_{DD}	–1836		69	COM4		603
16	V_{DD}	–1736		70	COM5		703
17	V_{SS}	–1556		71	COM6		803
18	V_{SS}	–1456		72	COM7		903
19	V_5	–1276		73	COM8	3670	1003
20	V_5	–1176		74	NC	3700	1204
21	V_4	–996		75	NC	3600	
22	V_4	–896		76	NC	3500	
23	V_3	–716		77	SEGS1	3319	
24	V_3	–616		78	SEGS2	3219	
25	V_2	–436		79	SEG1	3119	
26	V_2	–336		80	SEG2	3019	
27	V_1	–156		81	SEG3	2919	
28	V_1	–56		82	SEG4	2819	
29	V_0	124		83	SEG5	2719	
30	V_0	224		84	SEG6	2619	
31	V_R	404		85	SEG7	2519	
32	V_R	504		86	SEG8	2419	
33	V_{OUT}	684		87	SEG9	2319	
34	V_{OUT}	784		88	SEG10	2219	
35	CAP2–	964		89	SEG11	2119	
36	CAP2–	1064		90	SEG12	2019	
37	CAP2+	1244		91	SEG13	1919	
38	CAP2+	1344		92	SEG14	1819	
39	CAP1–	1524		93	SEG15	1719	
40	CAP1–	1624		94	SEG16	1619	
41	CAP1+	1804		95	SEG17	1519	
42	CAP1+	1904		96	SEG18	1419	
43	V_{SS}	2084		97	SEG19	1319	
44	V_{SS}	2184		98	SEG20	1219	
45	V_{DD}	2364		99	SEG21	1119	
46	V_{DD}	2464		100	SEG22	1019	
47	CK	2693		101	SEG23	919	
48	VS1	2821		102	SEG24	819	
49	P/S	2949		103	SEG25	719	
50	I/F	3077		104	SEG26	619	
51	RES	3205		105	SEG27	519	
52	NC	3500		106	SEG28	419	
53	NC	3600		107	SEG29	319	
54	NC	3700	–1204	108	SEG30	219	1204

(FS*) : This is a fuse adjusting terminal. Set it to floating state.
CK pins : Set it to V_{DD} when not used.

PAD		COORDINATES	
No.	Name	X	Y
109	SEG31	119	1204
110	SEG32	19	↑
111	SEG33	–81	
112	SEG34	–181	
113	SEG35	–281	
114	SEG36	–381	
115	SEG37	–481	
116	SEG38	–581	
117	SEG39	–681	
118	SEG40	–781	
119	SEG41	–881	
120	SEG42	–981	
121	SEG43	–1081	
122	SEG44	–1181	
123	SEG45	–1281	
124	SEG46	–1381	
125	SEG47	–1481	
126	SEG48	–1581	
127	SEG49	–1681	
128	SEG50	–1781	
129	SEG51	–1881	
130	SEG52	–1981	
131	SEG53	–2081	
132	SEG54	–2181	
133	SEG55	–2281	
134	SEG56	–2381	
135	SEG57	–2481	
136	SEG58	–2581	
137	SEG59	–2681	
138	SEG60	–2781	
139	SEGS4	–2881	
140	SEGS5	–2981	
141	NC	–3081	
142	NC	–3181	
143	NC	–3281	
144	NC	–3500	
145	NC	–3600	↓
146	NC	–3700	1204
147	COM16	–3670	1000
148	COM15	↑	900
149	COM14		800
150	COM13		700
151	COM12		600
152	COM11		500
153	COM10		400
154	COM9		300
155	COMS2		200
156	SEGSA		67
157	SEGSB		–33
158	SEGSC		–133
159	SEGSD		–233
160	SEGSE		–333
161	SEGSF		–433
162	SEGSG		–533
163	SEGSH		–633
164	SEGSI	↓	–733
165	SEGSJ	–3670	–833

DESCRIPTION OF PINS

Power Pins

Pin name	I/O	Description	Q'ty
V_{DD}	Power supply	Connected to logic supply. Common with MPU power terminal V_{CC}.	1
V_{SS}	Power supply	0V power terminal connected to system ground.	1
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined in the liquid crystal cell is resistance-divided or impedance-converted by operational amplifier, and the resultant voltage is applied. The potential is determined on the basis of V_{DD} and the following equation must be respected. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to pins V1 to V4 by built-in power circuit: V_1 = 1/5 V_5 (1/4 V_5) V_2 = 2/5 V_5 (2/4 V_5) V_3 = 3/5 V_5 (3/4 V_5) V_4 = 4/5 V_5 (4/4 V_5) voltage ratings in ( ) are for optinal choices.	6
V_{S1}	O	Power supply voltage output pin for oscillating circuit, and DC/DC source. Don't connect this pin to an external load.	1

LCD Power Circuit Pins

Pin name	I/O	Description	Q'ty
CAP1+	O	Capacitor positive side connecting pin for boosting. This pin connects the capacitor with pin CAP1–.	1
CAP1–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP+.	1
CAP2+	O	Capacitor positive side connecting pin for boosting. This pin connects a capacitor with pin CAP2–.	1
CAP2–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP2+.	1
V_{OUT}	O	Output pin for boosting. This pin connects a smoothing capacitor with V_{DD} pin.	1
V_R	I	Voltage regulating pin. This pin gives a voltage between V_{DD} and V_5 by resistance-division of voltage.	1

Pins for System Bus Connection

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Q'ty</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 ~ D0</td><td>I</td><td>8-bit input data bus. These pins are connected to a 8-bit or 16-bit standard MPU data bus.
When P/S = "Low", the D7 and D6 pins are operated as a serial data input and a serial clock input respectively.
<table>
<tr><td>P/S</td><td>RES</td><td>I/F</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
<tr><td>"L"</td><td>—</td><td>—</td><td>SI</td><td>SCL</td><td>—</td><td>—</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>—</td></tr>
<tr><td>"H"</td><td>"H"</td><td>"H"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>E</td></tr>
<tr><td>"H"</td><td>"L"</td><td>"H"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
<tr><td>"H"</td><td>"L"</td><td>"L"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
</table>
RES: Indicates the active potential.
OPEN: Though "OPEN" is available, fixing the potential is recommended for noise-withstnading characteristical reason.
—: Indicates that it can be set at either "H" or "L", but fixing the potential is required.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, this pin connects the least significant bit of the MPU address bus and identifies a data command.
0 : Indicates that D0 to D7 are a command.
1 : Indicates that D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>In case of a 68 series MPU, initialization can be performed by changing RES ↓. In case of an 80 series MPU, initialization can be performed by changing ↑.
A reset operation is performed by edge sensing of the RES signal.
An interface type for the 68/80 series MPU is selected by input level after initialization.
"L" : 68 series MPU interface
"H" : 80 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal. Usually, this pin inputs the signal obtained by decoding an address bus signal. At the "Low" level, this pin is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$

(E)</td><td>I</td><td><When connecting an 80 series MPU>
Active "Low". This pin connects the $\overline{WR}$ signal of the 80 series MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ signal.
<When connecting a 68 series MPU>
Active "High". This pin becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin switches between serial data input and parallel data input.
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Serial Clock</td></tr>
<tr><td>"High"</td><td>$\overline{CS}$</td><td>A0</td><td>D0~D7</td><td>–</td></tr>
<tr><td>"Low"</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>Interface data length select pin for parallel data input.
"High": 8-bit parallel input
"Low": 4-bit parallel input
When P/S = "Low", connect this pin to V_{DD} or V_{SS}.</td><td>1</td></tr>
<tr><td>CK</td><td>I</td><td>External input terminal
It must be fixed to "High" when the internal oscillation circuit is used.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

Dynamic drive terminal (SED1220D**/1221D**/122AD**)

Pin name	I/O	Description	Q'ty
COM1~ COM24	O	Common signal output pin (for characters)	24
COMS1, CMOS2	O	Common signal output pin (except for characters) CMOS1, CMOS2: Common output for symbol display	2
SEG1~ SEG60	O	Segment signal output pin (for characters)	60
SEGS1, 2 4, 5	O	Segment signal output pin (except for characters) SEGS1, SEGS2: Segment output for signal output	4

Dynamic drive terminal (SED1222D**)

Pin name	I/O	Description	Q'ty
COM1~ COM16	O	Common signal output pin (for characters)	16
COMS1, CMOS2	O	Common signal output pin (except for characters) CMOS1, CMOS2: Common output for symbol display	2
SEG1~ SEG60	O	Segment signal output pin (for characters)	60

Static drive terminal

Pin name	I/O	Description	Q'ty
COMSA	O	Common signal output pin (for icon)	1
SEGSA, B C, D, E F, G, H, I, J	O	Segment signal output pin (for icon) SEGSF, G, H, I, J (only SED122A)	5 to 10

Note: For the electrode of liquid crystal display panel to be connected to the static drive terminal, we recommend you to use a pattern in which it is separated from the electrode connected to the dynamic drive terminal. When this pattern is too close to the other electrode, both the liquid crystal display and electrode will be deteriorated.

FUNCTIONAL DESCRIPTION

MPU Interface

Selection of interface type

In the SED1220 Series, data transfer is performed through a 8-bit or 4-bit data bus or a serial data input (SI). By selecting "High" or "Low" as P/S pin polarity, a parallel data input or a serial data input can be selected as shown in Table 1.

Table 1

P/S	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0~D7
"High"	Parallel Input	$\overline{CS}$	A0	$\overline{WR}$	—	—	D0~D7
"Low"	Serial Input	$\overline{CS}$	A0	H, L	SI	SCL	—

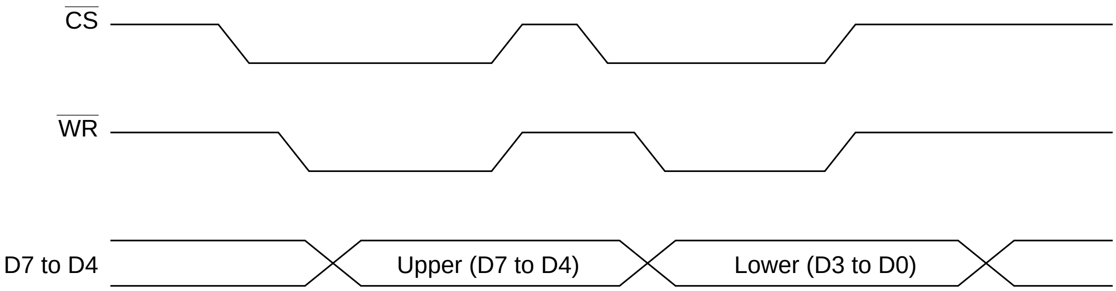
Parallel Input
In the SED1220 Series, when parallel input is selected (P/S = "High"), it can be directly connected to the 80 series MPU bus or 68 series MPU bus, as shown in Table 2, if either "High" or "Low" is selected as RES pin polarity after a reset input, because the RES pin has an MPU select function.
Selection between 8 bits and 4 bits is performed by command.

Table 2

RES input polarity	Type	A0	$\overline{WR}$	$\overline{CS}$	D0~D7
↓ active	68 series	A0	E	$\overline{CS}$	D0~D7
↑ active	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0~D7

Interface with 4-bit MPU interface

When data transfer is performed by 4-bit interface (IF = 0), an 8-bit command, data and address are divided into two parts.



Note: When performing writing in succession, reverse a time exceeding the system cycle time (t_{cyc}) and then perform writing.

Serial interface (P/S = "Low")

The serial interface consists of a 8-bit shift register and a 3-bit counter and acceptance of an SI input or SCL input is enabled in the ship selected status (CS = "Low").
When no chip is selected, the shift register and counter are reset to the initial status.
Serial data is input in the order of D7, D6 .... D0 from the serial data input pin (SI) at the rise of Serial Clock (SCL).
At the rising edge of the 8th serial clock, the serial data is converted into 8-bit parallel data and this data is processed.
The A0 input is used to identify whether the serial data input (SI) is display data or a command. That is, when A0 = "High", it is regarded as display data. When A0 = "Low", it is regarded as a command.
The A0 input is read in and identified at the rise of the 8 x n-th clock of Serial Clock (SCL) after chip selection.
Fig. 1 shows a timing chart of the serial interface.
Regarding the SCL signal, special care must be exercised about terminal reflection and external noise due to a wire length.
We recommend the user to perform an operation check with a real machine.
We also recommend the user to periodically refresh the write status of each command to prevent a malfunction due to noise.

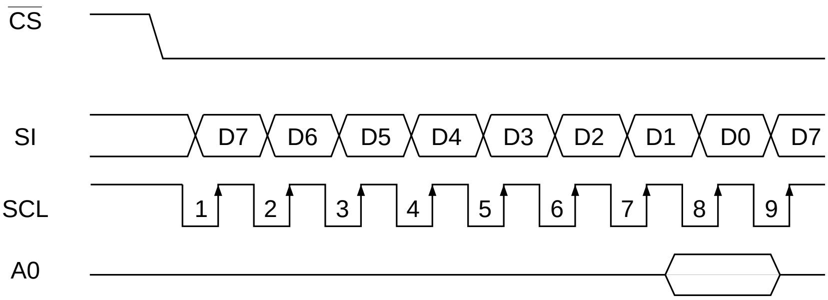


Fig. 1

Identification of data bus signals

The SED1220 series identifies data bus signals, as shown in Table 3, by combinations of A0 and $\overline{WR}$ (E).

Table 3

Common	68 series	80 series	Function
A0	E	$\overline{WR}$	
1	1	0	Writing to RAM and symbol register
0	1	0	Writing to internal register (command)

Chip select

The SED1220 series has a chip select pin ($\overline{CS}$). Only when $\overline{CS}$ = “Low”, MPU interfacing is enabled.
In any status other than Chip Select, D0 to D7 and A0, $\overline{WR}$, SI and SCL inputs are invalidated. When a serial input interface is selected, the shift register and counter are reset.

However, the Reset signal is input regardless of the $\overline{CS}$ status.

Power Circuit

This is a low-power-consumption power circuit that generates a voltage required for liquid crystal drive.
The power circuit consists of a boosting circuit, voltage regulating circuit and voltage follower.

The power circuit incorporated in the SED1220 Series is set for a small-scale liquid crystal panel, so that its display quality may be greatly deteriorated if it is used for a liquid crystal panel with a large display capacity.
In this case, an external power supply must be used.

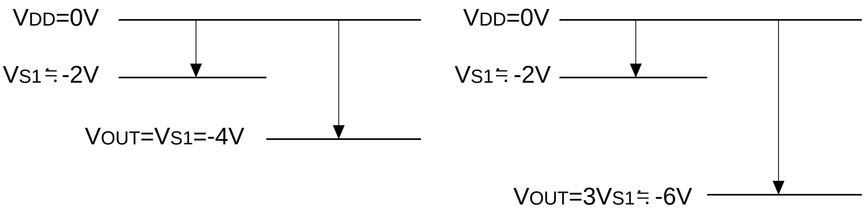
A power circuit function can be selected by power control command. With this, an external power supply and a part of the internal power supply can be used together.

	Amplifying circuit	Voltage regulating circuit	Voltage follower	External voltage input	Amplifying system pin
	○	○	○	—	Per specification
Note 1	×	○	○	V_{OUT}	OPEN
Note 2	×	×	○	$V_5 = V_{OUT}$	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

Note 1: When the boosting circuit is turned off, make boosting system pins (CAP1+, CAP1-, CAP2+, CAP2-) open and give a liquid crystal drive voltage to the V_{OUT} pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, make the boosting system pins open, connect between the V_5 pin and V_{OUT} pin, and give a liquid crystal drive voltage from the outside.
Note 3: When all the internal power supplies are turned off, supply liquid crystal drive voltages V_1, V_2, V_3, V_4 and V_5 from the outside, and make the CAP1+, CAP1-, CAP2+, CAP2- and V_{OUT} pins open.

Voltage Tripler Circuit

If capacitors are connected between CAP+1 – CAP–1 and CAP2+,CAP2– and V_{SS} V_{OUT}, V_{DD}– V_{SS} potential is negatively tripled and generated at V_{OUT} terminal. When the voltage is boosted double, open CAP2+ and connect CAP2– to V_{OUT} terminal.
At this time, the oscillating circuit must be operating since the amplifying circuit utilize the signal from the oscillation output.



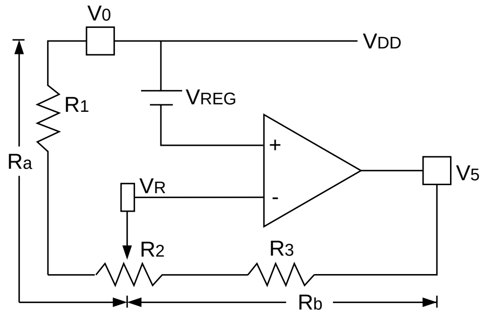
Potential relationship of amplified voltage

Voltage regulating circuit

Amplified voltage generated at V_{OUT} outputs liquid crystal drive voltage V_5 through the voltage regulation circuit.V_5 voltage can be obtained from the expression ① below by adjusting the resistors Ra and Rb within the range of $V_5 < V_{OUT}$.calculated by the following formula:

$$V_5 = \left(1 + \frac{R_b}{R_a}\right) \cdot V_{REG} \quad \text{①}$$

Where, V_{REG} is the constant power supply within IC. V_{REG} is maintained constantly at $V_{REG} \fallingdotseq 2.0V$.
Voltage regulation of V_5 output is done by connecting to a variable register between V_R, V_{DD} and V_5. It is recommended to combine fixed registers R1 and R3 with variable resistor R2 for fine adjustment of V_5 voltage.



R1 = 400KΩ
R2 = 200KΩ
R3 = 600KΩ

[Sample setting on R1, R2 and R3]

- R1 + R2 + R3 = 1.2 M ohm (decided from the current value I_{05} passed between V_{DD} – V_5. Where, $I_{05} \leq 5\ \mu A$ is supposed).
- Variable voltage range provided by R2 is from –4V to –6V (to be decided considering charecteristics of the liquid crystal).
- Since V_{REG} = 2.0V, if the electronic volume register is set at (0, 0, 0, 0, 0), followings are derived from above conditions and expression ① :

The voltage regulation circuit outputs V_{REG} with the temperature gradient of approximately –0.04%/°C.
Since V_R terminal has high input impedance, anti-noise measures must be considered including use of shortened wiring distance and shield wire.

● Voltage Regulation Circuit Using Electronic Volume Function

The electronic volume function allows to control the liquid crystal drive voltage V_5 with the commands and thus to adjust density of the liquid crystal display. Liquid crystal drive voltage V_5 can have one of 32 voltage values if 5-bit data is set to the electronic volume register.

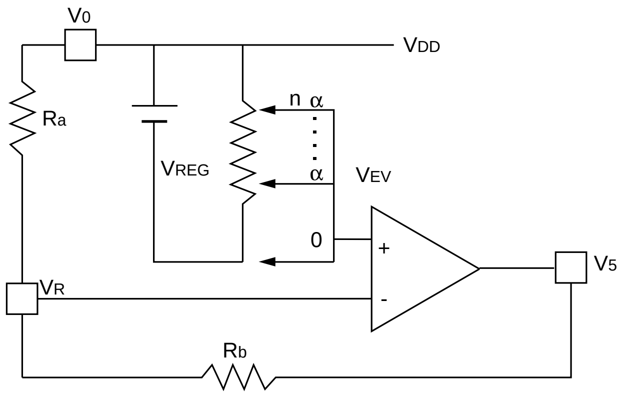
When using the electronic volume function, you need to turn the voltage regulation circuit on using the supply control command.

[Sample constants setting when electronic volume function is used]

$$V_5 = \left(1 + \frac{R_b}{R_a}\right) \cdot V_{EV} \quad \text{......} ②$$

Where $V_{EV} = V_{REG} - \alpha$

$\alpha = V_{REG} / 150$



No.	Electronic volume register	a	V_5
0	(0, 0, 0, 0, 0)	0	Large
1	(0, 0, 0, 0, 1)	1α	•
2	(0, 0, 0, 1, 0)	2α	•
3	(0, 0, 0, 1, 1)	3α	•
•	•	•	•
•	•	•	•
30	(1, 1, 1, 1, 0)	(n-1)α	•
31	(1, 1, 1, 1, 1)	nα	Small

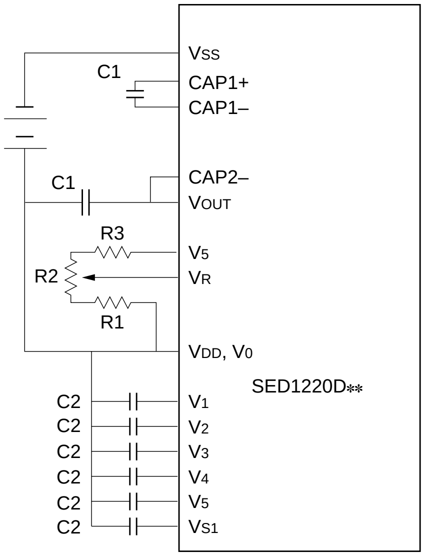
When the electronic volume function is not used, select (0, 0, 0, 0, 0) for the electronic volume register.

Liquid crystal voltage generating circuit

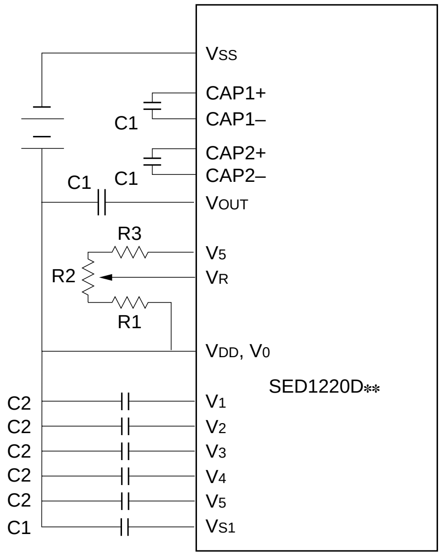
V_5 potential is resistive divided within IC to produce V_1, V_2, V_3 and V_4 potentials required for driving the liquid crystal. V_1, V_2, V_3 and V_4 potentials are then subject to impedance conversion and provided to the liquid crystal drive circuit.

The liquid crystal drive voltage is fixed to 1/5 (1/4) bias. The liquid crystal power terminals V_1 – V_5 must be externally connected with the voltage regulating capacitor C2.

When a built-in supply is used
When voltage is doubled



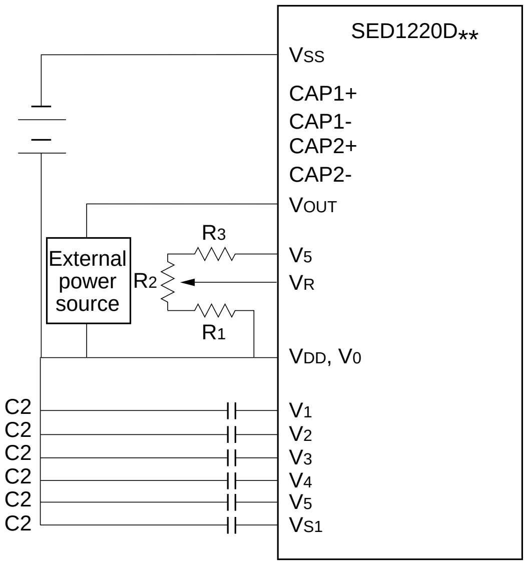
When voltage is tripled



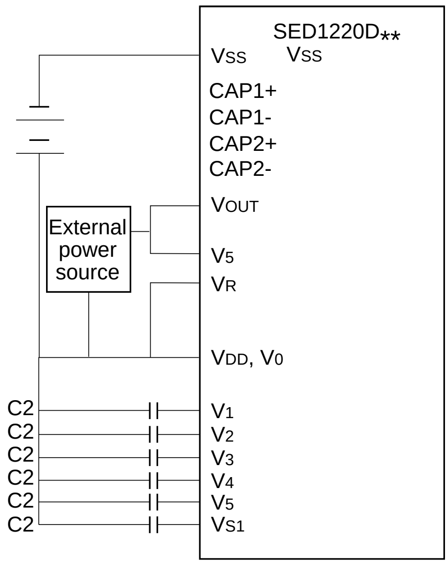
Reference setting values: C1: 0.1 - 4.7 µF, C2: 0.1 µF

We recommend the user to set the optimum values to capacitors C1 and C2 according to the panel size watching the liquid crystal display and drive waveforms.

Example 2: When using the built-in power source (VC, VF, P) = (1, 1, 0)

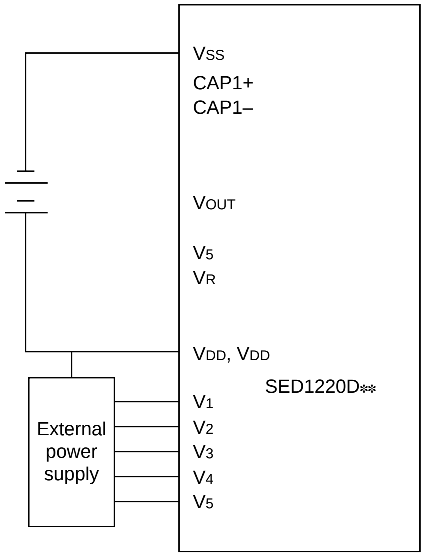


Example 3: When using the built-in power source (VC, VF, P) = (0, 1, 0)



Reference setting values: C1: 0.47 - 4.7 µF C2: 0.1 - 4.7 µF We suggest you to determine the most appropriate capacitance values, fitting to the panel size, for respective capacitors C1 and C2 in consideration of the liquid crystal display and drive waveforms.

When a built-in supply is used



Low Power Consumption Mode

SED1220 is provided with standby mode and sleep mode for saving power consumption during standby period.

● Standby Mode
Switching between on and off of the standby mode is done using the power save command.
In the standby mode, only static icon is displayed.

1. Liquid crystal display output
   COM1 ~ COM24, COMS1, COMS2 : VDD level
   SEG1 ~ SEG60, SEGS1, 2, 4, 5 : VDD level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Can be turned on by static drives.
   Use the static icon RAM for controlling the static icon display done with SEGSA, B, C, D, E, COMSA.
2. DD RAM, CG RAM and symbol register
   Written information is saved as it is irrespective of on or off of the stand-by mode.
3. Operation mode is retained the same as it was prior to execution of the standby mode.
   The internal circuit for the dynamic display output is stopped.
4. Oscillating circuit
   The oscillation circuit for the static display must be remained on.

● Sleep Mode
To enter the sleep mode, turning off the power circuit and oscillation circuit using the commands, and then execute power save command. This mode helps to save power consumption by reducing current to almost resting current level.

1. Liquid crystal display output
   COM1 ~ COM24, COMS1, COMS2 : VDD level
   SEG1 ~ SEG60, SEGS1, 2, 4, 5 : VDD level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Clear all the data of the static icon registers to "0".
2. DD RAM, CG RAM and symbol register
   Written information is saved at it is irrespective of on or off the sleep mode.
3. Operation mode mode is retained the same at it was prior to execution of the sleep mode.
   All internal circuits are stopped.
4. Power circuit and oscillation circuit
   Turn off the built-in supply circuit and oscillation circuit using the power save command and supply control command.

Reset Circuit

Upon activation of the RES input, this LSI will be initialized.

● Initial State

1. Display on/off control
   C = 0 : Cursor off
   B = 0 : Blink off
   D = 0 : Display off
2. Power save
   O = 0 : Oscillation off
   PS = 0 : Power save off
3. Supply control
   VC = 0 : Voltage regulation circuit off
   VF = 0 : Voltage follower off
   P = 0 : Amplifying circuit off
4. System setting
   N2, N1 = 0 : 2 lines
   S = 0 : Left-hand shift
   CG = 0 : "CGRAM" blank
5. Electronic volume control
   Address : 28H
   Data : (0, 0, 0, 0, 0)
6. Static icon
   Address : 20H
   Data : (0, 0, 0, 0, 0)
   Address : 21H
   Data : (0, 0, 0, 0, 0)
   Address : 22H
   Data : (0, 0, 0, 0, 0)
   Address : 23H
   Data : (0, 0, 0, 0, 0)

As explained in the Section "MPU interface", the RES terminal connects to the reset terminal of the MPU and initialization is being effected together with the MPU.
However, when the bus, port, etc. of the MPU maintains high-impedance for a certain duration of time after resetting, make the resetting input to the SED1220 after the inputs to the SED1220 have become definite.
As the resetting signal, like explained in the Section "DC characteristics", active level pulses of minimum 10us or more should be used. Normal operation status can be obtained after 1us from the edge of the RES signal.
By making the RES terminal active, respective registers can be cleared and the aforesaid setting state can be obtained.
If initialization is not effected by the RES terminal when the supply voltage is applied, it may go into a state where cancellation is unworkable.
In case the built-in liquid crystal power circuit will not be used, it becomes necessary that the RES input be active when the external liquid crystal power is being applied.

COMMAND

Table 4 lists the commands. SED1220 identifies the data bus signal using different combinations of A0 and $\overline{WR}$ (E). High speed command interpretation and execution are possible since only the internal timing is used.

- **Command Overview**

Command type	Command name	A0	$\overline{WR}$
Display control instruction	Cusor Home	0	0
	Display ON/OFF Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
System set	System set	0	0
Address control instruction	Address Set	0	0
Data input instruction	Data Write	1	0

Instruction execution duration of dependents on the internal process time of SED1220, therefore it is necessary to provide a duration larger than the system cycle time (t_{CYC}) between execution of two successive instruction.

- **Description of Commands**

(1) Cursor Home
This command presets the address counter to 30H and moves the cursor, when it is present, to the first digit of the first line.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	*	*	*	*

*: Don't Care

(2) Display ON/OFF Control
This command performs on or off of display and cursor setting.

Note: Symbols driven by COMSA and SEGSA – E must be controlled through the static icon RAM.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	C	B	*	D

D = 0 : Display off
1 : Display on

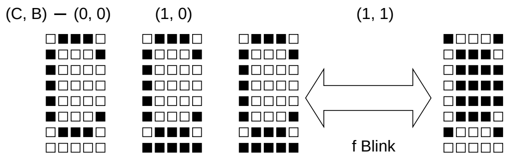
B = 0 : Cursor blink off
1 : Cursor blink on

Blink displays characters in black and white, alternately. The alternating display will be repeated with approx. 1 second interval.

C = 0 : Display of cursor
1 : Does not display

Following table shows relationship between B and C registers and the cursor.

C	B	Cursor display
0	0	Non-display
0	1	Non-display
1	0	Underbar cursor
1	1	Alternate display of display characters in black and white. The cursor position indicates the position of address



The cursor position indicates the position of address counter.

Therefore, whenever moving the cursor, change the address counter value using the RAM address set command or the auto increment done by writing the RAM data.

ISelective flashing symbol display is possible by selecting (C, B) = (1, 0) and thus locating the address counter to the position of the symbol register through selecting (since the symbol is corresponding to the character at each 5 dots).

(3) Power Save
This command is used to controlling the oscillation circuit and setting or resetting the sleep mode.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	*	*	O	PS

*: Don't Care

PS = 0 : Power save off (reset)
1 : Power save on (set)

O = 0 : Oscillating circuit off (stop of oscillation)
1 : Oscillating circuit on (oscilla tion)

(4) Supply Control
This command is used for controlling operation of the built-in power circuit.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	VC	VF	P

P = 0 : Amplifying circuit off
1 : Amplifying circuit on

Note: The oscillation circuit must be turned on for the amplitying circuit to be active.

VF = 0 : Voltage follower off
1 : Voltage follower on

VC = 0 : Voltage regulation circuit off
1 : Voltage regulation circuit on

(5) System Set
This command is used for selecting display line, common shift direction and use/non-use of CR RAM.
When power on or resetting is done, execute this command first.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	N1	N2	S	CG

∗ : Don't Care

N2, N1 = 0, 0 : 2lines
N2, N1 = 0, 1 : 3lines

S = 0 : COM left shift
= 1 : COM right shift

CG = 0 : Use CG RAM
1 : Does not use RAM

(6) RAM Address Set
This command sets addresses to write data into the DD RAM, CG RAM and symbol register in the address counter.

When the cursor is displayed, the cursor is displayed at the display position corresponding to the DD RAM address set by this command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ADDRESS						

① The settable address length is ADDRESS = 00H to 7FH.
② Before writing data into the RAM, set the data write address by this command. Next, when data is written in succession, the address is automatically incremented.

RAM Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 H	C G R A M (0 0 H)							–	C G R A M (0 1 H)							–
1 0 H	C G R A M (0 2 H)							–	C G R A M (0 3 H)							–
2 0 H	SI							–	EV	Test						–
3 0 H	DDRAM line 1								For signals					Unused		
4 0 H	DDRAM line 2													"		
5 0 H	DDRAM line 3													"		
6 0 H	Symbol register													"		
7 0 H	Symbol register													"		

– :Unused
For signals :Output from SEGS1 to SEGS2, SEGS4, SEGS5
For symbol register :Output from COMS1 to COMS2.

SI :Static icon register
EV :Electronic volume register
Test :Test register (Do not use)

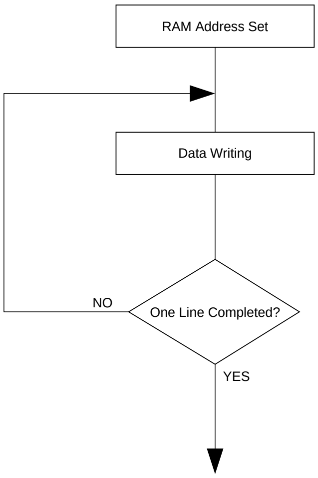
(7) Data Write

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DATA							

① This command writes data the DD RAM, CG RAM or symbol register.
② This command automatically increases the address counter by +1, thus enabling continuous writing of data.

<Example of Data Writing>

Following figures illustrates an example of continuous writing of one line data to DD RAM.



Note: When executing instructions in succession, reserve a time exceeding t_{CYC} and execute the next instruction.

Table 4 SED1220 Series Command List

Command	Code										Function
	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position.
(2) Display ON/OFF Control	0	0	0	0	1	1	C	B	*	D	Sets cursor ON/OFF (C), cursor blink ON//OFF (B), and display ON/OFF (D). C = 1 (cursor ON) 0 (cursor OFF), B = 1 (blink ON) 0 (blink OFF), D = 1 (display ON) D = 0 (display OFF)
(3) Power Save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (0). PS = 1 (power save ON) 0 (power save OFF), 0 = 1 (oscillating circuit ON) 0 (oscillating circuit OFF)
(4) Power Control	0	0	0	1	0	1	0	VC	VF	P	Sets voltage regulating circuit ON/OFF and boosting circuit ON/OFF (P). VC = 1 (voltage regulating circuit ON) 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) 0 (voltage follower OFF), P = 1 (boosting circuit ON) 0 (boosting circuit OFF)
(5) System Set	0	0	0	1	1	0	N2	N1	S	CG	Sets the use or non-use of CG RAM and shifting direction of display line (N1, N2) and COM CG = 1 (use of CG RAM), 0 = (Does not use CG RAM), M2, N1 = 0, 0 (2 lines) 0, 1 (3 lines). S = 0 (left shift), 1 (right shift).
(6) RAM Address Set	0	0	1	ADDRESS							Sets the DD RAM, CG RAM or symbol register address.
(7) RAM Write	1	0	DATA								Writes data into the DD RAM, CG RAM or symbol register address.
(8) NOP	0	0	0	0	0	0	0	0	0	0	Non-operation command
(9) Test Mode	0	0	0	0	0	0	*	*	*	*	Command for IC chip test. Don’t use this command.

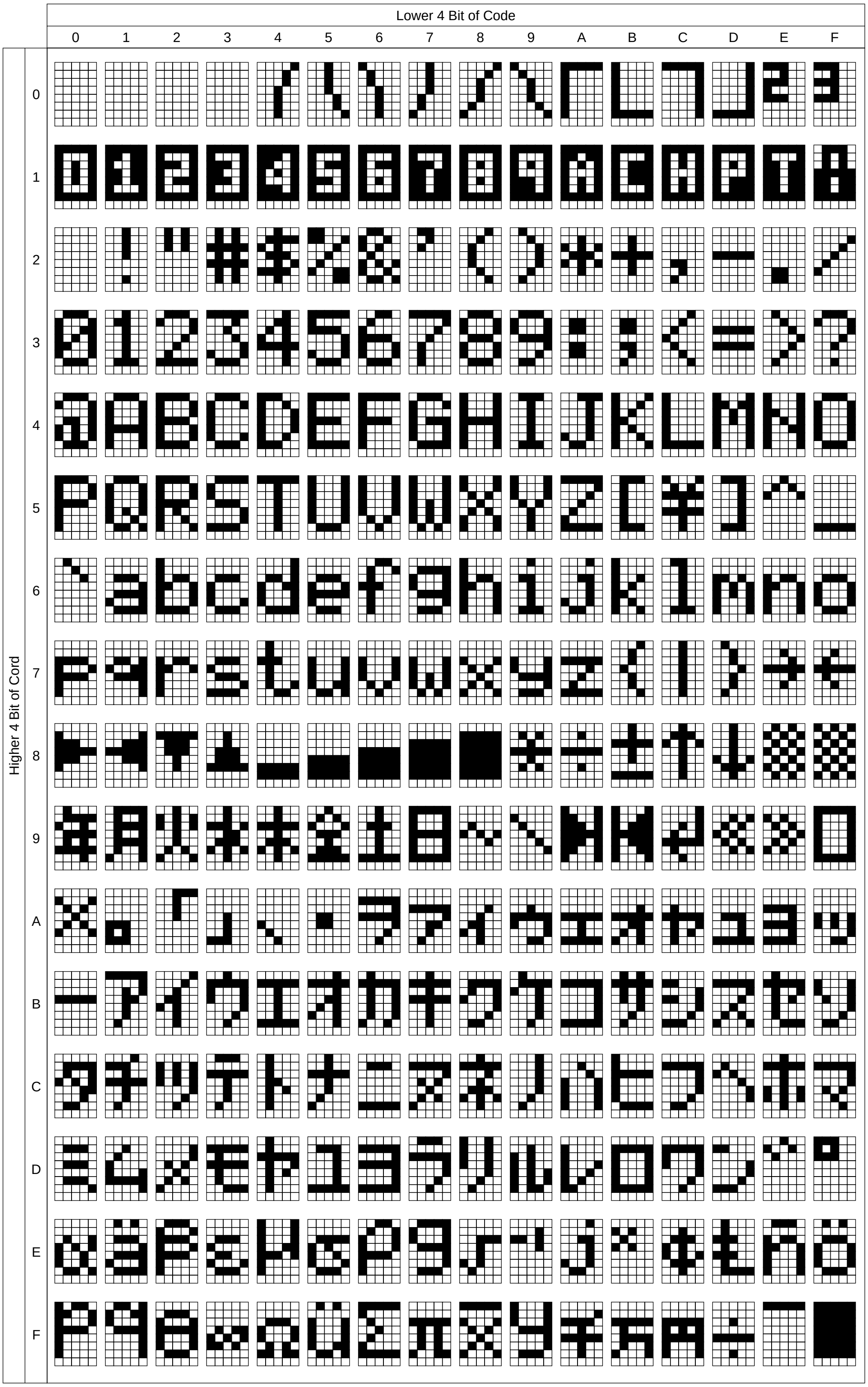
CHARACTER GENERATOR

Character Generator ROM (CG ROM)

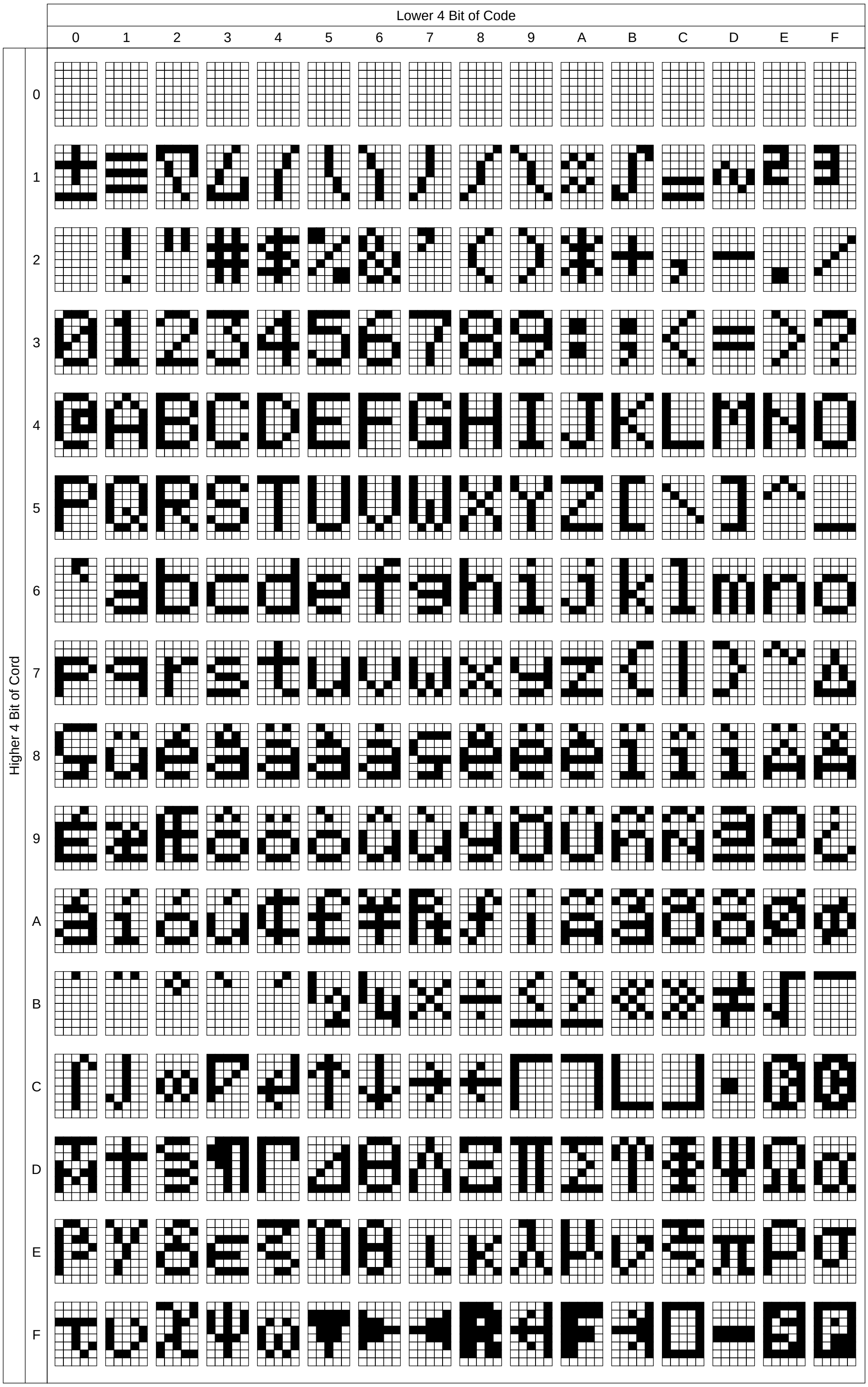
Character Generator ROM (CG ROM)
SED1220 cntains the character generator ROM (CG ROM) consisted of up to 256 types of characters.
Character size is 5 × 8 dots.
Tables 5 though 7 show the SED1220** character code.
Concerning the 4 characters from 00H through 03H, the system command selects on which of CG ROM and CG RAM they are to be used.
SED1220 CG ROM is mask ROM and compatible with customized ROM. Contact us for its use in your system.
Product name of modified CG ROM is defined as below:

(Example) S E D 1 2 2 0 D 0 B
↑
Digit for CG ROM pattern change

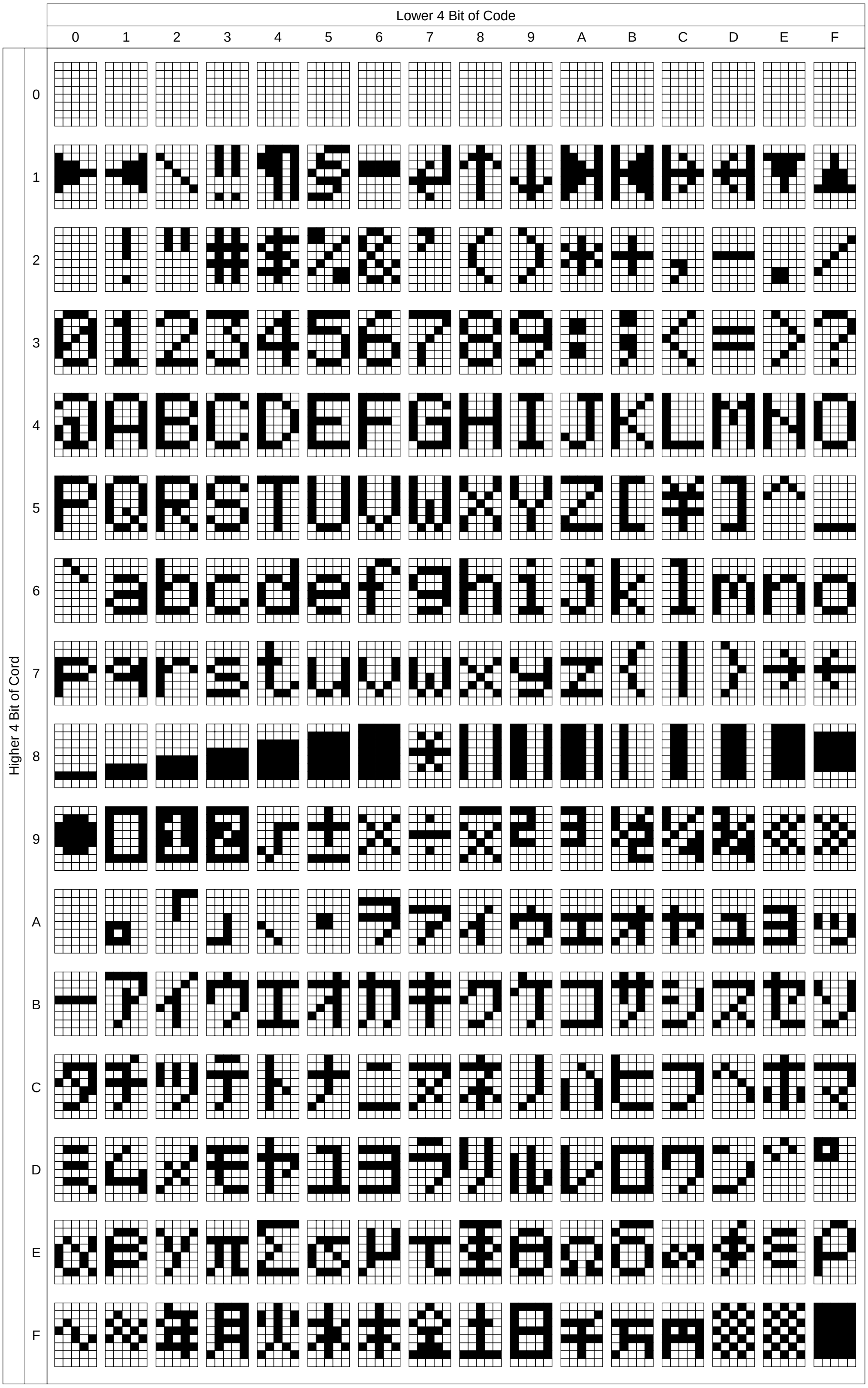
SED1220DA*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

SED1220DB*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

SED1220DG*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

Character Generator RAM (CG ROM)

CGRAM contained in SED1220 enables user programming of character patterns for display signals with higher degrees of freedom.

When using CGRAM, select it using the system command.

Capacity of CGRAM is 160 bits and accepts registration of any 4 5 ×8 dots patterns.

Following shows relationship between the CGRAM characters, CGRAM addresses and character code.

Character code	RAM address		CGRAM data (character pattern)								Character display	Signal display
			D7							D0	SEG	SEGS 1 2 4 5
00H 02H	00H~07H 10H~17H	0	*	*	*	0	1	1	1	1	□■■■■	□■ ■■
		1	*	*	*	1	0	0	0	0	■□□□□	■□ □□
		2	*	*	*	1	0	0	0	0	■□□□□	■□ □□
		3	*	*	*	0	1	1	1	1	□■■■■	□■ ■■
		4	*	*	*	0	0	0	0	1	□□□□■	□□ □■
		5	*	*	*	0	0	0	0	1	□□□□■	□□ □■
		6	*	*	*	1	1	1	1	0	■■■■□	■■ ■□
		7	*	*	*	0	0	0	0	0	□□□□□	□□ □□
01H 03H	08H~0FH 18H~1FH	8	*	*	*	0	0	1	0	0	□□■□□	□□ □□
		9	*	*	*	0	0	1	0	0	□□■□□	□□ □□
		A	*	*	*	0	1	1	1	0	□■■■□	□■ ■□
		B	*	*	*	0	1	1	1	0	□■■■□	□■ ■□
		C	*	*	*	0	1	1	1	0	□■■■□	□■ ■□
		D	*	*	*	1	1	1	1	1	■■■■■	■■ ■■
		E	*	*	*	0	0	0	0	0	■■■■■	■■ ■■
		F	*	*	*	0	0	0	0	0	□□□□□	□□ □□

Unused (D7–D5)

Character data (D4–D0)
1: Display
0: Non-display

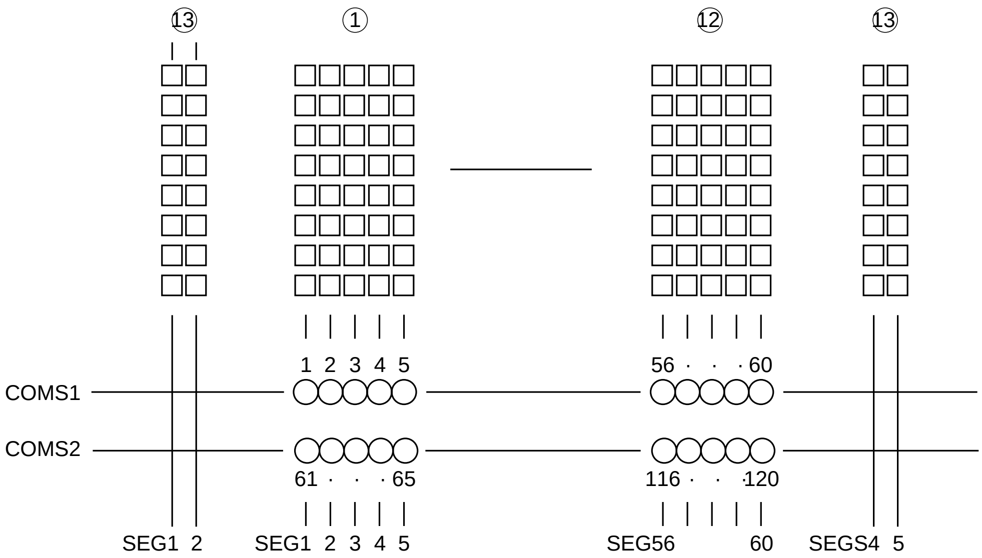
It is possible to set a 5 × 8 character size in this system. In this case, use the ∗7H/∗FH RAM. Note that the ∗7H/∗FH data is inverted when a under-bar cursor is used.

Symbol Register

SED1220 contains the symbol register which enable individual symbol setting for displaying on the screen.

Capacity of the symbol register is 120 bits and is capable of displaying up to 120 symbols.

Following shows relationship between the symbol register display patterns, RAM addresses and written data.



RAM address		Symbol Bits							
		D7							D0
60H~6BH	0	*	*	*	1	2	3	4	5
	1	*	*	*	6	7	8	9	10
	:	:							
	B	*	*	*	56	57	58	59	60
70H~7BH	0	*	*	*	61	62	63	64	65
	1	*	*	*	66	67	68	69	70
	:	:							
	B	*	*	*	116	117	118	119	120

Note: When the symbol is 1.5 times or more than the character, it is recommended to drive it using both COMS1 and COMS2.

Static Icon Ram

SED1220 contains the static icon RAM for displaying the static icons in addition to the dynamic icons. Capacity of static icon RAM is 10 bits (SED1220/1221/1222) or 20 bit (SED122A) and is capable of displaying up to 5 icons (SED1220/1221/1222) or 10 icons (SED122A).
Following shows relationship between the static icons functions, static icon RAM addresses and written data.

< SEGSA, B, C, D, E >

Function	RAM address	Static icon data								Display
		D7							D0	S E G S A B C D E
Display On/Off	20H	*	*	*	0	0	1	1	1	□□■■■
Blink On/Off	21H	*	*	*	1	0	0	0	1	□□■■■ ⇕ f BLINK ■□■■□

< SEGSF, G, H, I, J >

Function	RAM address	Static icon data								Display
		D7							D0	S E G S F G H I J
Display On/Off	22H	*	*	*	0	0	1	1	1	□□■■■
Blink On/Off	23H	*	*	*	1	0	0	0	1	□□■■■ ⇕ f BLINK ■□■■□

*: Blank
1: Display or blink on
0: Display or blink off
f_{BLINK}: 1–2 Hz

Electronic Volume RAM (register)

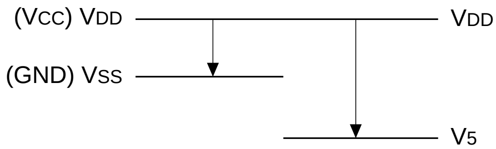
SED1220 contains the electronic volume function for controlling the liquid crystal drive voltage V5 and density of liquid crystal display. The electronic volume function enables to select one of 32 voltage status of the liquid crystal drive voltage V5 by writting 5-bit data to the electronic volume RAM.
Following shows relationship between RAM addresses set by the electronic volume and written data.

Function	RAM address	Electronic volume data								Condi-tion	V_{EV}
		D7							D0		
Electronic volume data	28H	*	*	*	0	0	0	0	0	0	V_{REG}–0
		*	*	*	0	0	0	0	1	1	V_{REG}–α
		*	*	*	0	0	0	0	0	2	V_{REG}–2α
							:			:	
							:			:	
		*	*	*	1	1	1	0	1	29	V_{REG}–29α
		*	*	*	1	1	1	1	0	30	V_{REG}–30α
		*	*	*	1	1	1	1	1	31	V_{REG}–31α
	29H	*	*	*	*	*					For testing

* : Blank
Note : Do not use the address "29H". It is for testing
$\alpha = V_{REG}/150$

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	–6.0~+0.3	V
Power supply voltage (2)		V_5, V_{out}	–7.0~+0.3	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	V_5~+0.3	V
Input voltage		V_{IN}	V_{SS}–0.3~+0.3	V
Output voltage		V_O	V_{SS}–0.3~+0.3	V
Operating temperature		T_{opr}	–30~+85	°C
Storage temperature	TCP	T_{str}	–55~+100	°C
	Bare chip		–65~+125	



Notes: 1. All the voltage values are based on V_{DD} = 0 V.
2. For voltages of V_1, V_2, V_3 and V_4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

SED1220

DC CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.

Item		Symbol	Condition	min	typ	max	Unit	Applicable pin
Power supply voltage (1)	Operatable	V_{SS}		–3.6	–3.0	–2.4	V	V_{SS} *1
	Data retain voltage			–3.6		–2.0		
Power supply voltage (2)	Operatable	V_5		–7.0		–4.0	V	V_5 *2
	Operatable	V_1, V_2		0.6×V_5		V_{DD}	V	V_1, V_2
	Operatable	V_3, V_4		V_5		0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHC}		0.2×V_{SS}		V_{DD}	V	*3
Low-level input voltage		V_{ILC}		V_{SS}		0.8×V_{SS}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0		1.0	µA	*3
LC driver ON resistance		R_{ON}	Ta=25°C V_5=–7.0V ΔV=0.1V		20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}			0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	Display state	V_5 = –6 V without load			80	µA	V_{DD} *5
		Standby state	Oscillation ON, Power OFF, V_{SS} = –3V without load			20	µA	V_{DD}
		Sleep state	Oscillation OFF, Power OFF, V_{SS} = –3.0V			5	µA	V_{DD}
		Access state	f_{cyc}=200KHz, V_{SS} = –3.0V			500	µA	V_{DD} *6
Input pin capacity		C_{IN}	Ta=25°C f=1MHz		5.0	8.0	pF	*3

Item	Symbol	Condition	min	typ	max	Unit	Applicable pin
Frame frequency	f_{FR}	Ta=25°C V_{SS}=–3.0V	70	100	130	Hz	*10
External clock frequency	f_{ck}	Display of 2 lines		23.4		KHz	*10 *11
	f_{ck}	Display of 3 lines		33.8		KHz	*10 *11

Item	Symbol	Condition	min	typ	max	Unit	Applicable pin
Reset time	t_R		1.0			µs	*7
Reset pulse width	t_{RW}		10			µs	*8
Reset start time	t_{RES}		50			ns	*8

Dynamic system

	Item	Symbol	Condition	min	typ	max	Unit	Applicable pin
Built-in power supply	Input voltage	V_{S1}		–2.3	–2.1	–1.9	V	*9
	Amplified voltage output voltage	V_{OUT}	When voltage is tripled	–6.9	–6.3	–5.7	V	V_{OUT}
	Voltage follower operating voltage	V_5		–7.0		–4.0	V	
	Reference voltage	V_{REG}	Ta = 25°C	–2.06	–2.0	–1.94	V	

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

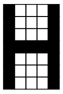
*2: When the voltage is Tripled, care must be paid to supply the voltage V_{SS} so that operating voltage of V_{OUT} and V_5 may not be exceeded.

*3: D0 ~ D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).

R_{ON} = 0.1 V / ΔI

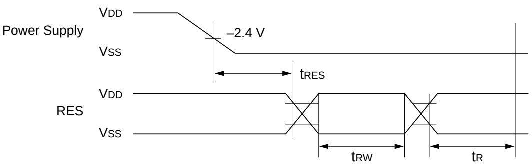
(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Character “  ” display. This is applicable to the case where no access is made from the MPU and the built-in power circuit and oscillating circuit are in operation.

*6: Current consumption when data is always written by f_{cyc}.
The current consumption in the access state is almost proportional to the access frequency (f_{cyc}).
When no access is made, only I_{DD} (I) occurs.

*7: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the SED1220 usually enters the operating state after t_R.

*8: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.



All signal timings are based on 20% and 80% of VSS signals.

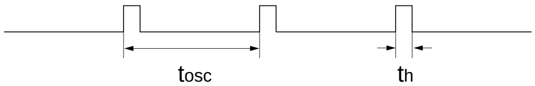
*9: When operating the boosting circuit, the power supply VSS must be used within the input voltage range.

*10: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

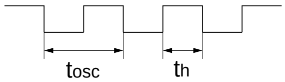
f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}

*11: When performing the operations using an external clock, not taking advantage of the built-in oscillation circuit, input the waveforms indicated below. Meanwhile, while using an external clock but when clock inputs are not being made, fix it to “H”. (Normal High)

<Incase the external clock = fosc>
- Duty = (t_h/tosc) × 100 = 20 ~ 30%
- fosc = 1/tosc

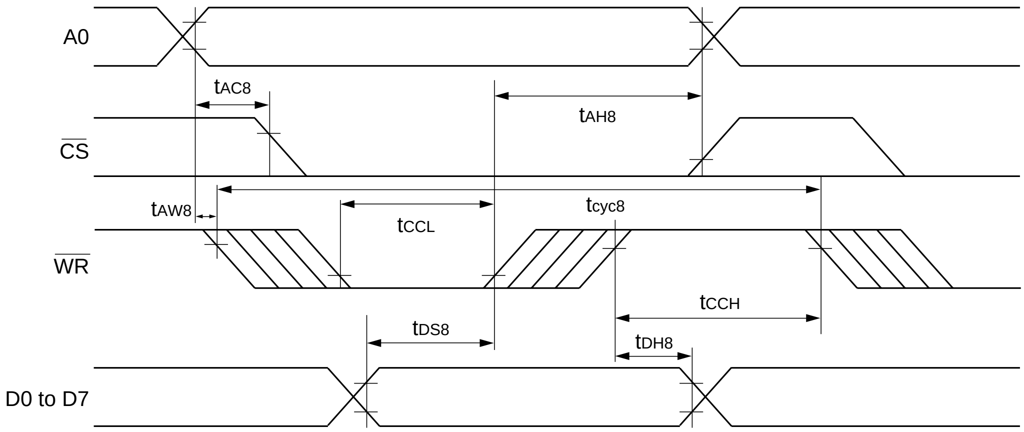


<Incase the external clock = 4 × fosc>
- Duty = (t_h/tosc) × 100 = 50%
- fosc = 1/tosc



TIMING CHARACTERISTICS

(1) MPU Bus Write Timing (80 series)



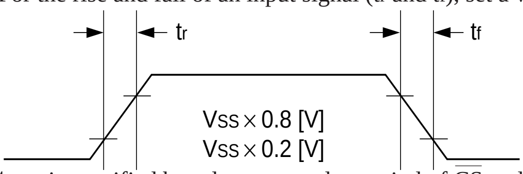
[Ta = –30 to 85°C, VSS = –3.6 V to –2.4 V]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}	Every timing is specified	30	–	ns
Address setup time		t_{AW8}	on the basis of 20% and	60	–	ns
$\overline{CS}$ setup time		t_{AC8}	80% of VSS.	0	–	ns
System cycle time	$\overline{WR}$	t_{CYC8}		650	–	ns
Write “L” pulse width (WR)		t_{CCL}		150	–	ns
Write “H” pulse width (WR)		t_{CCH}		450	–	ns
Data setup time	D0 ~ D7	t_{DS8}		100	–	ns
Data hold time		t_{DH8}		50	–	ns

[Ta = –30 to 85°C, VSS = –3.3 V to –2.7 V]

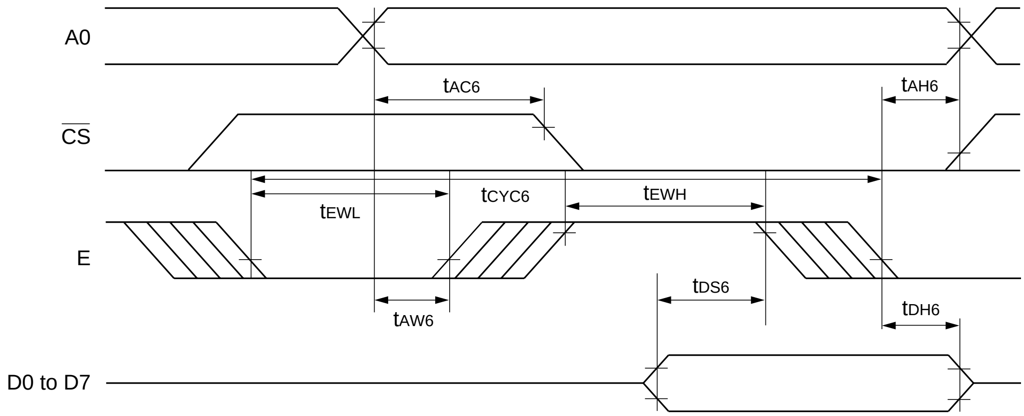
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}	Every timing is specified	10	–	ns
Address setup time		t_{AW8}	on the basis of 20% and	60	–	ns
$\overline{CS}$ setup time		t_{AC8}	80% of VSS.	0	–	ns
System cycle time	$\overline{WR}$	t_{CYC8}		500	–	ns
Write “L” pulse width (WR)		t_{CCL}		100	–	ns
Write “H” pulse width (WR)		t_{CCH}		350	–	ns
Data setup time	D0 ~ D7	t_{DS8}		100	–	ns
Data hold time		t_{DH8}		20	–	ns

*1: For the rise and fall of an input signal (t_r and t_f), set a value not exceeding 25ns (excluding RES input).



*2: t_{CCL} is specified based on an overlap period of $\overline{CS}$ and $\overline{WR}$ “L” levels.

(2) MPU Bus Write Timing (68 series)



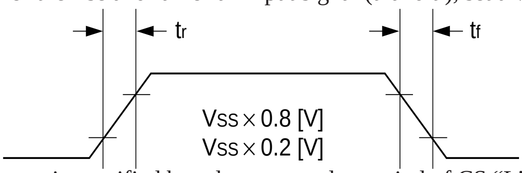
[Ta = –30 to 85°C, VSS = –3.6 V to –2.4 V]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address setup time	A0, $\overline{CS}$	t_{AW6}	Every timing is specified on the basis of 20% and 80% of VSS.	60	–	ns
Address hold time		t_{AH6}		30	–	ns
$\overline{CS}$ setup time		t_{AC6}		0	–	ns
System cycle time	$\overline{WR}$	t_{CYC6}		650	–	ns
Enable "L" pulse width (WR)		t_{EWL}		150	–	ns
Enable "H" pulse width (WR)		t_{EWH}		450	–	ns
Data setup time	D0 ~ D7	t_{DS6}		100	–	ns
Data hold time		t_{DH6}		50	–	ns

[Ta = –30 to 85°C, VSS = –3.3 V to –2.7 V]

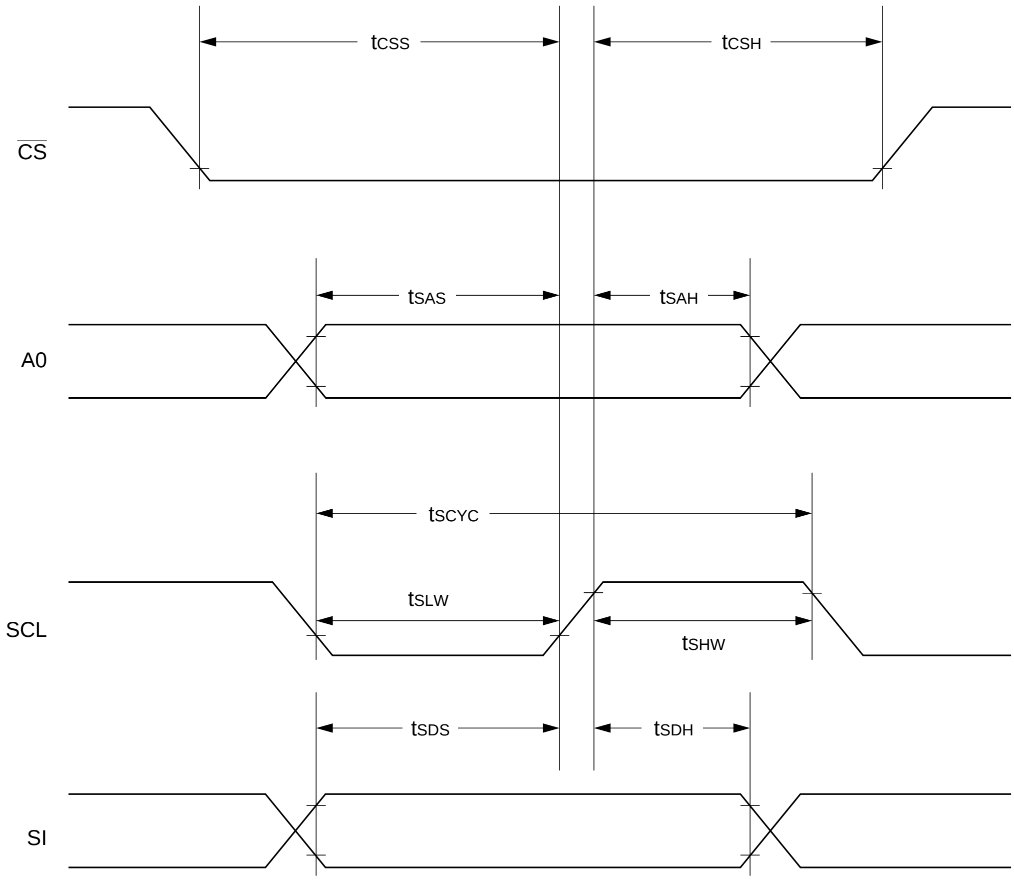
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address setup time	A0, $\overline{CS}$	t_{AW6}	Every timing is specified on the basis of 20% and 80% of VSS.	60	–	ns
Address hold time		t_{AH6}		10	–	ns
$\overline{CS}$ setup time		t_{AC6}		0	–	ns
System cycle time	$\overline{WR}$	t_{CYC6}		500	–	ns
Enable "L" pulse width (WR)		t_{EWL}		100	–	ns
Enable "H" pulse width (WR)		t_{EWH}		350	–	ns
Data setup time	D0 ~ D7	t_{DS6}		100	–	ns
Data hold time		t_{DH6}		20	–	ns

*1: For the rise and fall of an input signal (t_r and t_f), set a value not exceeding 25ns (excluding RES input).



*2: t_{EWH} is specified based on an overlap period of CS "L" and E "H" levels.

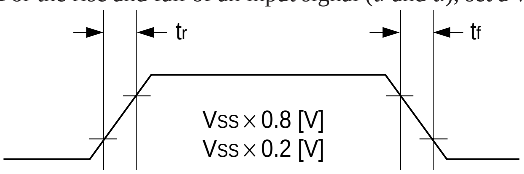
(3) Serial Interface



[Ta = –30 to 85°C, VSS = –3.6 V to –2.4 V]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	Every timing is specified	1000		ns
SCL "H" pulse width		tSHW	on the basis of 20% and	300		ns
SCL "L" pulse width		tSLW	80% of VSS.	300		ns
Address setup time	A0	tSAS		50		ns
Address hold time		tSAH		300		ns
Data setup time	SI	tSDS		50		ns
Data hold time		tSDH		50		ns
CS-SCL time	CS	tCSS		150		ns
		tCSH		700		ns

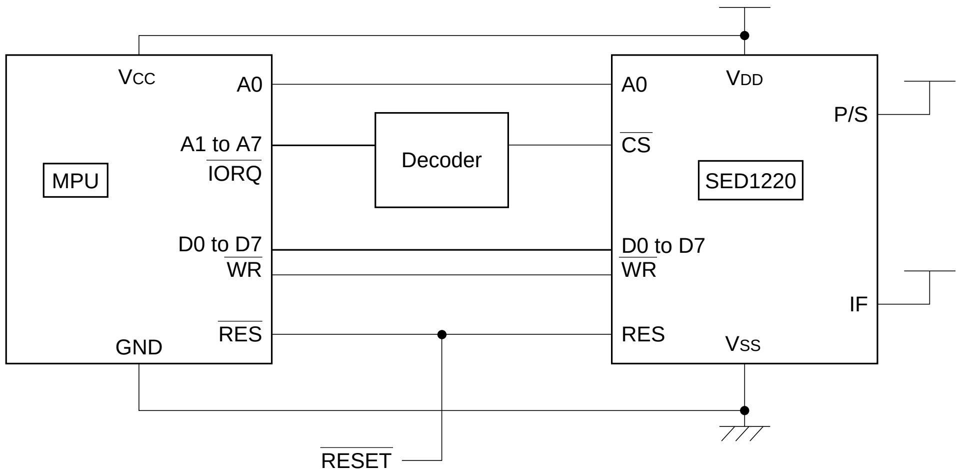
*1: For the rise and fall of an input signal (tr and tf), set a value not exceeding 25ns (excluding RES input).



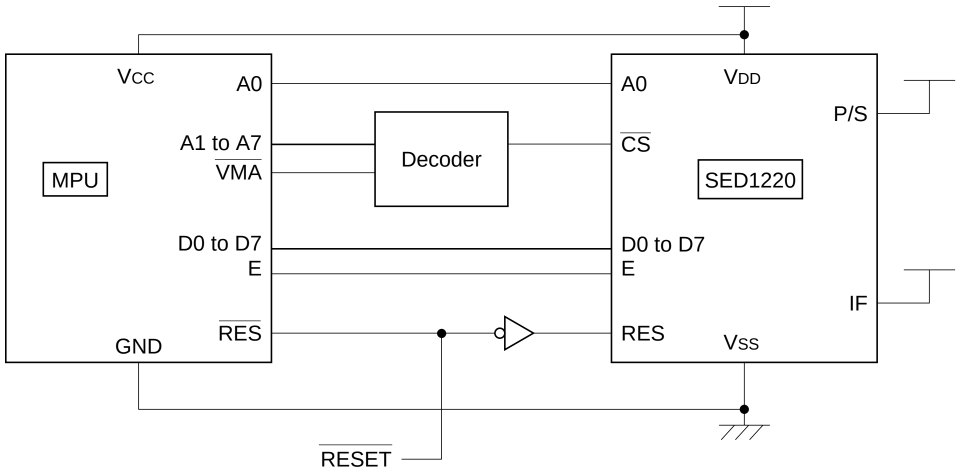
MPU INTERFACE (REFERENCE EXAMPLES)

The SED1220 Series can be connected to the 80 series MPU and 68 series MPU. When an serial interface is used, the SED1220 Series can be operated by less signal lines.

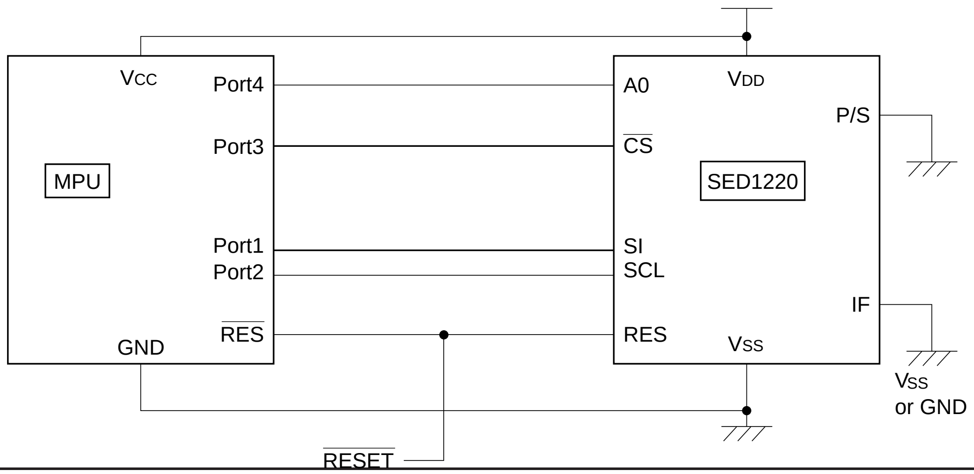
80 Series MPU



68 Series MPU

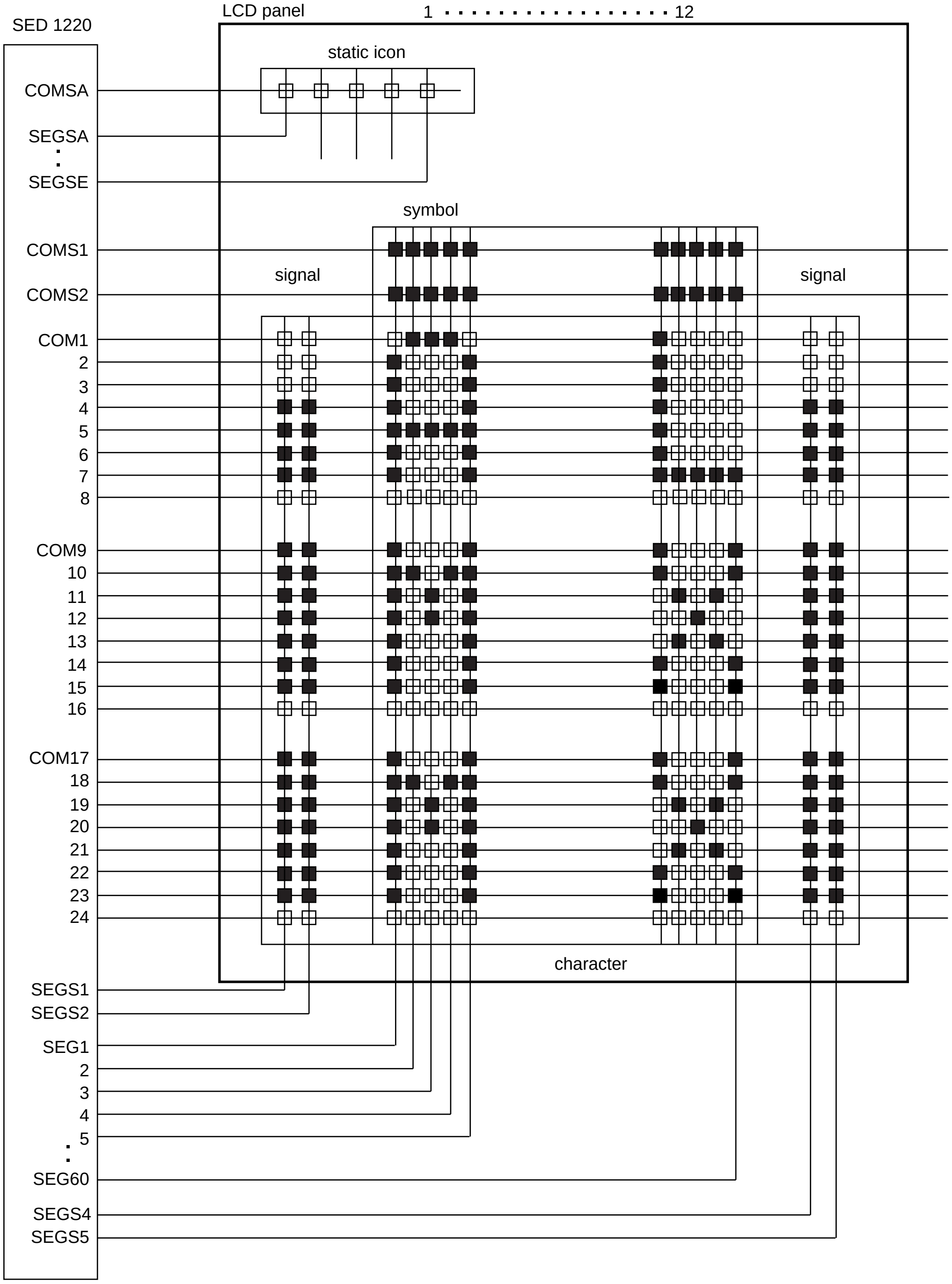


Serial Interface

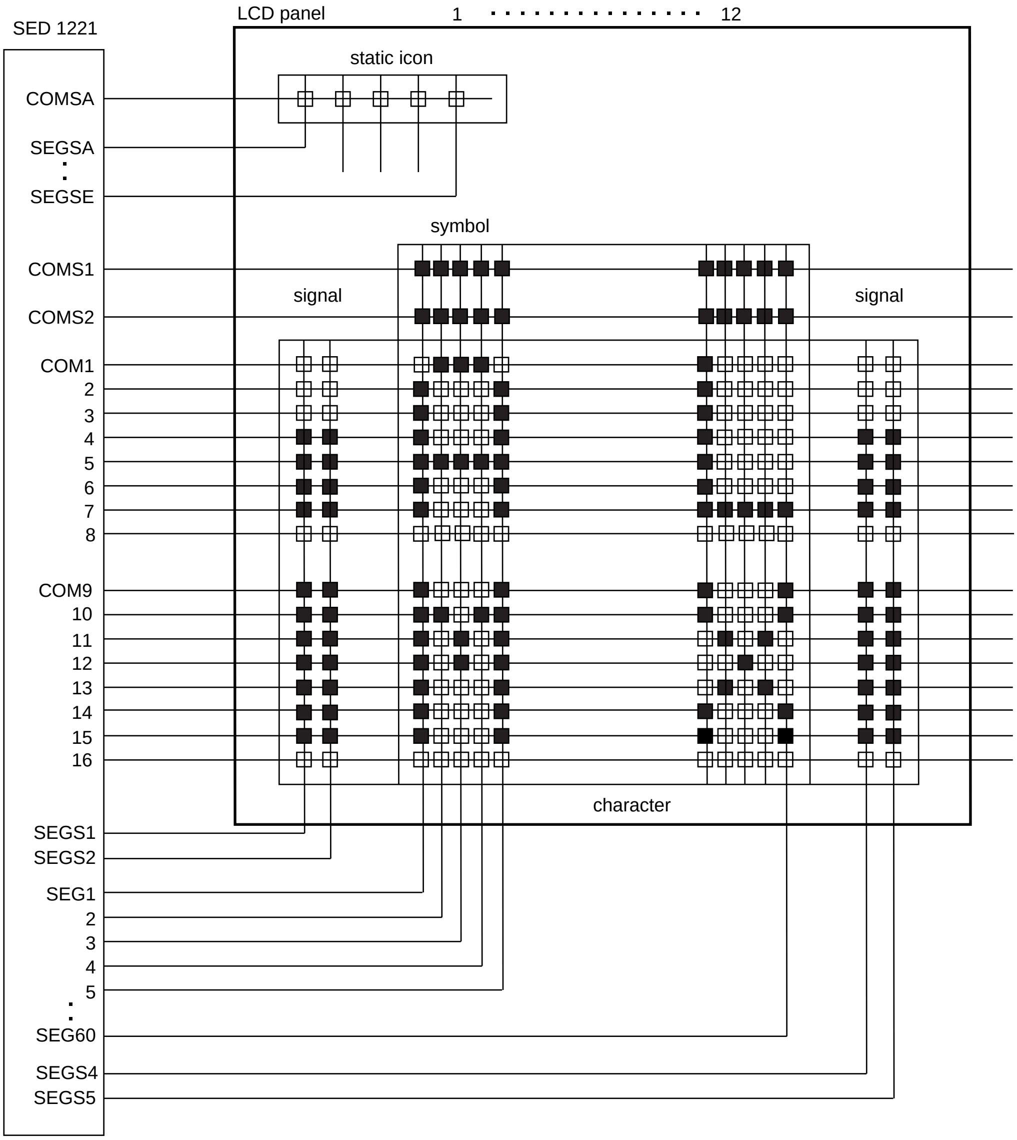


INTERFACE TO LCD CELLS (REFERENCE)

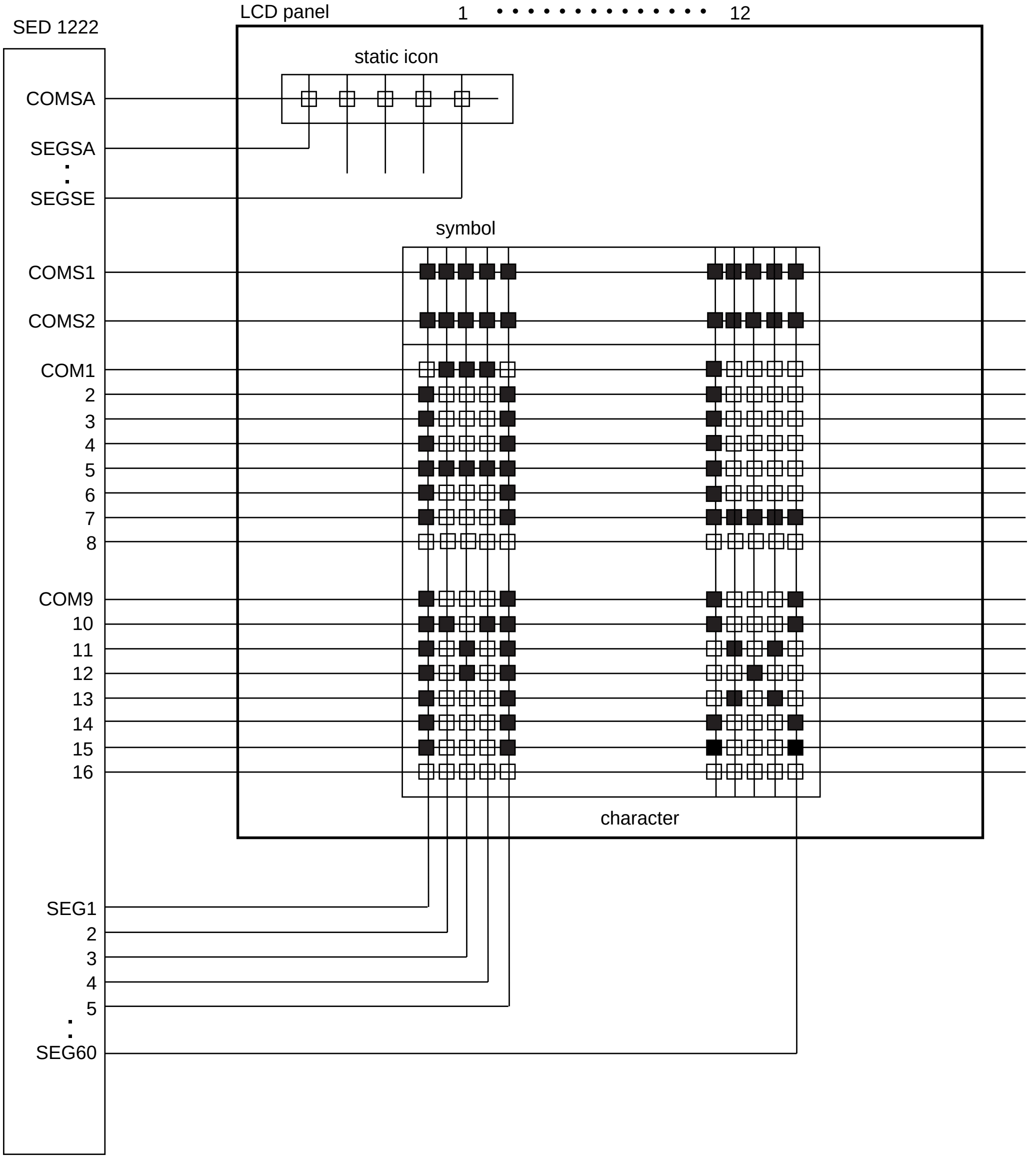
12 columns by 3 lines, 5 × 8-dot matrix segments and symbols



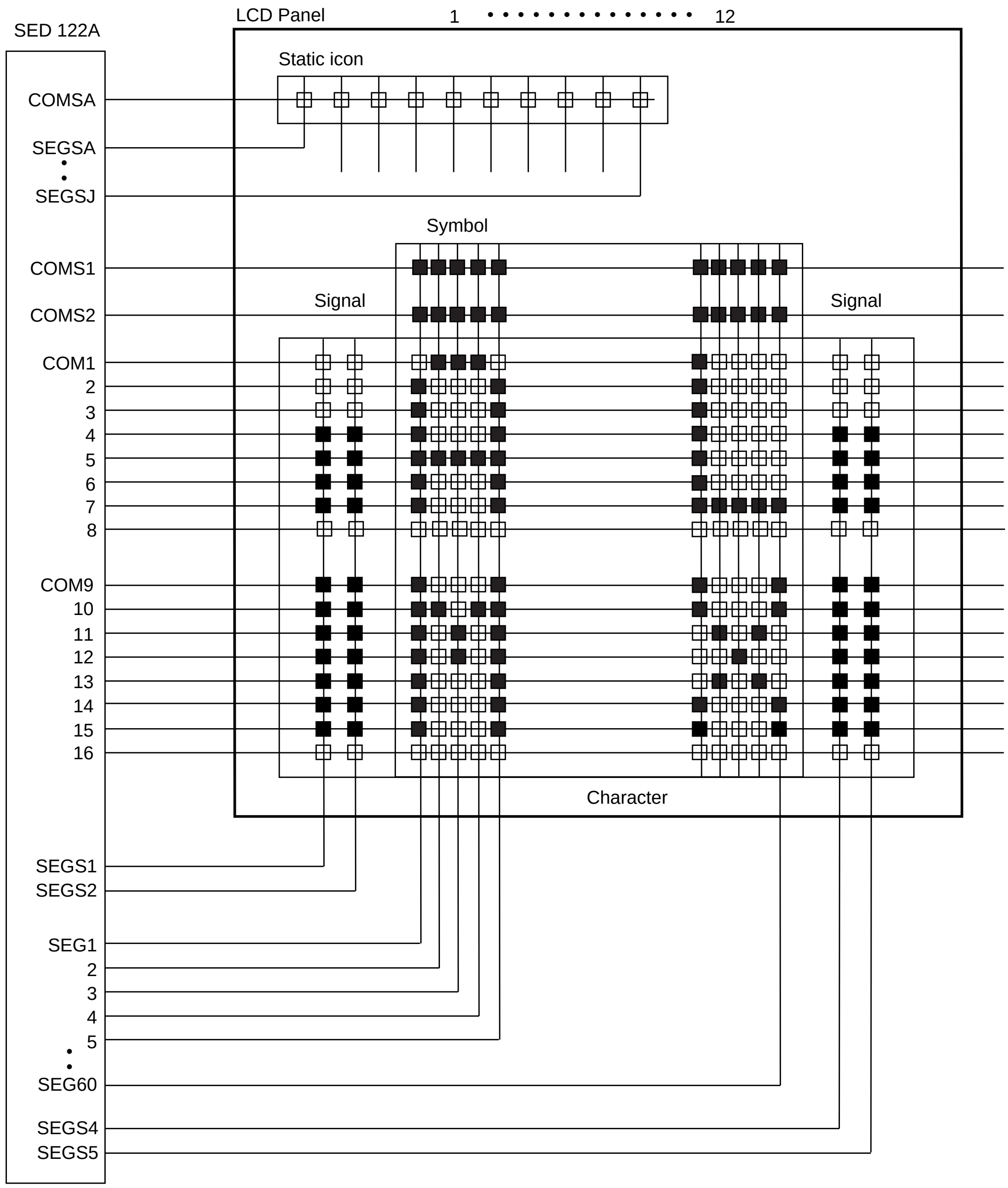
12 columns by 2 lines, 5 × 8-dot matrix segments and symbols



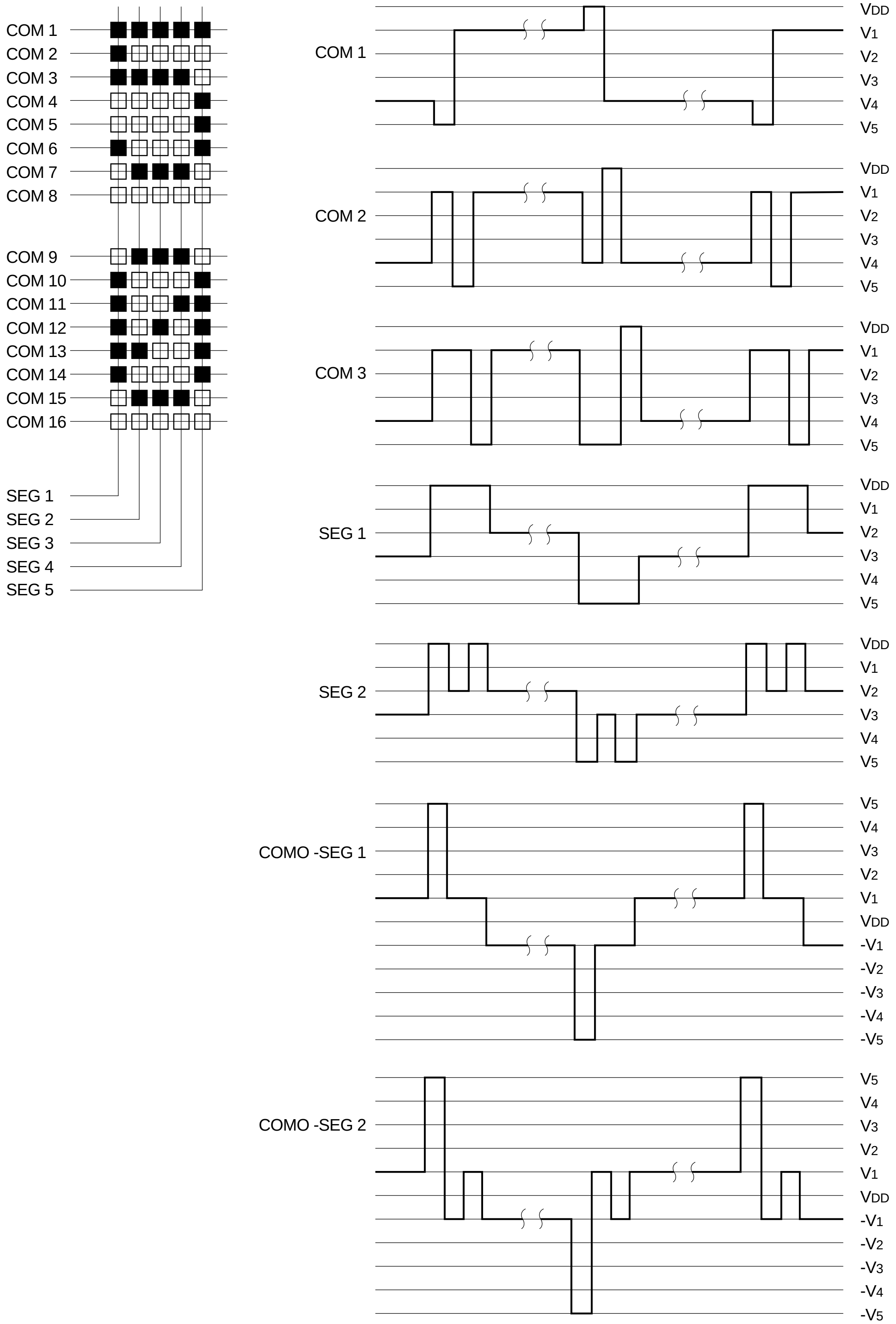
12 columns by 2 lines, 5 × 8-dot matrix segments and symbols



12 columns by 2 lines, 5 × 8-dot matrix segments and symbols



LIQUID CRYSTAL DRIVE WAVEFORMS (B WAVEFORMS)



Instruction Setup Example (Reference Only)

(1) Initial setup

VDD-VSS power ON

Power regulation

Input of reset signal

Command status
- Static display control: Off
- Display on/off control: Off
- Power save: Off
- Power control: Off
- System setup: Off
- Electronic volume (0, 0, 0, 0, 0)
- Static icon (0, 0, 0, 0, 0)
- Others are undefined.

Waiting for 10 sec or more

Command input:
(Asterisk indicates any command sequence.)
(1) NOP command
(2) System setup command
( ) Electronic volume register setup
- Address: 28H
- Data: (, , , ,)

( ) Power save command
- PS: Off (Power save)
- O: On (Oscillation)

(5) Power control commands
- P, VF, VC: On

(6) RAM address setup 1)
(7) Data writing 1)

Waiting for 20msec or more 2)

Command input
(8) Display on/off control command 3)
- D: On (Display)

Data input
(9) Static icon control 3)
- Address: 20H
- Data: (, , , ,)
- Address: 21H
- Data: (, , , ,)

End of initialization

(2) Display mode

End of initialization

Input of RAM address setup command

Input of RAM (data) write command

Display of written data

Notes 1) Commands (6) and (7) initialize the RAM. The display contents must first be set. The non-display area must satisfy the following conditions (for RAM clear).
- DDRAM: Write the 20H data (character code).
- CGRAM: Write the 00H data (null data).
- Symbol register: Write the 00H data (null data).

As the RAM data is unstable during reset signal input (after power-on), null data must be written. If not, unexpected display may result.

2) Since it is specified based on rise characteristics of the booster, power control and voltage follower circuits, time to be set differs depending on external capacity. Be sure to set it after the external capacity is confirmed.

3) A display of the dynamic drive series is turned on when the on command is input and the static icon is turned on using the static icon control command.
To turn both on at the same time when the display is turned on, execute display on/off command and static icon control within 1 frame period.

(3-1) Selecting the Standby mode

End of initialization

Normal operation
(Power Save is released and
oscillator circuit is turned ON.)

(1) Input of display on/off control command
- D: Off (Display)

(2) Input of power save command
- PS: On (Power save)
- O: On (Oscillation)

(3) Input of power control command
- P, VF, VC: Off

Standby status

Only static icon displayed

(3-2) Releasing the Standby mode

Standby mode

(1) Input of power save command
- PS: Off (Power save)
- O: On (Oscillation)

(2) Input of power control command
- P, VF, VC: On

Waiting for 20msec or more [2)]

(3) Input of display on/off control command
- D: Off (Display)

Return to normal operation (initial status).

(4-1) Selecting the Sleep mode

End of initialization

Normal operation
(Power Save is released and
oscillator circuit is turned ON.)

(1) Input of display on/off control command
- D: Off (Display)

(2) Static icon control
- Address: 20H
- Data: (0, 0, 0, 0, 0)
- Address: 21H
- Data: (0, 0, 0, 0, 0)

(3) Input of power save command
- PS: On (Power save)
- O: Off (Oscillation)

(4) Input of power control command
- P, VF, VC: Off

Enter the Sleep mode.

(4-2) Releasing the Sleep mode

Sleep mode

(1) Input of power save command
- PS: Off (Power save)
- O: On (Oscillation)

(2) Input of power control command
- P, VF, VC: On

Waiting for 20msec or more [2)]

(3) Input of display on/off control command [3)]
- D: Off (Display)

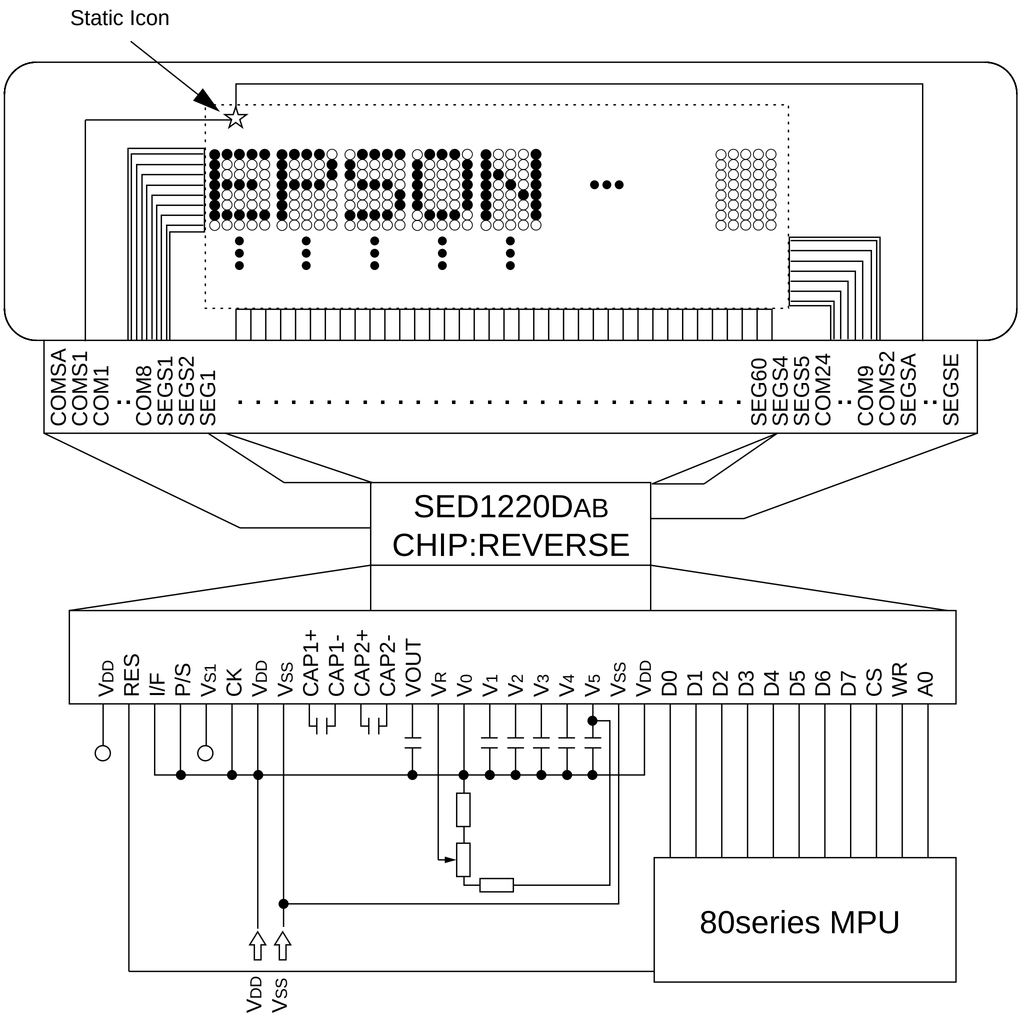
(4) Static icon control [3)]
- Address: 20H
- Data: (, , , ,)
- Address: 21H
- Data: (, , , ,)

Return to normal operation (initial status).

Instruction Setup Example of SED1220 series

(1) Initial setup
(2) display ON “EPSON”
(3) Display ON the Icon
(4) Standby Mode sequence
(5) Releasing the Standby Mode sequence

<Diagram of SED1220Txx and LCD Panel>



(1) Initial setup

(1.1) VDD–VSS Power ON

(1.2) Power regulation

(1.3) Input of RESET signal

(1.4) Command Status

- Display ON/OFF :OFF
- Power save :OFF
- Power control :OFF
- System reset :OFF
- Electronic Volume :(0, 0, 0, 0, 0)
- Static display control :OFF
- Others are undefined.

(1.5) Waiting for 10µ sec or more

(1.6) Command Input: ((*) indicates any command sequence.)

(a) System Setup command: CGRAM→Not use, 3lines, COM Left shift

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	1	0	0

(*) Electronic volume resister setup: Data→(0, 0, 0, 0, 0, 0)

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0

(*) Power save command: PS→0, 0→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0/1	0/1	1	0

(d) Power Control command: P, VF, VC→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	1	1	1

(e) (f) RAM address setup, Data writing

• RAM address setup: Set address is 30H

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	0	0	0

• Data writing: All data→20H (for 1 Line)

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0

• RAM address setup: Set address is 40H

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	0	0	0

• Data writing: All data→20H (for 2 line)

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0

• RAM address setup: Set address is 50H

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	0	0	0	0

• Data writing: All data →20H (for 3 Line)

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0

• End of Initialization

(2) Display ON “EPSON”
(2.1) RAM address setup command: 30H

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	0	0	0

(2.2) Data writing command: Writing “EPSON”

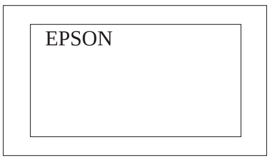
A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	1	0	0	0	1	0	1	E: 45H
1	0	0	1	0	1	0	0	0	0	P: 50H
1	0	0	1	0	1	0	0	1	1	S: 53H
1	0	0	1	0	0	1	1	1	1	O: 4FH
1	0	0	1	0	0	1	1	1	0	N: 4EH

(2.3) Waiting for 20ms or more

(2.4) Display ON/OFF control command: B, C→0, D→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	1

Display ON 5×7 Dots “EPSON”



(3) Display ON The Icon: Valid in Standby mode only

(3.1) Display ON/OFF command: D→OFF

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	0

(3.2) Static display control command: 1 ~ 2Hz Blink

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1
1	0	0	0	0	1	0	0	0	0

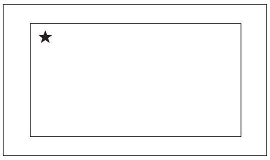
(3.3) Power save command: PS→ON, 0→ON

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0/1	0/1	1	1

(3.4) Power control commands: P, VF, VC→OFF

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	0	0	0

Display ON the Icon



(4) Releasing the Standby Mode

(4.1) Power save command: PS→0, 0→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0/1	0/1	1	0

(4.2) Power control commands: P, VF, VC→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	1	1	1

(4.3) Waiting for 20ms or more

(4.4) Display ON/OFF command: D→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	1

END of Releasing the Standby mode

Option List

SED1220 provides the optional functions as described in the following. Being adaptable to the customer's optional demand, contact the Business Department of our company when installed.

○ Our product name corresponding to a customer's option is defined as shown below:

(Example) SED1220D XB

- X: Option corresponding digit
- B: Shipping form: A (AL pad product) or B (metal bump product)
- 0 (after SED122): Machine type: 0 (12 digits × 3 lines) or 1 (12 digits × 2 lines)

1. Specification of Character Generator ROM (CGROM)
   SED1220 integrates a character generator ROM which can generate a maximum of 256 type characters. The size of these characters is composed of 5 × 7 (8) dots.
   Being a mask ROM, the SED1220 CGROM is adaptable to the character generator ROM exclusive for the customer, too.
   For our standard CGROMs, refer to the Character Fonts Table.
2. Specification of Liquid Crystal Driver Voltage Bias Value.
   SED1220 integrates a liquid crystal diver voltage generator circuit. Its 5-volt potential is divided into resistance inside of IC to generate 1-V, 2-V, 3-V or 4-V potential as required for the liquid crystal driver. Further, the 1-V, 2-V, 3-V or 4-Vpotential is converted into impedance by a voltage follower to be supplied to the liquid crystal driver circuit.
   Either 1/5 or 1/4 bias value can be selected as demanded by the customer.
   Our standard bias value is preset to 1/5.
3. Specification of Reference Voltage of Liquid Crystal Driver Voltage Regulation Circuit.
   SED1220 integrates a voltage regulation circuit using a booster voltage as its power supply to generate 5V for the liquid crystal driver via the voltage regulation circuit.
   The voltage regulation circuit integrates a reference voltage regulator V_{REG}.
   The customer can select a specification of using either the internal reference voltage or external V_{SS} reference voltage.
   Our standard specification is preset to the internal reference voltage.
4. Power Supply to Booster Circuit
   SED1220 integrates a booster circuit.
   The customer can select a specification of using either the regulator output V_{S1} or V_{SS} as the supply voltage to the booster circuit.
   Our standard specification is preset to the regulator output V_{S1}.
5. External Clock Specifications
   SED1220 integrates an external clock terminal and there are two clock specifications, f and 4×f oscillation.
   Either of them can be selected on your request.

	Internal oscillation	External clock f osc.	External clock 4×f osc.
Standard	○	○	×
Optional	○	×	○

The standard external clock specification is set to f_{OSC}.

6. Reset Signal Input Polarity Specifications
   SED1220 inputs reset signal from the reset terminal using edge detection and I/F specification 80/68 series can be selected according to this signal level.
   RES input polarity can also be selected on your request.

RES input polarity	Type	
	Standard	Optional
↓ (falling)	68 series	80 series
↑ (rising)	80 series	68 series

↓ is set to the 68 series and ↑ to the 80 series as the standard RES input polarities.

7. Pad Layout Specifications of COMS1 Symbol Terminal
   On SED1220, pad layout of COMS1 symbol terminal can be changed. COMS1 pad layout can be selected on your request.

	Standard	Optional
Pad No	Pad Name	Pad Name
65	COMS1	COM1
66	COM1	COM2
67	COM2	COM3
68	COM3	COM4
69	COM4	COM5
70	COM5	COM6
71	COM6	COM7
72	COM7	COM8
73	COM8	COMS1

SED1225 Series
LCD Controller/Drivers

Technical Manual

Contents

OUTLINE

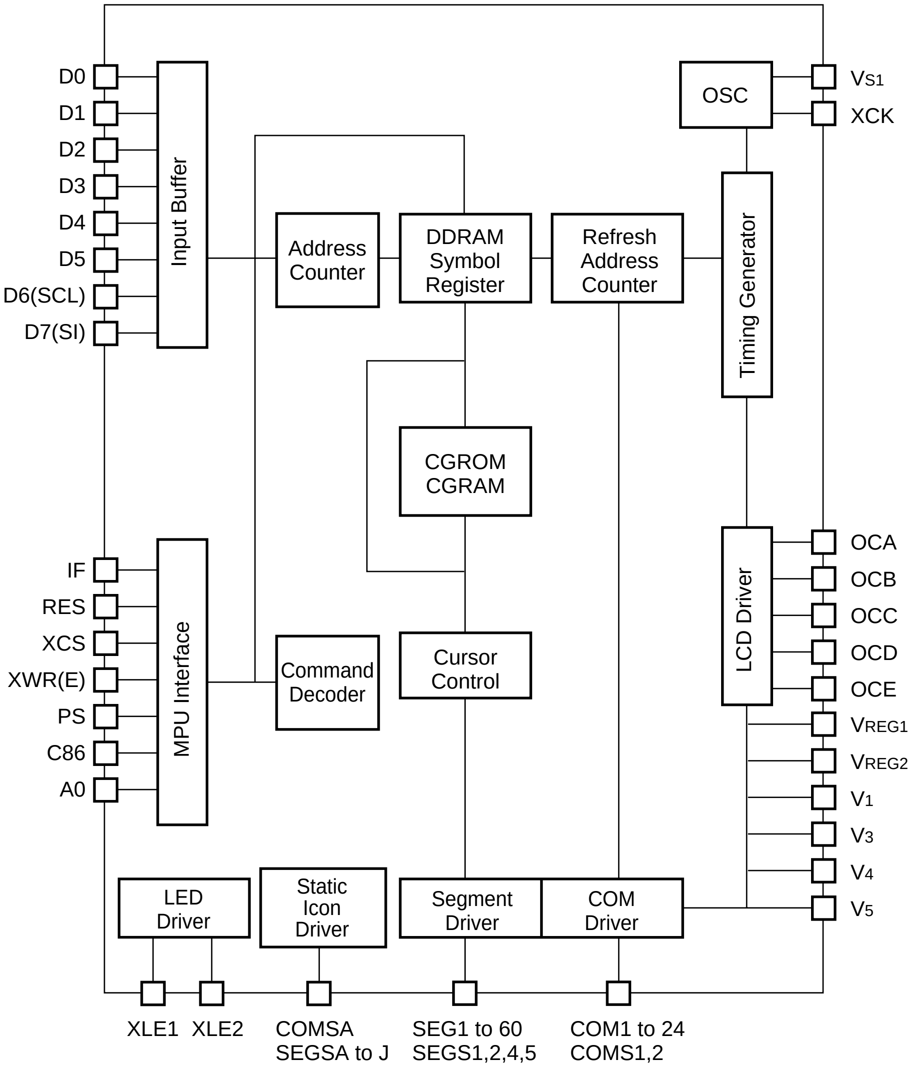
The SED1225 dot-matrix LCD Controller Driver receives 4-bit, 8-bit, or serial data from the microprocessor and displays up to 36 characters, four user-defined characters, and up to 120 symbols.
Up to 256 types of built-in character generator ROMs are provided. Each character font has a 5×8-dot structure. Also, the user-defined character RAM contains four 5×8-dot characters. In addition, a symbolic register can be used for flexible symbol display. The Driver featuring the very low power consumption can drive a handy terminal unit in either Sleep or Standby mode with the minimum power consumption.

FEATURES

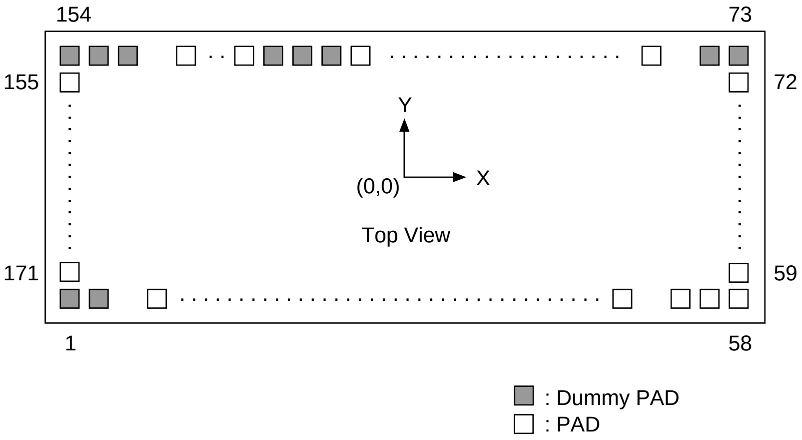
- Built-in display data RAM
  Can display up to 36 characters, 4 user-defined characters, and 120 symbols.
- Built-in CGROM (for 256-character display), CGRAM (for 4-character display), and symbol register (for 120 symbol display)
- No. of display columns by lines
  Normal mode: (12 columns plus 4 signal segments) × 3 line + 120 symbols + 10 static symbols
  Standby mode: 10 static symbols
- Built-in C&R oscillators
- Available external clock input
- High-speed MPU interfaces
  Interface to both 68- and 80-series MPUs
  Support of 4/8-bit interface
- Support of serial interface
- Character font: 5x8 dots
- Duty ratio: 1/18, 1/26
- Simple command setup
- Built-in LCD drive power circuit: Power amp and regulator
- Built-in electronic controls
- Very low power consumption
  30 µA (including the operating current of the built-in power supply during normal operation)
  10 µA (Static icon display during Standby operation
  5 µA (Display off during Sleep operation)
- Power supplies
  $V_{DD} – V_{SS}$: –1.7 to –3.6 V
  $V_{DD} – V_5$: –3.0 to –6.0 V
- Wide operating temperature range: Ta=-30 to +85°C
- CMOS process
- Package design
  Chip (with gold bump): SED1225D✱B
  TCP: SED1225T✱✱
- This IC package is not designed to have a radiation or strong light resistance.

SED1225 Series

BLOCK DIAGRAM



PIN ASSIGNMENT



SED1225D**
↑
CGROM pattern version number

Chip size: 7.85 × 1.97 mm
Pad pitch: 90 µm (min)
Chip thickness (Reference): 625 µm

Au bump specifications
Bump size:
Pad Nos. 59 to 72, and 155 to 171: 78 µm × 59 µm
Pad Nos. 1 to 58, and 73 to 154: 59 µm × 78 µm
Bump height (Reference): 22.5 µm

Pad coordinates (1/2)

PAD		Coordinate	
No.	Name	X	Y
1	Dummy	-3768	-822
2	Dummy	-3678	-822
3	A0	-3349	-822
4	XWR(E)	-3200	-822
5	XCS	-3050	-822
6	D7(SI)	-2901	-822
7	D6(SCL)	-2751	-822
8	D5	-2602	-822
9	D4	-2452	-822
10	D3	-2303	-822
11	D2	-2153	-822
12	D1	-2004	-822
13	D0	-1854	-822
14	XLE1	-1705	-822
15	XLE1	-1615	-822
16	XLE2	-1466	-822
17	XLE2	-1376	-822
18	V_{DD}	-1286	-822
19	V_{DD}	-1197	-822
20	V_{SS}	-1107	-822
21	V_{SS}	-1017	-822
22	V_5	-868	-822
23	V_5	-778	-822
24	V_4	-629	-822
25	V_4	-539	-822
26	V_3	-389	-822
27	V_3	-300	-822
28	V_1	-150	-822
29	V_1	-60	-822
30	(V_{REG1})	89	-822
31	(V_{REG1})	179	-822
32	V_{REG2}	328	-822
33	V_{REG2}	418	-822
34	OCA	567	-822
35	OCA	657	-822
36	OCB	807	-822
37	OCB	896	-822
38	OCC	1046	-822
39	OCC	1136	-822
40	OCD	1285	-822
41	OCD	1375	-822
42	OCE	1524	-822
43	OCE	1614	-822

PAD		Coordinate	
No.	Name	X	Y
44	V_{SS}	1718	-822
45	V_{SS}	1808	-822
46	C86	1973	-822
47	PS	2122	-822
48	IF	2272	-822
49	RES	2421	-822
50	XCK	2571	-822
51	VS1	2720	-822
52	(FSA)	2893	-822
53	(FSB)	3065	-822
54	(FSC)	3237	-822
55	(FS3)	3409	-822
56	(V_{DD})	3589	-822
57	(V_{DD})	3678	-822
58	(V_{DD})	3768	-822
59	(FS2)	3758	-628
60	(FS1)	3758	-456
61	(FS0)	3758	-283
62	COMSA	3758	-179
63	COMS1	3758	-90
64	COM1	3758	0
65	COM2	3758	90
66	COM3	3758	179
67	COM4	3758	269
68	COM5	3758	359
69	COM6	3758	449
70	COM7	3758	538
71	COM8	3758	628
72	COMS1	3758	718
73	Dummy	3768	822
74	Dummy	3678	822
75	SEGS1	3409	822
76	SEGS2	3320	822
77	SEG1	3230	822
78	SEG2	3140	822
79	SEG3	3050	822
80	SEG4	2961	822
81	SEG5	2871	822
82	SEG6	2781	822
83	SEG7	2692	822
84	SEG8	2602	822
85	SEG9	2512	822
86	SEG10	2423	822

Pad coordinates (2/2)

PAD		Coordinate	
No.	Name	X	Y
87	SEG11	2333	822
88	SEG12	2243	822
89	SEG13	2153	822
90	SEG14	2064	822
91	SEG15	1974	822
92	SEG16	1884	822
93	SEG17	1795	822
94	SEG18	1705	822
95	SEG19	1615	822
96	SEG20	1526	822
97	SEG21	1436	822
98	SEG22	1346	822
99	SEG23	1256	822
100	SEG24	1167	822
101	SEG25	1077	822
102	SEG26	987	822
103	SEG27	898	822
104	SEG28	808	822
105	SEG29	718	822
106	SEG30	629	822
107	SEG31	539	822
108	SEG32	449	822
109	SEG33	359	822
110	SEG34	270	822
111	SEG35	180	822
112	SEG36	90	822
113	SEG37	1	822
114	SEG38	-89	822
115	SEG39	-179	822
116	SEG40	-268	822
117	SEG41	-358	822
118	SEG42	-448	822
119	SEG43	-538	822
120	SEG44	-627	822
121	SEG45	-717	822
122	SEG46	-807	822
123	SEG47	-896	822
124	SEG48	-986	822
125	SEG49	-1076	822
126	SEG50	-1165	822
127	SEG51	-1255	822
128	SEG52	-1345	822
129	SEG53	-1435	822

PAD		Coordinate	
No.	Name	X	Y
130	SEG54	-1524	822
131	SEG55	-1614	822
132	SEG56	-1704	822
133	SEG57	-1793	822
134	SEG58	-1883	822
135	SEG59	-1973	822
136	SEG60	-2062	822
137	SEGS4	-2152	822
138	SEGS5	-2242	822
139	Dummy	-2332	822
140	Dummy	-2422	822
141	Dummy	-2512	822
142	COM24	-2602	822
143	COM23	-2692	822
144	COM22	-2781	822
145	COM21	-2871	822
146	COM20	-2961	822
147	COM19	-3050	822
148	COM18	-3140	822
149	COM17	-3230	822
150	COM16	-3320	822
151	COM15	-3409	822
152	Dummy	-3589	822
153	Dummy	-3678	822
154	Dummy	-3768	822
155	COM14	-3758	718
156	COM13	-3758	628
157	COM12	-3758	538
158	COM11	-3758	449
159	COM10	-3758	359
160	COM9	-3758	269
161	COMS2	-3758	179
162	SEGSA	-3758	90
163	SEGSB	-3758	0
164	SEGSC	-3758	-90
165	SEGSD	-3758	-179
166	SEGSE	-3758	-269
167	SEGSF	-3758	-359
168	SEGSG	-3758	-449
169	SEGSH	-3758	-538
170	SEGSI	-3758	-628
171	SEGSJ	-3758	-718

PIN DESCRIPTION

Power Supply Pins

Pin Name	I/O	Description	No. of Pins
V_{DD}	Power supply	Connects to the logic power supply. This is common to the Vcc power pin of the MPU.	1
V_{SS}	Power supply	0V power pin connected to system ground (GND)	2
V_1, V_3 V_4, V_5	Power supply	Multi-level LCD drive power supplies. A capacitor is required for external stabilization.	4
V_{S1}	O	Output pin of oscillator (OSC) power voltage. A capacitor is required for stabilization.	1

Notes: Two V_{SS} pins are provided. As they are commonly connected inside the IC, an input into any V_{SS} can be used if power impedance is low. To have the enough noise resistance, however, the V_{SS} power input from each pin is recommended.

LCD Power Pins

Pin Name	I/O	Description	No. of Pins
V_{REG2}	O	Output pins of LCD voltage and amp source power supplies. A capacitor is required for stabilization.	1
OCA OCB OCC OCD OCE	O	A voltage capacitor pin. A capacitor is required for amplification.	5

LED Drive Terminal

Pin Name	I/O	Description	No. of Pins
XLE1 XLE2	O	An Nch open drain output terminal to drive the LED. Connects to the LED cathode.	2

System Bus Connector Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descrition</th><th>No. of Pins</th></tr>
<tr><td>D7(SI)
D6(SCL)
D5 to D0</td><td>I</td><td>An 8-bit input data bus to be connected to the standard 8- or 16-bit MPU data bus. Pins D7 and D6 function as the serial data and clock inputs respectively if PS is logical low.
<table>
<tr><th>PS</th><th>C86</th><th>IF</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3 to D0</th><th>XCS</th><th>A0</th><th>XWR</th></tr>
<tr><td>"L"</td><td>—</td><td>—</td><td>SI</td><td>SCL</td><td>OPEN</td><td>OPEN</td><td>OPEN</td><td>XCS</td><td>A0</td><td>—</td></tr>
<tr><td>"H"</td><td>"H"</td><td>"H"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>XCS</td><td>A0</td><td>E</td></tr>
<tr><td>"H"</td><td>"H"</td><td>"L"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>XCS</td><td>A0</td><td>E</td></tr>
<tr><td>"H"</td><td>"L"</td><td>"H"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>XCS</td><td>A0</td><td>XWR</td></tr>
<tr><td>"H"</td><td>"L"</td><td>"L"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>XCS</td><td>A0</td><td>XWR</td></tr>
</table>
Open : May be open. However, the potential is recommended to fix to have better noise-resistance characteristics.
- : May be high or low. However, the potential must be fixed.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, the most significant bit of MPU address bus is connected to identify data or command.
0: Indicates D0 to D7 are command.
1: Indicates D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>Initializes when RES is set to low. The system is reset at RES signal level.</td><td>1</td></tr>
<tr><td>XCS</td><td>I</td><td>A Chip Select signal. The address bus signal is decoded and entered.
This is valid when low.</td><td>1</td></tr>
<tr><td>XWR</td><td>I</td><td>- When an 80-series MPU is connected
Active low.
The WR signal of 80-series MPU is connected. The data bus signal is fetched at the rising edge of XWR signal.
- When a 68-series MPU is connected
Active high.
Used as an Enable Clock input of 68-series MPU. The data bus signal is fetched at the falling edge of XWR signal.</td><td>1</td></tr>
<tr><td>PS</td><td>I</td><td>A switching pin between serial data input and parallel data input.
<table>
<tr><th>P/S</th><th>Chip select</th><th>Data/Command</th><th>Data</th><th>Serial Clock</th></tr>
<tr><td>"H"</td><td>XCS</td><td>A0</td><td>D0 to D7</td><td>—</td></tr>
<tr><td>"L"</td><td>XCS</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>An interface data length select pin during parallel data input.
- 8-bit parallel input if IF=high
- 4-bit parallel input if IF=low
This pin is connected to V_{DD} or V_{SS} if PS=low.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>An MPU interface switch pin.
- 68-series MPU interface if C86=high
- 80-series MPU interface if C86=low
This pin is connected to V_{DD} or V_{SS} if PS=low.</td><td>1</td></tr>
<tr><td>XCK</td><td>I</td><td>An external clock input pin.
It must be fixed to high to use the internal oscillator.
To use an external clock input, turn the internal oscillator OFF by issuing the command.</td><td>1</td></tr>
</table>

LCD Driver Signals

Dynamic drive pins

Pin Name	I/O	Description	No. of Pins
COM1 to COM24	O	Common signal output pins (for character display)	24
COMS1, COMS2	O	Common signal output pins (for non-character display) COMS1, COMS2: Common outputs for symbol display	3
SEG1 to SEG60	O	Segment signal output pins (for character display)	60
SEGS1, 2 4, 5	O	Segment signal output pins (for non-character display) SEGS1, 2, 4, 5: Segment outputs for signal output	4

Note: As the same COMS1 signal is output at two pins, one of them must be used.

Static drive pins

Pin Name	I/O	Description	No. of Pins
COMSA	O	Common signal output pin (for icon display)	1
SEGSA, B C, D, E, F G, H, I, J	O	Segment signal output pin (for icon display)	10

Notes: We recommend to separate LCD panel electrodes of static drive pins from those of dynamic drive pins. If these patterns are closely located, the LCD and its electrodes may be deteriorated.

FUNCTION DESCRIPTION

MPU Interfaces

Interface type selection

The SED1225 can transfer data via the 4- or 8-bit data bus or via the serial data input (SI). The parallel or serial data input can be selected by setting the PS pin to high or low (see Table 1).

Table 1

PS	Type	XCS	A0	XWR	SI	SCL	D0 to D7
H	Parallel input	XCS	A0	XWR	–	–	D0 to D7
L	Serial input	XCS	A0	H, L	SI	SCL	–

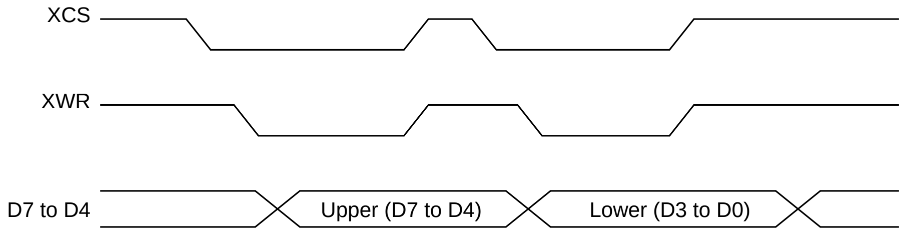
The SED1225 has the C86 pin for MPU selection. If the parallel input is selected (PS=high), if can be connected directly to the 80-series or 68-series MPU by setting the C86 pin to high or low (see Table 2). Also, the 8-bit or 4-bit data bus can be selected by the IF pin signal.

Table 2

C86 pin signal	Type	A0	XWR	XCS	D0 to D7
"L"	80 series	A0	XWR	XCS	D0 to D7
"H"	68 series	A0	E	XCS	D0 to D7

Interface to 4-bit MPU

If the 4-bit interface is selected (IF=low), the 8-bit command and data, and its address are transferred in two times.



Note: During continuous writing, the write time greater than the system cycle time (tcyc) must be set before the subsequent write operation.

Serial interface

The serial interface consists of an 8-bit shift register and a 3-bit counter. During chip select (XCS=low), an SI input and an SCL input can be accepted. During no chip select (XCS=high), the shift register and counter is initialized (reset).
Serial data of D7 to D0 are fetched in this order from the serial data input pin (SI) at the rising edge of serial clock. The data is converted into 8-bit parallel data at the rising edge of the eighth serial clock.
The serial data input (SI) is identified to have the display data or command by the A0 input. It is display data if A0=high, and it is command if A0=low.
The A0 input is fetched and identified at the rising edge of "8 × n-th" serial clock (SCL). Figure 1 shows a serial interface timing chart.
The SCL signals must be well protected from the far-end reflection and ambient noise due to increased line length. The operation checkout on the actual machine is recommended.
Also, we recommend to repeat periodical command writing and status refreshing to avoid a malfunction due to noise.

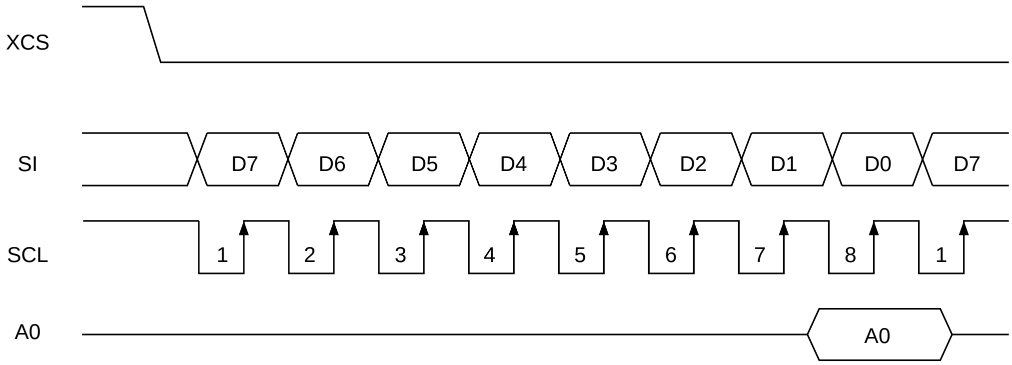


Figure 1

Data bus signal identification

The SED1225 identifies the data bus based on a combination of A0, AWR and E signals as defined on Table 3.

Table 3

Common	68 Series	80 Series	Function
A0	E	XWR	
1	1	0	Writes in the RAM and symbol register.
0	1	0	Writes (commands) in the internal register.

Chip Select

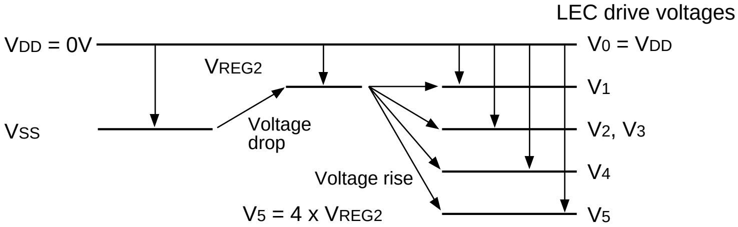
The SED1225 has an Chip Select pin (XCS) to allow an MPU interface input only if XCS=low.
During no chip select status, all of D0 to D7, A0, XWR, SI and SCL inputs are made invalid. If the serial input interface is selected, the shift register and counter are reset.
However, the Reset signal is entered independent from the XCS status.

Power Circuit

The built-in power circuit featuring the low power consumption generates the required LCD drive voltages. The power circuit consists of an amp and a voltage regulator.

Amp

When the capacitors are connected to the OCA, OCB, OCC, OCD, OCE, V_{REG2} pins, the LCD drive voltages are generated.
As the amp uses the signals from the oscillator, the oscillator or an external clock must be operating.
The following provides the potential relationship.



Voltage regulator

- Voltage regulator using the electronic control function
  Use the electronic control function and set the voltages appropriate to the LCD panel driving.
  When a 5-bit data is set in the electronic control register, one of 32-state voltages can be set for LCD driving. Before using the electronic control function, turn ON the power circuit by issuing the power control command.
  The following explains how to calculate the voltages using the electronic control function.

$V_5 = 4 \times V_{EV}$

Conditions:

$V_{EV} = V_{REG2} - X$

where,

$X = n\alpha$ (n=0, 1, ..., 31)

$\alpha = V_{REG2}/95$

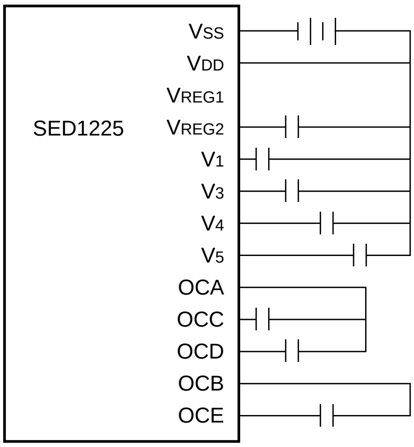
No.	Electronic control register	X	V_5
0	(0, 0, 0, 0, 0)	0	Large
1	(0, 0, 0, 0, 1)	1α	•
2	(0, 0, 0, 1, 0)	2α	•
3	(0, 0, 0, 1, 1)	3α	•
•	•	•	•
•	•	•	•
30	(1, 1, 1, 1, 0)	n-1α	•
31	(1, 1, 1, 1, 1)	nα	Small

This is reference voltage for the liquid crystal drive power circuit. The V_{REGZ} has a temperature characteristics of about –0.05%/deg.

External unit connection examples

An external voltage regulation capacitor must be connected to the LCD power pin. The LCD drive voltages are fixed to 1/4 biasing.

1/4 bias example



Note: We recommend to display the capacitance appropriate to the LCD panel size and set up the capacitance by observing the drive signal waveforms.

Reference set value: (0.1~1.0 µF)

Power Save mode

The SED1225 supports the Standby and Sleep modes to save the power consumption during system idling.

- Standby mode
  The Standby mode is selected or released by the Power Save command. During Standby mode, only the static icon is displayed.
  1. LCD display outputs
     COM1 to COM16, COMS1, COMS2:
     V_{DD} level
     SEG1 to SEG60, SEGS1, 2, 4, 5:
     V_{DD} level
     SEGSA, B, C, D, E, F, G, H, I, J, COMSA:
     Can light by static drive
     Use the Static Icon RAM to display the static icon with SEGSA, B, C, D, E, F, G, H, I, J and COMSA.
  2. DDRAM, CGRAM and symbol register
     Their write contents do not change. The contents are kept regardless of Standby mode selection or release.
  3. The operation mode before selection of Standby mode is kept.
     The internal circuits for dynamic display are stopped.
  4. Oscillator
     The oscillator must be turned ON for static display.
- Sleep mode
  To select the Sleep mode, turn OFF the power circuit and oscillator by issuing the command, and clear all data of Static Icon register to zero. Then, issue the Power Save command. The system power consumption will be minimized to almost the stopped status.
  1. LCD display outputs
     COM1 to COM16, COMS1, COMS2:
     V_{DD} level
     SEG1 to SEG60, SEGS1, 2, 4, 5:
     V_{DD} level
     SEGSA, B, C, D, E, F, G, H, I, J, COMSA:
     Clear all data of Static Icon register to zero.
  2. DDRAM, CGRAM and symbol register
     Their write contents do not change. The contents are kept regardless of Standby mode selection or release.
  3. The operation mode before selection of Standby mode is kept.
     All internal circuits are stopped.
  4. Oscillator
     Turn OFF the built-in power supply and oscillator by issuing the Power Save and power control commands.

Reset Circuit

When the RES input is made active, this LSI is initialized.

- Initialization status
  - (1) Display ON/OFF control
    - C=0: Cursor off
    - B=0: Blink off
    - DC=0: Normal display
    - D=0: Display off
  - (2) Power save
    - O=0: Oscillating circuit off
    - PS=0: Power save off
  - (3) Power control
    - P=0: Power circuit off
  - (4) System set
    - N=0: 3 lines
    - S2, S1=0: Direction of normal display
    - CG=0: CGRAM unused
  - (5) Electronic control
    - Address: 28H
    - Data: (0,0,0,0,0)
  - (6) Static icon
    - Address: 20H to 23H
    - Data: (0,0,0,0,0)
  - (7) LED register
    - Address: 2AH
    - Data: (0,0,0,0,0)
  - (8) CG RAM, DD RAM and symbol register
    - Address: 00H to 1FH, 30H to 7CH
    - Data: Must be initialized by MPU after reset input because of being indefinite.

Connect the RES terminal to the MPU reset terminal as described in “6-1 MPU Interface”, and execute initialization simultaneously with the MPU. However, if the MPU bus and port are put into high impedance for a certain time period by resetting, perform reset input to the SED1225 after the input to the SED1225 has been determined. When the RES terminal becomes “L”, each register is cleared and the above setup is established. If initialization by the RES terminal is not performed when power voltage is applied, resetting may be disabled.

COMMAND

Table 4 lists the supported commands. The SED1225 identifies a data bus by a combination of A0, XWR and E signals. It features high-speed processing as the commands are analyzed and executed in the internal timing only.

- Command outline

Table 4

Command type	Command name	A0	XWR
Display control instruction	Cursor Home	0	0
	Display On/Off Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
System setup	System Setup	0	0
Address control instruction	Address Setup	0	0
Data input instruction	Data Write	1	0

As the execution time of each instruction depends on the internal processing time of the SED1225, an enough time greater than the system cycle time (tcyc) must be assigned for continuous instruction execution.

- Explanation of commands
  (1) Cursor Home
  The Cursor Home command presets the Address counter to 30H, and shifts the cursor to column 1 of line 1 if Cursor Display is ON.

A0 XWR D7 ——— D0

A0	XWR	D7							D0
0	0	0	0	0	1	✻	✻	✻	✻

✻ : Don’t Care

  (2) Display On/Off Control
  The Display On/Off Control command sets the LCD character and cursor display.

A0 XWR D7 ——— D0

A0	XWR	D7							D0
0	0	0	0	1	1	C	B	DC	D

✻ : Don’t Care

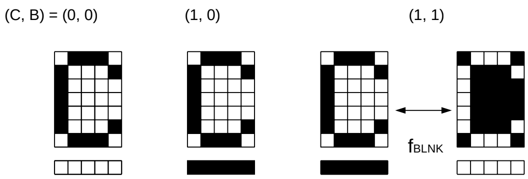
D=0: Turns the display off.
D=1: Turns the display on.
DC=0: Selects the standard size display.
DC=1: Selects the double-height vertical display.
B=0: Turns cursor blinking off.
B=1: Turns cursor blinking on.

During blinking, the cursor character is alternately displayed normally and reversely. The normal and reverse display is repeated approximately every one second.

C=0: Does not display the cursor.
C=1: Displays the cursor.

The following provides the relationship between the C and B registers and cursor display.

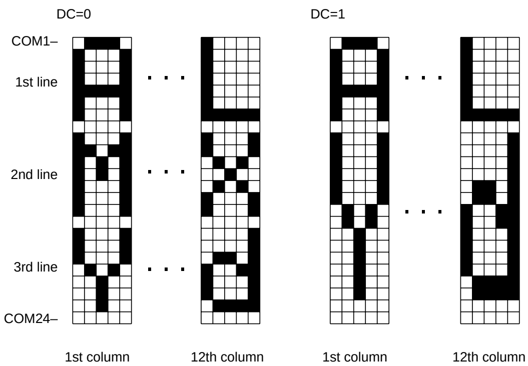
C	B	Cursor display
0	0	Not displayed
0	1	Not displayed
1	0	Underbar cursor
1	1	Alternate character display normally and reversely



The cursor display position is indicated by the address counter. Accordingly, to move the cursor, change the address counter value by automatic increment by writing the RAM address set command or RAM data.

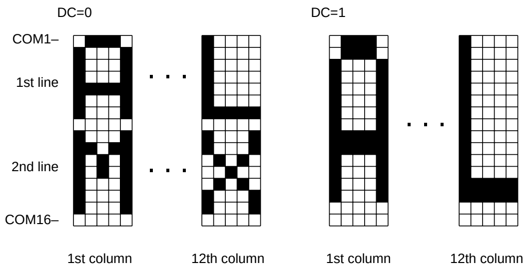
The following shows the relationship between the DC resistor and display:

(1) N=0 (1/26 duty)



The character on the 3rd line will be displayed in double size on the second and third lines by setting DC=1.

(2) N=1 (1/18 duty)



The character on the 1st line will be displayed in double size on the first and second lines by setting DC=1.

(3) Power Save
The Power Save command controls the oscillator and sets or releases the Sleep mode.

A0	XWR	D7							D0
0	0	0	1	0	0	✻	✻	O	PS

✻ : Don't Care

PS=0: Turns the Power Save on. (Release)
PS=1: Turns the Power Save off. (Select)
O=0: Turn the oscillator off. (Stop oscillation)
O=1: Turns the oscillator on. (Oscillation)

(4) Power Control
The Power Control command controls the built-in power circuit operations.

A0	XWR	D7							D0
0	0	0	1	0	1	0	0	0	P

✻ : Don't Care

P=0: Turns the power circuit off.
P=1: Turns the power circuit on.
Note: The oscillator must be operating to operate the voltage amp.

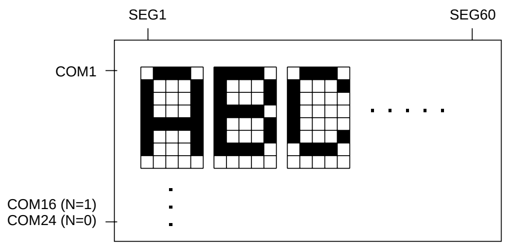
(5) System Reset
The System Reset command sets the display direction, the display line, and the use or no use of CGRAM. This command must first be executed after the power-on or reset.

A0	XWR	D7							D0
0	0	0	1	1	0	N	S2	S1	CG

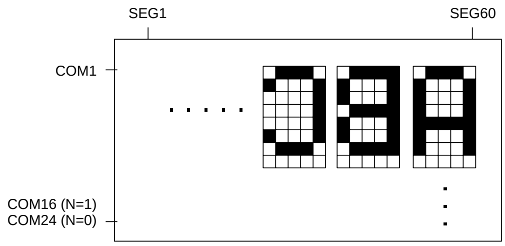
✻ : Don't Care

N=0: Displays 3 lines. (1/26 duty)
N=1: Displays 2 lines. (1/18 duty)
S2=0: Normal display
S2=1: Right and left reverse display
S1=0: Normal display
S1=1: Top and bottom reverse display
CG=0: Does not use the CGRAM.
CG=1: Uses the CGRAM.

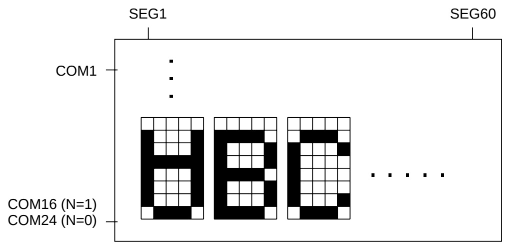
(1) Normal display



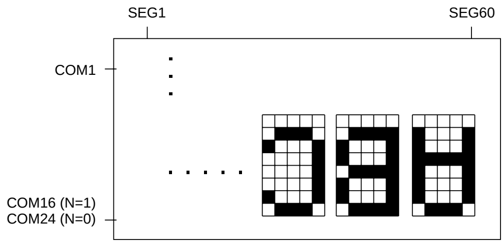
(2) Horizontal flipping



(3) Vertical flipping



(4) Horizontal vertical flipping



(6) RAM Address Setup

The RAM Address Setup command sets an address into the Address counter to write data into DDRAM, CGRAM and Symbol register.
When the cursor display is ON, the cursor is located at a position corresponding to the DDRAM address set by this command.

A0	XWR	D7 — D0
0	0	1 ADDRESS

✻ : Don't Care

① The 00H to 7FH address length can be set. To write data in the RAM, set the data write address by this command. When the subsequent data is written continuously, the address is automatically incremented.

RAM map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	CGRAM (00H)								CGRAM (01H)							
10H	CGRAM (02H)								CGRAM (03H)							
20H	SI1		SI2		Unused				EV	TEST	LED	Unused				
30H	DDRAM line 1									For signals →				Unused		
40H	DDRAM line 2									→				Unused		
50H	DDRAM line 3									→				Unused		
60H	Symbol register													Unused		
70H	Symbol register													Unused		

SI : Static Icon register
EV : Electronic Control register
TEST : Test register
(Do not use in normal operations.)
LED : LED register
For signals : SEGS1, 2, 4, 5
Symbol register : COMS1, COMS2

(7) Data Write

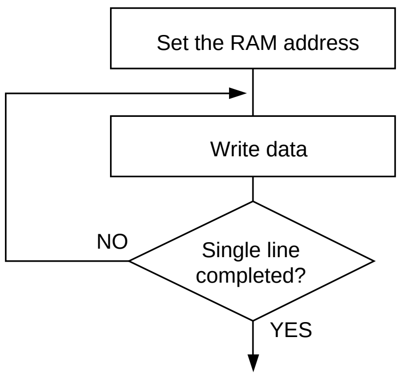
A0	XWR	D7 — D0
1	0	DATA

✻ : Don't Care

① This command writes data in the DDRAM, CGRAM or Symbol register.
② When this command is executed, the Address counter is incremented by 1 automatically. This allows continuous data writing.

Data write example:

The following gives an example to write a single line of data continuously.



Note: Assign an enough time greater than "tcyc" before executing the next instruction.

SED1225 Series

Table 4 SED1225 command list

Command	Code										Function
	A0	XWR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Shifts the cursor to its home position.
(2) Display On/Off Control	0	0	0	0	1	1	C	B	DC	D	Turns on or off the cursor, cursor blinking, double-size display, and data display. C=1: Cursor ON; C=0: Cursor OFF B=1: Blinking ON; B=0: Blinking OFF DC=1: Double-size display; DC=0: Normal display D=1: Display ON; D=0: Display OFF
(3) Power Save	0	0	0	1	0	0	*	*	0	PS	Turns on or off the Power Save mode and oscillator. PS=1: Power Save ON; PS=0: Power Save OFF O=1: OSC ON; O=0: OSC OFF
(4) Power Control	0	0	0	1	0	1	0	0	0	P	Turns on or off the built-in power circuit and voltage follower capacity, and sets the amp frequency. P=1: Power circuit ON; P=0: Power circuit OFF
(5) System Reset	0	0	0	1	1	0	N	S2	S1	CG	Sets the use or no use of CGRAM and the display direction. N=1: 3-line display; N=0: 2-line display CG=1: Use of CGRAM; CG=0: No use of CGRAM S2=0, S1=0: Normal display S2=0, S1=1: Top and bottom reverse display S2=1, S1=0: Right and left reverse display S2=1, S1=1: 180-degree rotation display
(6) RAM Address Setup	0	0	1	ADDRESS							Sets an address of DDRAM, CGRAM or Symbol register.
(7) RAM Write	1	0	DATA								Writes data in the DDRAM, CGRAM or Symbol register.
(8) NOP	0	0	0	0	0	0	0	0	0	0	This is a non-operation command.
(9) Test Mode	0	0	0	0	0	0	*	*	*	*	This is an IC chip test command. Do not use in normal operations.

BUILT-IN MEMORIES

Character Generator ROM (CGROM)

The SED1225 contains up to 126 types of CGROMs. Each character has a 5×8-dot structure.
Tables 5 to 8 defines the SED1225D✽✽ character codes. Four characters (00H to 03H) of character codes are used for the CGROM or CGRAM by the System Setup command.

The SED1225's CGROM is a mask ROM and it can be used as a custom CGROM. Consult to our sales agency for details.
The CGROM versions are identified as follows:
Example: SED1225D0B
↑
CGROM pattern ID

Table 5 SED1225DAB

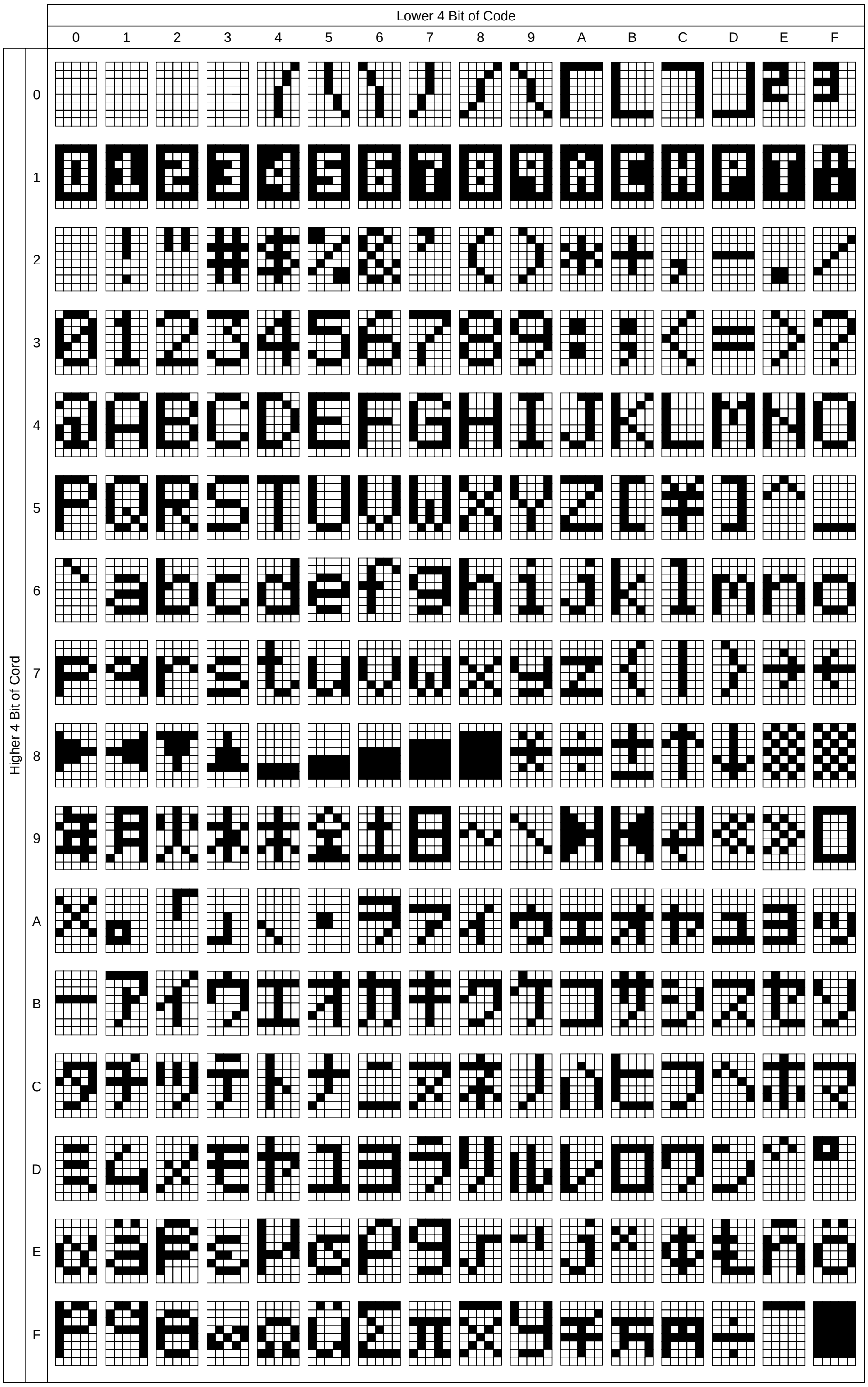


Table 6 SED1225DBB

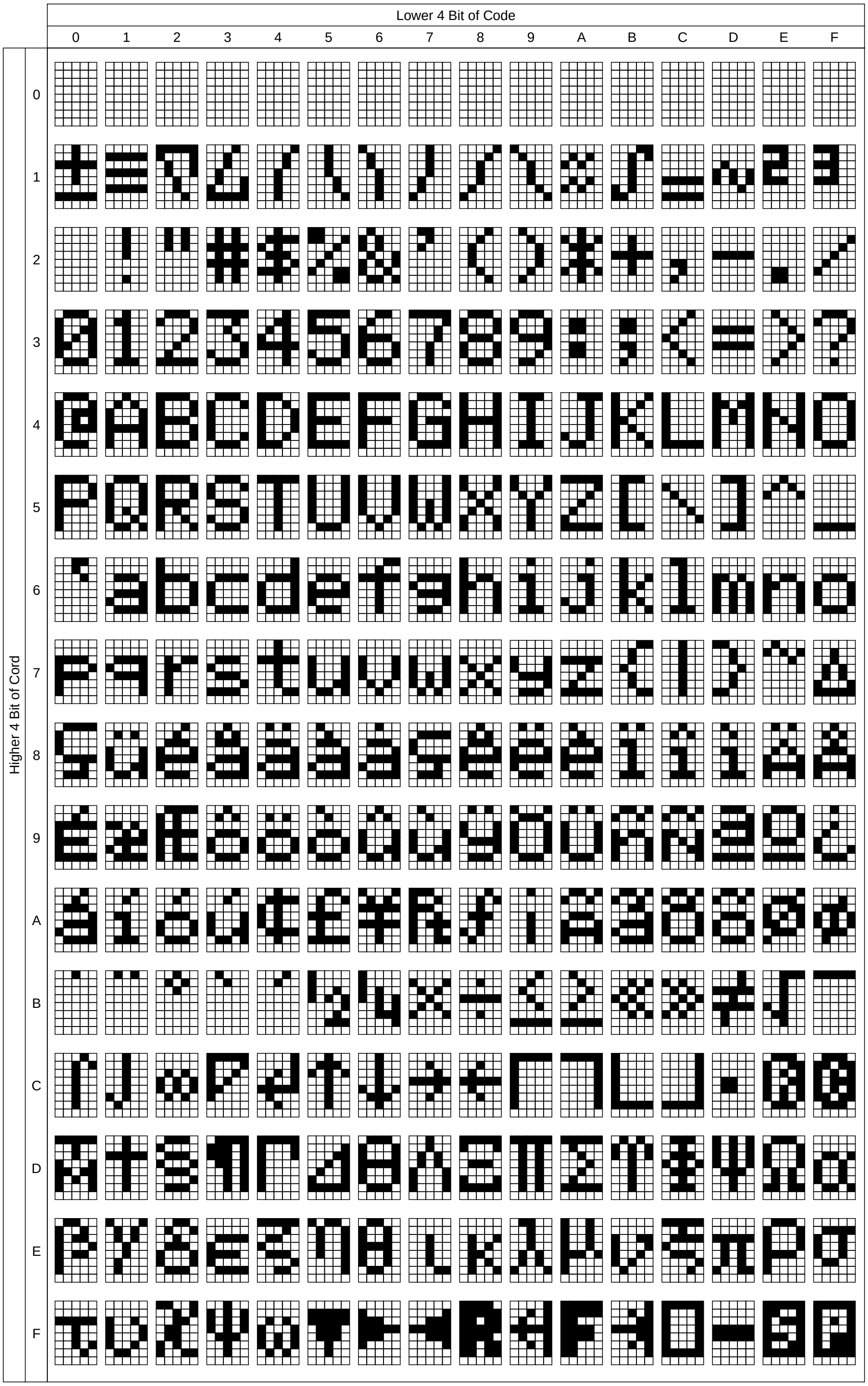
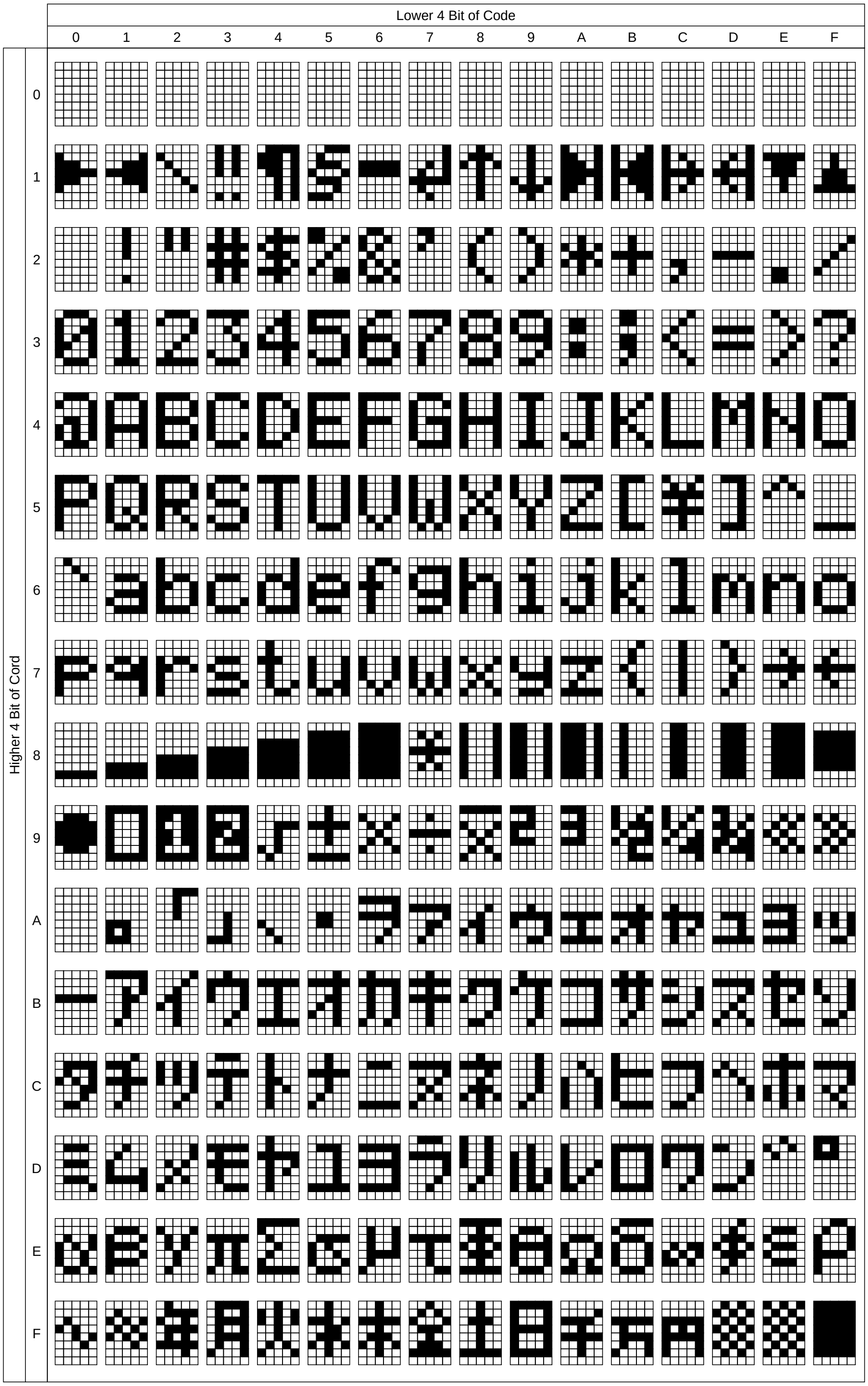


Table 7 SED1225DGB



Character Generator RAM (CGRAM)

The SED1225 has a built-in CGRAM to program user-defined character patterns for highly flexible signal and character display.
Issue the System Setup command to use the CGRAM. The CGRAM has the 160-bit storage capacity, and it can store up to four 5×8-dot character patterns.
The following provides the relationship between CGRAM character patterns and CGRAM addresses and character codes.

Character Code	RAM Address		CGRAM Data D7							D0	Character Display SEG	Signal Display SEGS 1 2	4 5
00H	00H to 07H	0	✻	✻	✻	0	1	1	1	1	□■■■■	□■	■■
		1	✻	✻	✻	1	0	0	0	0	■□□□□	■□	□□
		2	✻	✻	✻	1	0	0	0	0	■□□□□	■□	□□
		3	✻	✻	✻	0	1	1	1	1	□■■■■	□■	■■
		4	✻	✻	✻	0	0	0	0	1	□□□□■	□□	□■
		5	✻	✻	✻	0	0	0	0	1	□□□□■	□□	□■
		6	✻	✻	✻	1	1	1	1	0	■■■■□	■■	■□
		7	✻	✻	✻	0	0	0	0	0	□□□□□	□□	□□
01H	08H to 0FH	8	✻	✻	✻	0	0	1	0	0	□□■□□	□□	□□
		9	✻	✻	✻	0	0	1	0	0	□□■□□	□□	□□
		A	✻	✻	✻	0	1	1	1	0	□■■■□	□■	■□
		B	✻	✻	✻	0	1	1	1	0	□■■■□	□■	■□
		C	✻	✻	✻	0	1	1	1	0	□■■■□	□■	■□
		D	✻	✻	✻	1	1	1	1	1	■■■■■	■■	■■
		E	✻	✻	✻	1	1	1	1	1	■■■■■	■■	■■
		F	✻	✻	✻	0	0	0	0	0	□□□□□	□□	□□

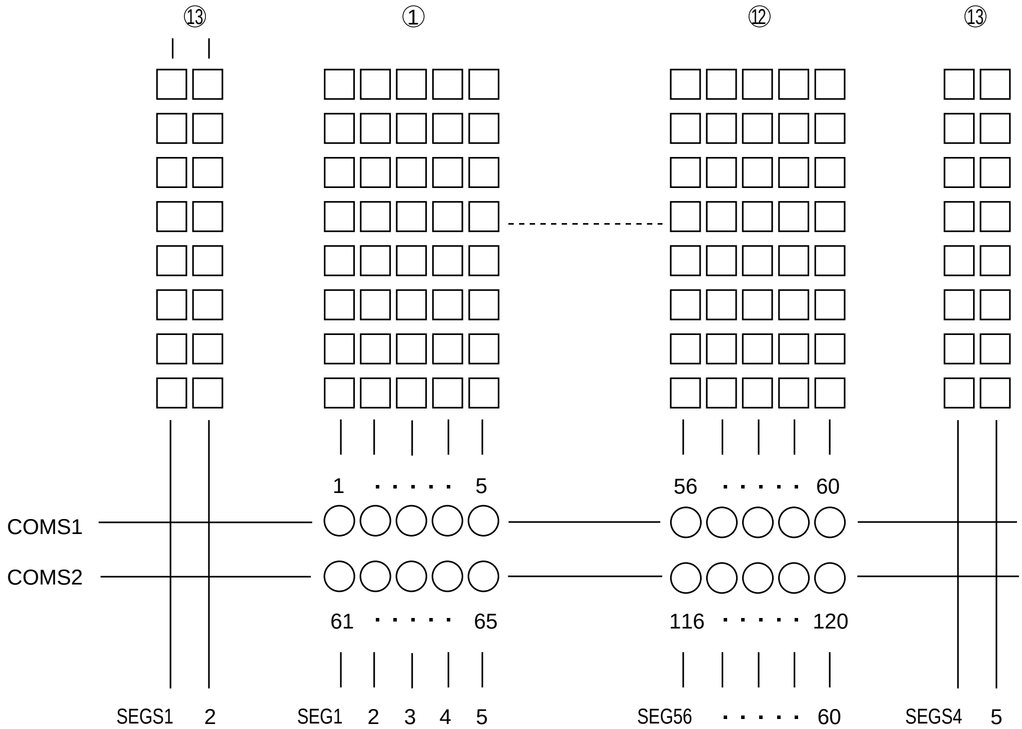
D7 to D5: Un used
D4 to D0: Character data (1 for display; 0 for no display)

The 5×8-dot character size can also be set. To do so, use the *7H and *FH RAM addresses. However, the *7H and *FH data is reversed if the underbar cursor is used.

Symbol Register

The SED1225 has a built-in Symbol register to allow separate symbol setup on the display panel.
The Symbol register has the 120-bit storage capacity, and it can display 120 symbols. Also, the SED1225 contains a Blink register for every 5-dot blinking.

The following provides the relationship between the Symbol register display patterns, RAM addresses and write data.



RAM Address		Corresponding symbol bits							
		D7	D6	D5	D4	D3	D2	D1	D0
60H to 6BH	0	✻	✻	BL1	1	2	3	4	5
	1	✻	✻	BL2	6	7	8	9	10
	:	:							
	B	✻	✻	BL12	56	57	58	59	60
70H to 7BH	0	✻	✻	BL13	61	62	63	64	65
	1	✻	✻	BL14	66	67	68	69	70
	:	:							
	B	✻	✻	BL24	116	117	118	119	120

BL1 to BL24: Blinking setup (0 for no blinking; 1 for blinking)

Note: If the symbol size is 1.5 times greater than other dots, we recommend to divide and drive the SEG* and COMS1 and COMS2 separately.

Static Icon RAM

The SED1225 has a built-in Static Icon RAM to display a static icon separately from the dynamic icon.
The Static Icon RAM has the 20-bit storage capacity, and it can display 10 icons. The following provides the relationship between the static icon functions and the static icon, RAM address and write data.

(SEGSA, B, C, D, E)

Function	RAM Address	Static Icon Data								Display
		D7							D0	SEGSA B C D E
Display ON/OFF	20H	*	*	*	0	0	1	1	1	□□■■■
Blink ON/OFF	21H	*	*	*	1	0	0	0	1	□□■■■ ⇕ f BLINK ■□■■□

(SEGSF, G, H, I, J)

Function	RAM Address	Static Icon Data								Display
		D7							D0	SEGSA B C D E
Display ON/OFF	22H	*	*	*	0	0	1	1	1	□□■■■
Blink ON/OFF	23H	*	*	*	1	0	0	0	1	□□■■■ ⇕ f BLINK ■□■■□

* : Unused
1 : Display or blinking
0 : No display or no blinking
f BLINK : 1 to 2Hz

Electronic Control RAM (Register)

The SED1225 has the electronic control functions to control LCD drive voltages and to adjust the LCD display density. One of 32-state LCD voltages can be selected when the 5-bit data is written in the Electronic Control RAM.

The following provides the relationship between the RAM address and write data by electronic control setup.

Function	RAM Address	Electronic Control Data D7							D0	Status	VEV
Electronic Control	28H	*	*	*	0	0	0	0	0	0	VREG-0
		*	*	*	0	0	0	0	1	1	VREG-α
		*	*	*	0	0	0	1	0	2	VREG-2α
						⋮				⋮	⋮
		*	*	*	1	1	1	0	1	29	VREG-29α
		*	*	*	1	1	1	1	0	30	VREG-30α
		*	*	*	1	1	1	1	1	31	VREG-31α
	29H	*	*	*	*	*					For test

* : Unused

α : α=VREG/95 (1/4biased)

Note: Do not use address 29H as it can be used for IC chip test only.

LED RAM (Register)

The SED1225 has the LED drive functions to drive the LCD by controlling the XLE1 and XLE2 pins.

The following provides the relationship between the RAM address and write data by LED register setup.

Function	RAM Address	LED Register Data D7				D3	D2	D1	D0
LED ON/OFF Timer	2AH	✻	✻	✻	✻	TIM2	TIM1	LED2	LED1

✻ : Unused

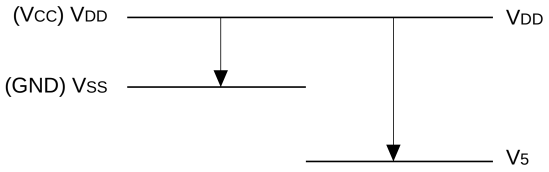
The following defines the XLE1 and XLE2 pin state depending on the TIM1, TIM2, LED1 and LED2 set values.

LED Register Set Value		Output Status (XLE1, XLE2)
TIM2 TIM1	LED2 LED1	
0	0	XLE = High impedance
0	1	XLE = Low
1	0	Keeps XLE low approximately 15 sec after input of Display ON command.
1	1	XLE = Low

Note: When this function is used, minimize power supply and power cable impedance to avoid IC misoperation due to large current.

MAXIMUM ABSOLUTE RATINGS

Item		Symbol	Rating	Unit
Power voltage (1)		V_{SS}	–0.6 to +0.3	V
Power voltage (2)		V_5	–7.0 to +0.3	V
Power voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		Topr	–30 to +85	°C
Storage temperature	TCP	Tstr	–55 to +100	°C
	Bare chip		–65 to +125	



Notes: 1. All voltages are referenced to V_{DD}=0 V.
2. The following voltage levels must always be satisfied:
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4$, and $V_{DD} \geq V_{SS} \geq V_5$
3. If the LSI is used beyond the maximum absolute rating, the LSI may be destroyed permanently. The LSI should meet the electric characteristics during normal operations. If not, the LSI may be malfunction or the LSI reliability may be lost.

DC CHARACTERISTICS

(V_{SS} = –3.6 to –1.7 V, Ta = –30 to +85°C unless otherwise noted.)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Pin
Power voltage (1)	Operable	V_{SS}	1/4 bias	–3.6	–3.0	–1.7	V	V_{SS}
			1/5 bias	–3.6	–3.0	–2.7		
	Data hold voltage			–3.6		–1.5		
Power voltage (2)	Operable	V_5		–6.0		–3.0	V	V_5
	Operable	V_1, V_2		0.5 × V_5		V_{DD}	V	V_1, V_2
	Operable	V_3, V_4		V_5		0.5 × V_5	V	V_3, V_4
"Hi" input voltage		V_{IHC}		0.2 × V_{SS}		V_{DD}	V	*2
"Lo" input voltage		V_{ILC}		V_{SS}		0.8 × V_{DD}	V	*2
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0		1.0	µA	*2
LCD driver ON resistance		R_{ON} (LCD)	Ta=25°C ΔV=0.1V; V_5=–5.0V		10	20	kΩ	COM, SEG *3
LED driver ON resistance		R_{ON} (LED)	V_{SS}=–3.0V I_{OL}=10mA		100		Ω	XLE1, XLE2
Static current consumption		I_{DDQ}			0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	During display	V_5 = –5V; No loading V_{SS}=–1.8V		20	30	µA	V_{DD} *4
		During display	V_5 = –5V; No loading V_{SS}=–3.0V		30	45	µA	V_{DD} *4
		During standby	OSC On; PWR off No loading; V_{SS}=–3.0V		10	15	µA	V_{DD}
		During sleep	OSC Off; PWR off No loading; V_{SS}=–3.0V		0.1	5	µA	V_{DD}
		During access	fcyc=200KHz V_{SS}=–3.0V		150	300	µA	V_{DD} *5
Input pin capacity		C_{IN}	Ta=25°C, f=1MHz		8.0	10.0	pF	*3

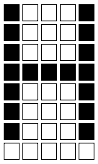
Frame frequency	f_{FR}	Ta = 25°C, V_{SS} = –3.0V	70	100	130	Hz	*8
External clock frequency	f_{CK}			33.8		kHz	*8, *9

Reset time	t_R		1.0			µs	*6
Reset pulse width	t_{RW}		10			µs	*6
Reset start time	t_{RES}		50			ns	*7

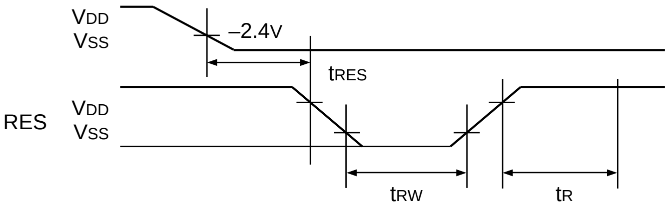
Dynamic system:

Built-in power supply	Amp output voltage	V_5	Ta = 25°C (during 1/4 bias)	4 × V_{REG2}			V	
	Reference voltage	V_{REG2}	Ta = 25°C (during 1/4 bias)	–1.55	–1.5	–1.45	V	

*1 Although the wide operating character range is guaranteed, a quick and excessive voltage variation may not be guaranteed during access by the MPU. The low-voltage data hold characteristics are valid during Sleep mode. No access by the MPU is allowed during this time.
*2 D0 to D5, D6 (SCL), D7 (SI), A0, RES, XCS, XWR (E), PS, IF, C86
*3 The resistance if a 0.1-volt voltage is supplied between the SEGn, SEGSn, COMn or COMSn output pin and each power pin (V_1, V_2, V_3 or V_4). It is defined within power voltage (2).
$R_{ON} = 0.1V/\Delta I$
where, ΔI is current that flows when the 0.1-volt voltage is supplied between the power supply and output.
*4 Applied if not accessed by the MPU during character display and if the built-in power circuit and oscillator are operating.
Display character:



*5 Current consumption if always written in “fcyc”. The current consumption during access is roughly proportional to the access frequency (fcyc).
*6 The “t_R” (reset time) indicates a time period from the rising edge of RES signal to the completion of internal circuit reset. Therefore, the SED1225 enters the normal operation status after “t_R”.
*7 Defines the minimum pulse width of RES signal. A pulse width greater than “t_{RW}” must be entered for reset.

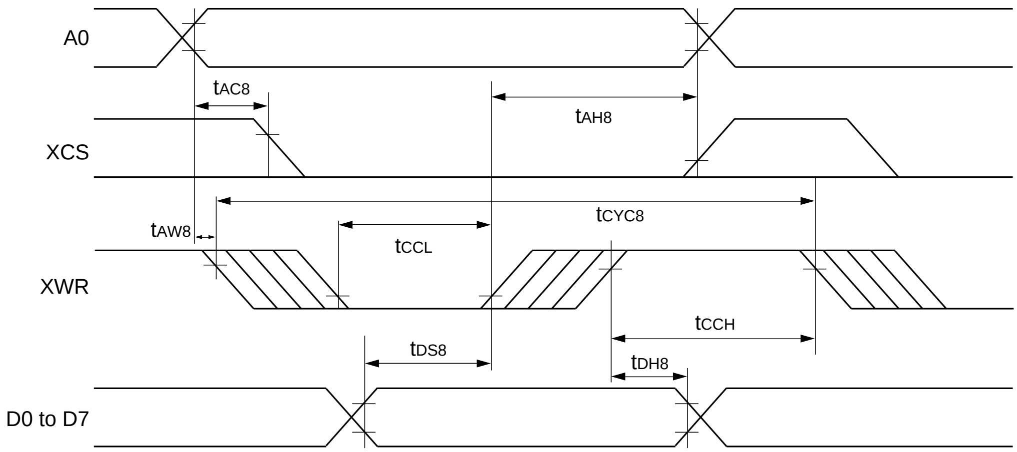


All signal timings are based on 20% and 80% of Vss.

*8 The following provides the relationship between the oscillator frequency (f_{OSC}) for built-in circuit driving and the frame frequency (f_{FR}).
$f_{OSC} = 13 \times 26 \times f_{FR}$ (3-line display)
$= 13 \times 18 \times f_{FR}$ (2-line display)
<Reference>
$f_{BLK} = (1/128) \times f_{FR}$
*9 Enter the waveforms in 40% to 60% duty to use an external clock instead of the built-in oscillator. If no external clock is entered, fix it to high. (Normal high)

SIGNAL TIMING CHARACTERISTICS

(1) MPU bus write timing (80 series)



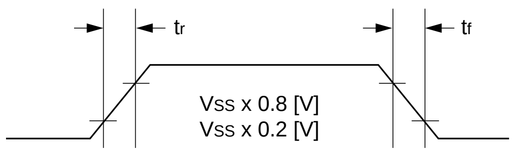
(Ta = –30 to +85°C, VSS = –3.6V to –1.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time XCS setup time	A0 XCS	t_{AW8} t_{AH8} t_{AC8}	All timing must be based on 20% and 80% of VSS.	60 30 0	— — —	ns
System cycle time	XWR	t_{CYC8}		1850	—	ns
Write "Lo" pulse width (XWR)		t_{CCL}		150	—	ns
Write "Hi" pulse width (XWR)		t_{CCH}		1650	—	ns
Data setup time Data hold time	D0 to D7	t_{DS8} t_{DH8}		50 50	— —	ns

(Ta = –30 to +85°C, VSS = –3.3V to –2.7V)

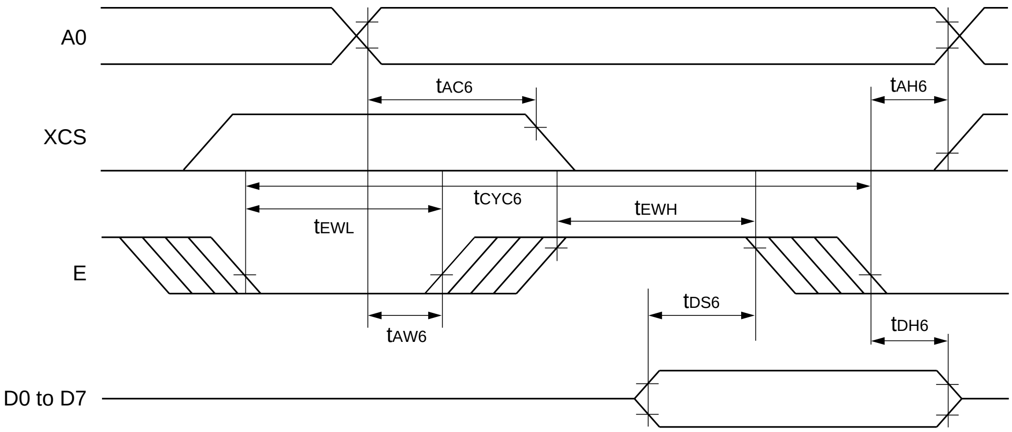
Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time XCS setup time	A0 XCS	t_{AW8} t_{AH8} t_{AC8}	All timing must be based on 20% and 80% of VSS.	60 30 0	— — —	ns
System cycle time	XWR	t_{CYC8}		1150	—	ns
Write "Lo" pulse width (XWR)		t_{CCL}		100	—	ns
Write "Hi" pulse width (XWR)		t_{CCH}		1000	—	ns
Data setup time Data hold time	D0 to D7	t_{DS8} t_{DH8}		20 20	— —	ns

*1 The input signal rise and fall times (t_r, t_f) are defined to be 25 nsec max (except for RES input).



*2 "t_{CCL}" is defined by the overlap time of XCS low level and XWR low level.

(2) MPU bus write timing (68 series)



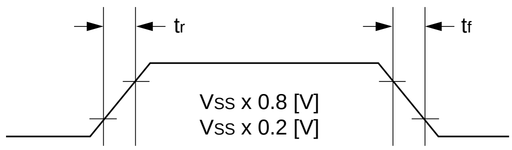
(Ta = –30 to +85°C, V_{SS} = –3.6V to –1.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time XCS setup time	A0 XCS	t_{AW6} t_{AH6} t_{AC6}	All timing must be based on 20% and 80% of V_{SS}.	60 50 0	– – –	ns
System cycle time	XWR	t_{CYC6}		1850	–	ns
Enable "Lo" pulse width (XWR)		t_{EWL}		1650	–	ns
Enable "Hi" pulse width (XWR)		t_{EWH}		150	–	ns
Data setup time Data hold time	D0 to D7	t_{DS6} t_{DH6}		20 80	– –	ns

(Ta = –30 to +85°C, V_{SS} = –3.3V to –2.7V)

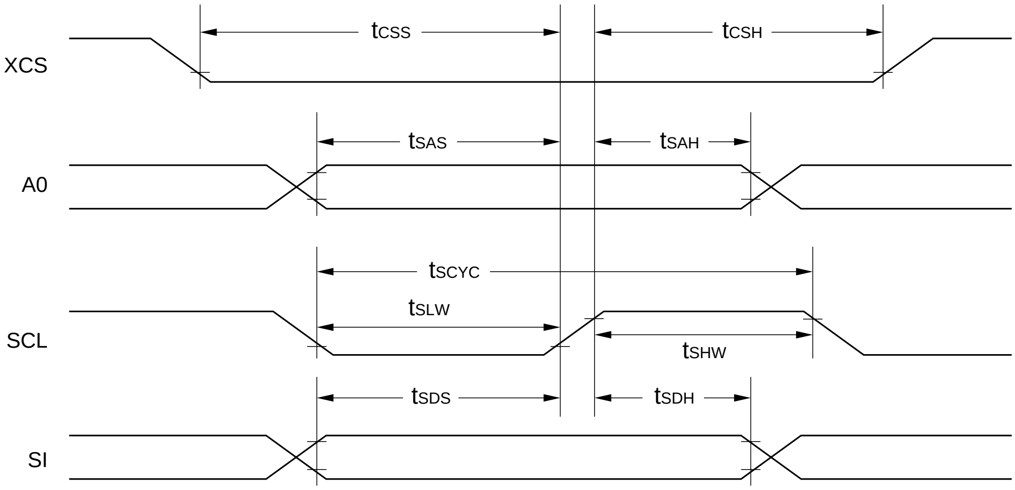
Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time XCS setup time	A0 XCS	t_{AW6} t_{AH6} t_{AC6}	All timing must be based on 20% and 80% of V_{SS}.	60 30 0	– – –	ns
System cycle time	XWR	t_{CYC6}		1150	–	ns
Enable "Lo" pulse width (XWR)		t_{EWL}		1000	–	ns
Enable "Hi" pulse width (XWR)		t_{EWH}		100	–	ns
Data setup time Data hold time	D0 to D7	t_{DS6} t_{DH6}		20 50	– –	ns

*1 The input signal rise and fall times (t_r, t_f) are defined to be 25 nsec max (except for RES input).



*2 "t_{EWH}" is defined by the overlap time of XCS low level and XWR low level.

(3) Serial interface



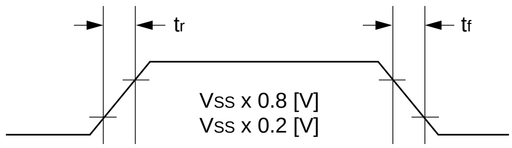
(Ta = –30 to +85°C, V_{SS} = –3.6V to –1.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
System clock cycle SCL "Hi" pulse width SCL "Lo" pulse width	SCL	t_{SCYC} t_{SHW} t_{SLW}	All timing must be based on 20% and 80% of V_{SS}.	3000 2850 150	— — —	ns
Address setup time Address hold time	A0	t_{SAS} t_{SAH}		50 800	— —	ns
Data setup time Data hold time	SI	t_{SDS} t_{SDH}		50 50	— —	ns
CS-to-SCL time	XCS	t_{CSS} t_{CSH}		400 2500	— —	ns

(Ta = –30 to +85°C, V_{SS} = –3.3V to –2.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
System clock cycle SCL "Hi" pulse width SCL "Lo" pulse width	SCL	t_{SCYC} t_{SHW} t_{SLW}	All timing must be based on 20% and 80% of V_{SS}.	1400 1300 50	— — —	ns
Address setup time Address hold time	A0	t_{SAS} t_{SDH}		50 500	— —	ns
Data setup time Data hold time	SI	t_{SDS} t_{SDH}		30 30	— —	ns
CS-to-SCL time	XCS	t_{CSS} t_{CSH}		200 1500	— —	ns

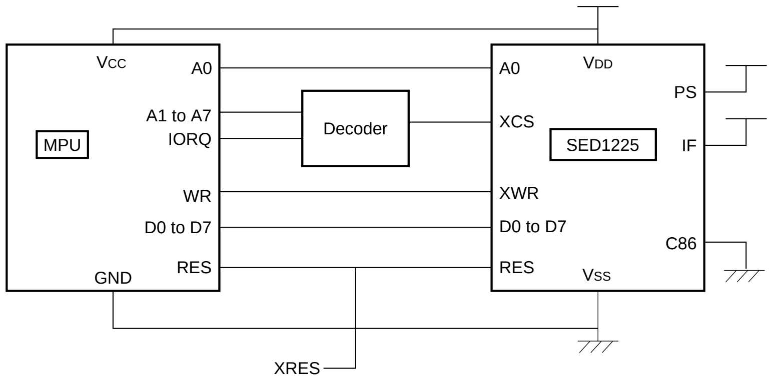
*1 The input signal rise and fall times (t_r, t_f) are defined to be 25 nsec max (except for RES input).



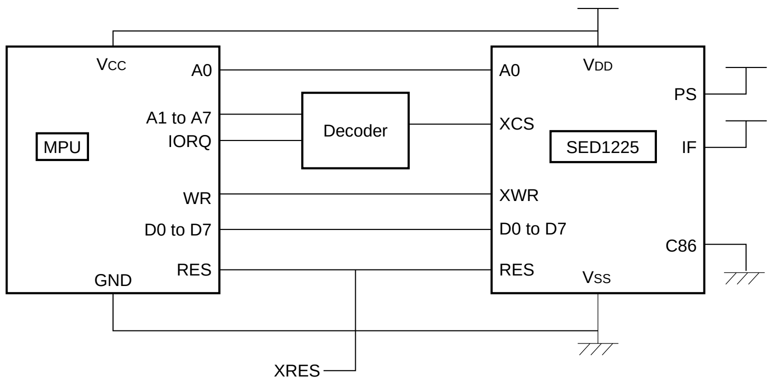
MPU INTERFACES (REFERENCE)

The SED1225 can be connected to the 80-series or 68-series MPU. Also, it can operate with a less number of signal lines via the serial interface.
If the MPU buses and ports are set to high impedance for a certain time due to RESET, the RESET signal must be entered in the SED1225 after the SED1225's inputs have been determined.

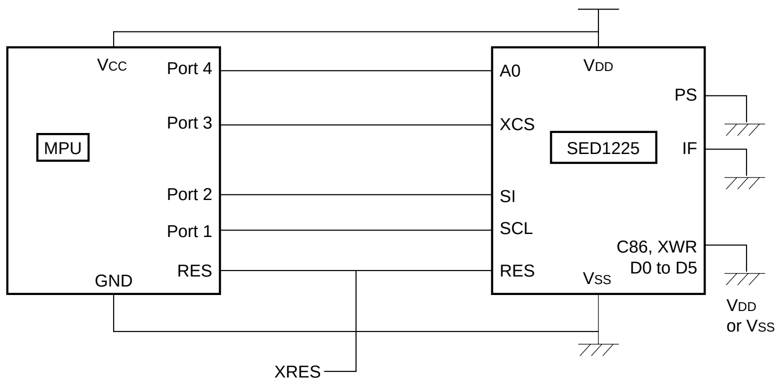
80-Series MPU



68-Series MPU

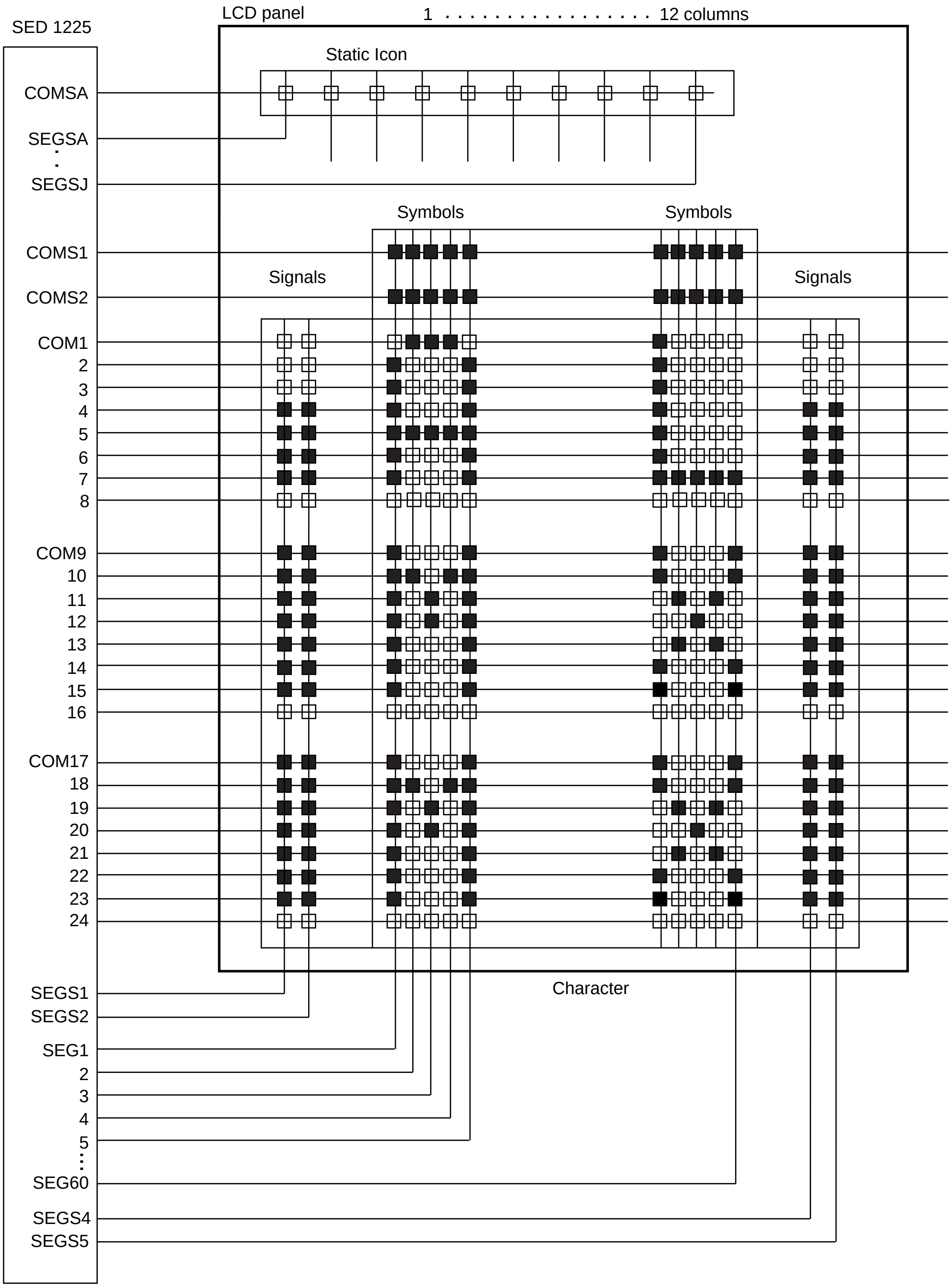


Serial Interface

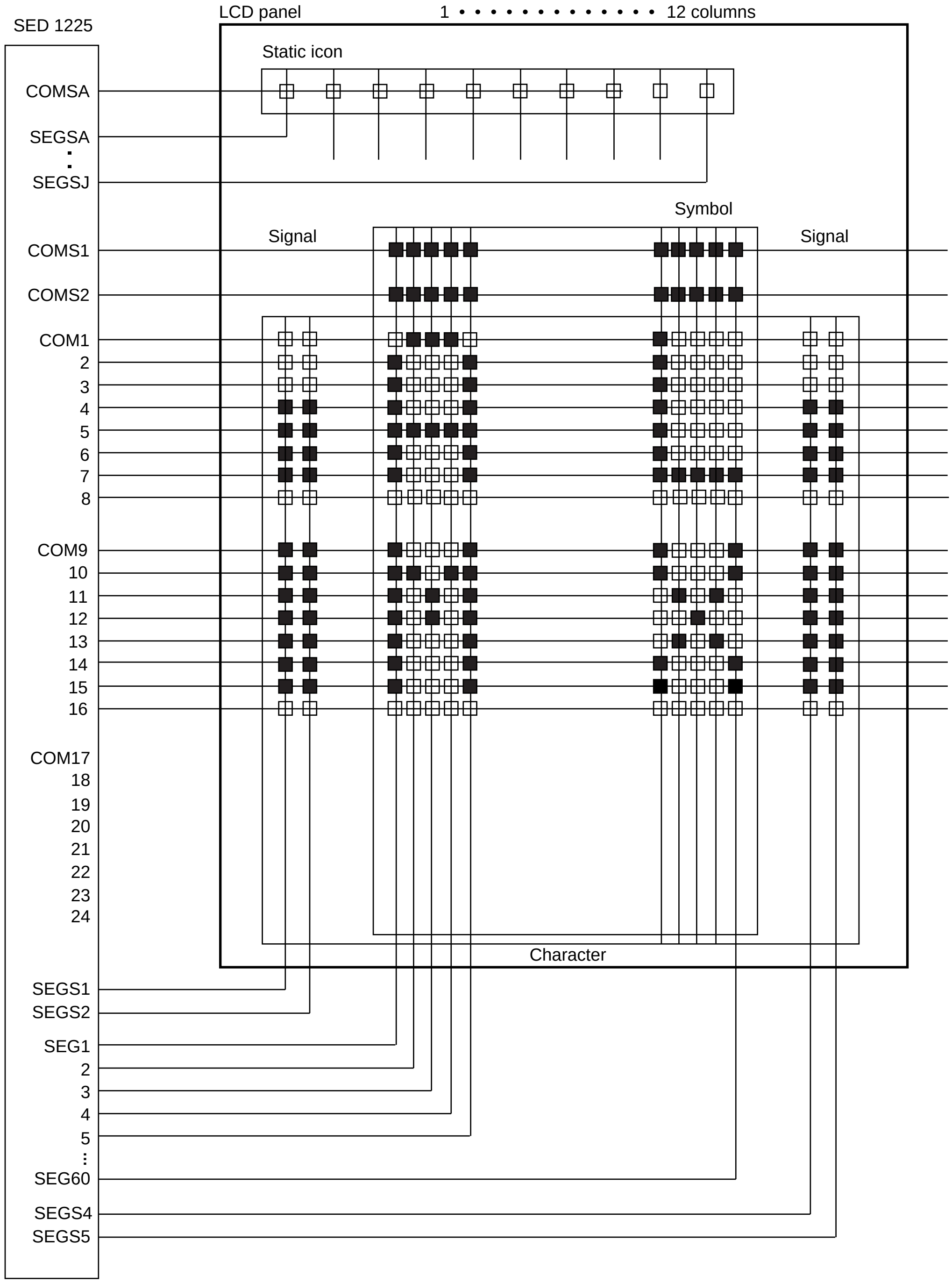


LCD CELL INTERFACE

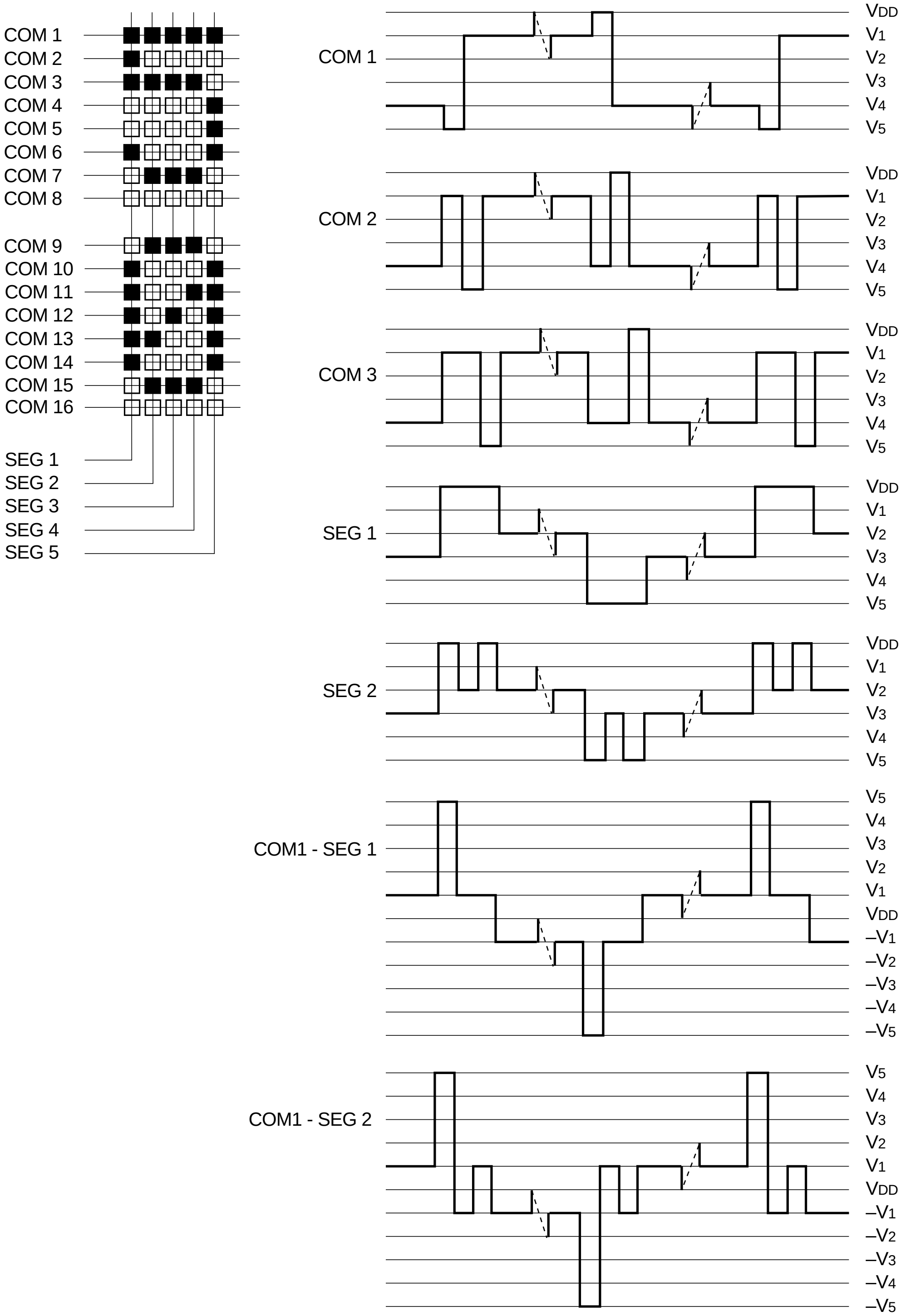
12 columns by 3 lines, 5×8 dots + Symbols



12 columns by 2 lines (N=1), 5×8 dots + Symbols



LCD DRIVE WAVEFORMS (B WAVEFORMS)



EXAMPLE OF INSTRUCTION SETUP (REFERENCE)

Initialization

VDD-VSS power on

↓

Power stable

↓

Reset input

↓

Command status
- Static display control - off
- Display on/off control - off
- Power save - off
- Power supply control - off
- System setup - 3-digit display, CGRAM unused. normal display
- Electronic volume - (0, 0, 0, 0, 0)
- Static icon - (0, 0, 0, 0, 0)

Others are undefined.

↓

Wait for 10 microseconds or more.

↓

Command input: asterisked items (*) are in no particular order.
<1> NOP command
<2> System setup command
* Electronic volume resistor set - Address 28H, data (*, *, *, *, *)
* Power save command - PS off (power save), O on (oscillation)
<5> Power supply control command - P on
<6> RAM address set (See Note 1)
<7> Data write (See Note 1)

↓

Wait for 20 microseconds or more. (See Note 2)

↓

Command input
<8> Display on/off command input - D on (display) (See Note 3)

↓

Data input
<9> Static icon control - Address 20H, 22H (See Note 3)
Data (*, *, *, *, *)
Address 21H, 23H (See Note 3)
Data (*, *, *, *, *)

↓

End of initialization

Display Mode

End of initialization

RAM address set input

RAM (data) write input

Display the written contents.

Standby Mode

(1) Setting the standby mode

End of initialization

Normal operation - Power save is cleared and oscillating circuit turns on.

<1> Display on/off control command input - D off (display)
<2> Power save command input - PS on (power save)
O on (oscillation)
<3> Power supply control command input - P off

Starts the standby mode.

Displays only the static icon.

(2) Clearing the standby mode

Standby mode

<1> Power save command input - PS off (power save)
O on (oscillation)
<2> Power supply control command inpu - P on
O on (oscillation)
- P off

Wait for 20 microseconds or more.

<3> Display on/off command input - D on (display)

Returns to normal operation (original state).

Sleep Mode

(1) Setting the Sleep mode.

End of initialization

↓

Normal operation
(Power save is cleared and oscillating circuit turns on.)

↓

<1> Display on/off control command input	- D off (display)	
<2> Power save icon control	- Address 20H, 22H Data (0, 0, 0, 0, 0)	(See Note 3)
	- Address 21H, 23H Data (0, 0, 0, 0, 0)	(See Note 3)
<3> Power save command input	- PS on (power save) O off (oscillating)	
<4> Power supply control command input	- P off	

↓

Starts the sleep mode.

(2) Clearing the sleep mode

Sleep mode

↓

<1> Power save command input	- PS off (power save) O on (oscillation)
<2> Power supply control command input	- P on

↓

Wait for 20 microseconds or more. (See Note 2)

↓

<3> Display on/off command input - D on (display) (See Note 3)

↓

<4> Static icon control - Address 20H, 22H
Data (*, *, *, *, *)
Address 21H, 23H
Data (*, *, *, *, *) (See Note 3)

↓

Returns to normal operation (original state).

Note 1. <6> and <7> of 15-1 indicate RAM initialization. Set the contents to be displayed in the beginning. For items not to be displayed (RAM Clear), use the following steps:
- DD RAM - write 20H (character code).
- CG RAM - write 00H (data ‘0’).
- Symbol register - write 00H (data ‘0’).

The RAM data is unspecified at the time of reset input (after power is turned on). If the data ‘0’ is not written at this stage, unexpected display may occur to the unset position.

Note 2. Defined by the rising characteristics of the power circuit, time setting varies according to the external capacity. So be sure to make confirmation by external capacity, and set this time.

Note 3. The dynamic drive system display lamp is lit up by the display on/off command when it is on. The static icon lamp is lit by the static icon control command. So to light up the lamp simultaneously with start of display, execute the display on/off control command and static icon control within one frame.

OPTION LIST

The SED 1225 has the following options. Options are available exclusively for users. Please contact our Sales Department for information.

- The following shows how to define the name of the product compatible with options:

  Example: SED1225D*B
  ↑
  Option compatibility column

Specification of character generator ROM (CGROM)

The SED1225 incorporates a characters generator ROM consisting of up to 256 types of characters, with each character size featuring 5 × 7 (8) dots. The SED1225 CGROM is designed as a masked ROM, and is compatible with the CGROM for exclusive use of the user. For the standard CGROM, see the Character Font Table.

Specifications of external clock

The SED1225 has an external clock terminal which is provided with two types of functions; f_{OSC} and $4 \times f_{OSC}$. Either f_{OSC} or $4 \times f_{OSC}$ can be selected according to the user's requirements.

	Built-in oscillation f_{OSC}	External clock f_{OSC}	External clock $4 \times f_{OSC}$
Standard	○	○	×
Optional	○	×	○

The standard external clock specifications are set on the f_{OSC}.

CAUTIONS

The following points should be noted when this Development Specification is used:

1. This Development Specification is subject to modification for improvement without prior notice.
2. This Development Specification is not intended to guarantee enforcement of industrial property and other rights, or to grant license for the use of this product. Examples of applications mentioned in this Development Specification are given for effective understanding of the product. We are not responsible for any circuit problems which might occur due to use of these examples. The size of the values appearing in the characteristics table is represented by the size of the number line.
3. Part or whole of this Development Specification shall not be quoted, reproduced or used for other purposes without permission of our company.

For the use of the semi-conductor, take note of the following:
“Handling cautions for light”

According to the principle of the solar battery the semiconductor characteristics are changed when exposed to light. So misoperation may occur if this IC is exposed to light.

For the single IC unit, measures against light are not yet completely taken. The board and the product where this IC is mounted must be provided with the following measures:

(1) For designing and mounting, measures must be taken to provide the structure which ensures the light protecting properties of the IC during actual use.
(2) In the inspection process, environmental design must be made with consideration given to the light protecting properties of the IC.
(3) To ensure light protecting properties of the IC, consideration must be given to the surface, back and sides of the IC chip.

SED1230 Series
LCD Controller/Drivers

Technical Manual

Contents

OVERVIEW

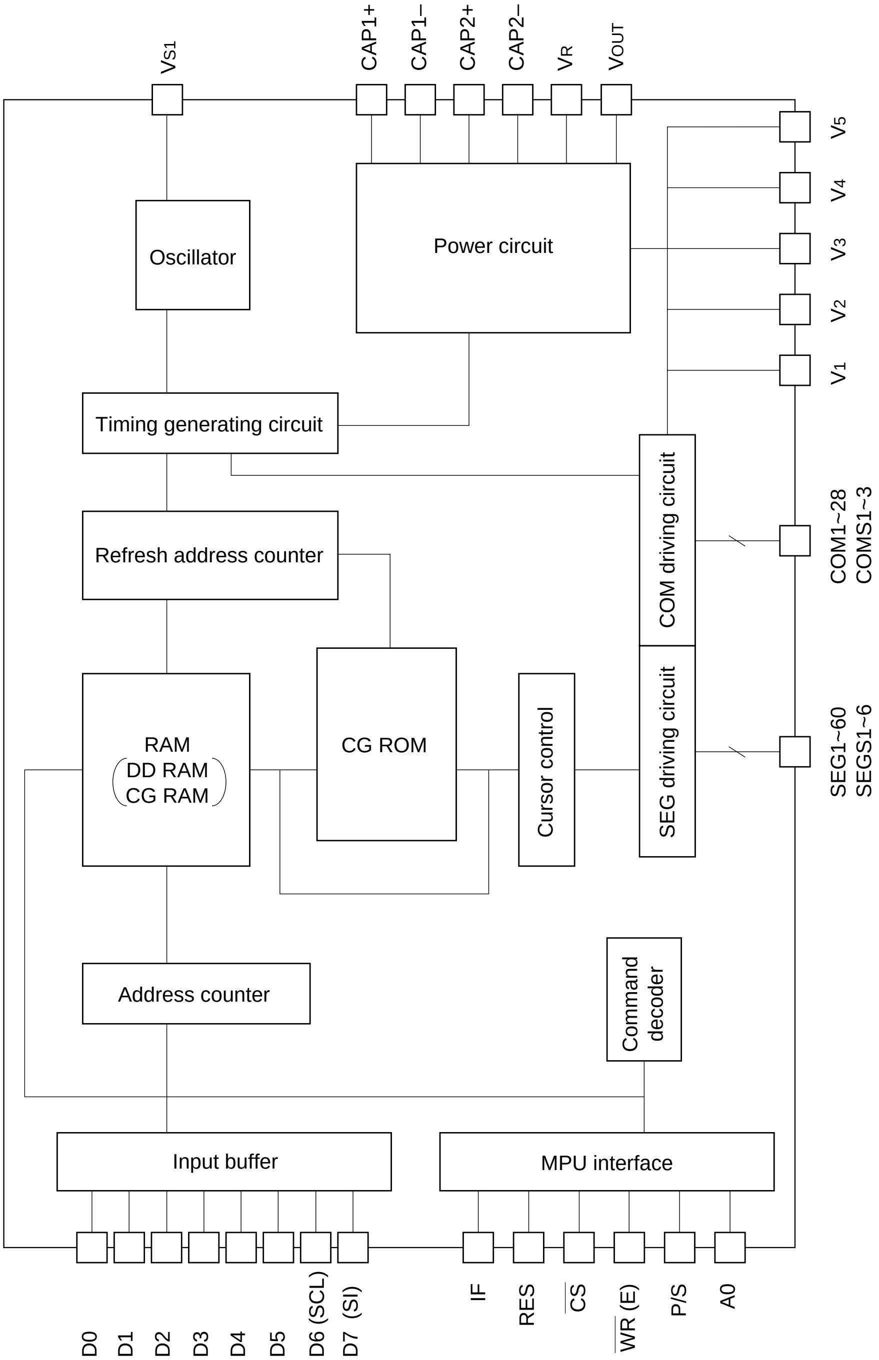
The SED1230 Series is a dot matrix LCD controller driver for character display, and can display a maximum of 48 characters, 4 user-defined characters, and a maximum of 64 symbols by means of 4-bit, 8-bit or serial data sent from a microcomputer.
A built-in character generator ROM is prepared for 256 character types, and each character font consists of 5 × 7 dots. A user-defined character RAM for four characters of 5 × 7 dots are incorporated, and a symbol register is also incorporated. With these, it is possible to apply this Series to display with a high degree of freedom. This Series can operate handy units with a minimum power consumption by means of its low power consumption and standby mode.
The SED1230 Series are classified into SED1230, SED1231, SED1232, and SED1233 depending on the duty of use and the number of display columns.

FEATURES

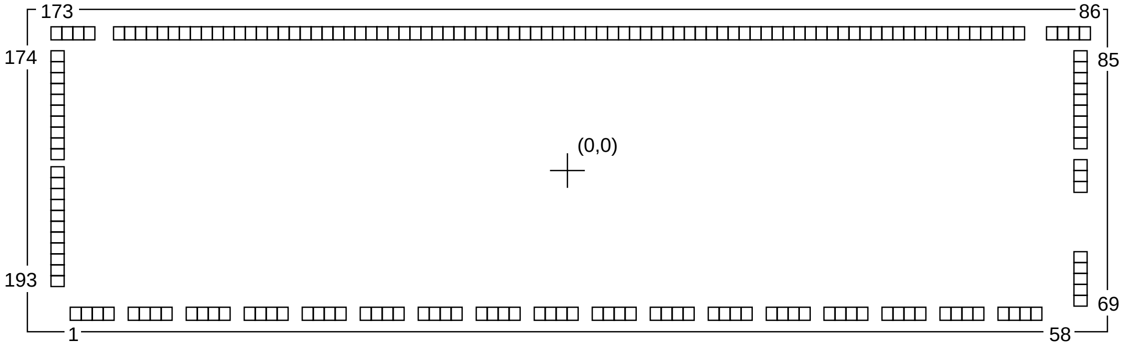
- Built-in display RAM
  48 characters + 4 user-defined characters + 64 symbols
- CG ROM (for up to 256 characters), CG RAM (4 characters), and symbol register (64 symbols)
- Number of display columns × number of lines
  (12 columns + 1 column for signal) × 4 lines + 52 symbols: SED1230
  (12 columns + 1 column for signal) × 3 lines + 52 symbols: SED1231
  (12 columns + 1 column for signal) × 2 lines + 52 symbols: SED1232
  16 columns × 2 lines + 64 symbols: SED1233
- CR oscillation circuit (on-chip C and R)
- High-speed MPU interface
  Interfacing with both 68 series and 80 series MPU
  Interfacing in 4 bits/8 bits
- Serial interface
- Character font 5 × 7 dots
- Duty ratio 1/16 (SED1232, SED1233)
  1/23 (SED1231)
  1/30 (SED1230)
- Simple command setting
- Built-in liquid crystal driving power circuit
  Power boosting circuit, power regulating circuit, voltage follower × 4
- Built-in electronic volume function
- Low power consumption
  100 µA Max. (In normal operation mode: Including the operating current of the built-in power supply)
  20 µA Max. (In standby display mode)
- Power supply
  V_{DD} - V_{SS} (logic section): –2.4 V to –3.6 V
  V_{DD} - V_5 (liquid crystal drive section)
  : –5.0 V to –11.0 V
- Wide operating temperature range
  Ta = -30 to 85°C
- CMOS process
- Delivery form: Chip SED123∗D∗B, SED123∗D∗E (Gold bump product)
  SED123∗D∗A, SED123∗D∗C (A1 pad product)
  TCP SED123∗T∗∗
- This IC is not designed with a protection against radioactive rays.

SED1230 Series

BLOCK DIAGRAM



SED1230 SERIES, CHIP SPECIFICATION



SED1230D∗∗	1/30 duty	12 columns + 1 signal column
SED1231D∗∗	1/23 duty	12 columns + 1 signal column
SED1232D∗∗	1/16 duty	12 columns + 1 signal column
SED1233D∗∗	1/16 duty	16 columns

↑ #1 Column for CG ROM pattern change

Chip size: 10.23 × 3.11 mm
Pad pitch: 110 µm (Min.)
Chip thickness: 625 (SED123∗D∗A, SED123∗D∗B)
525 (SED123∗D∗C, SED123∗D∗E)

1) A1 pad specification (SED123∗D∗A)
   Pad size: A 86 µm × 135 µm
   B 135 µm × 86 µm
2) Au bump specification (SED123∗D∗B)
   For reference:
   Bump size A 80 µm × 129 µm
   B 129 µm × 80 µm
   Bump height 22.5 µm

<SED1230D**>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2	↓	–4683	↓
3	↓	–4572	↓
4	↓	–4462	↓
5	V_{DD}	–4242	↓
6	↓	–4132	↓
7	↓	–4021	↓
8	↓	–3911	↓
9	V_{SS}	–3691	↓
10	↓	–3581	↓
11	↓	–3470	↓
12	↓	–3360	↓
13	V_5	–3140	↓
14	↓	–3030	↓
15	↓	–2919	↓
16	↓	–2809	↓
17	V_4	–2589	↓
18	↓	–2479	↓
19	↓	–2368	↓
20	↓	–2258	↓
21	V_3	–2021	↓
22	↓	–1910	↓
23	↓	–1800	↓
24	↓	–1690	↓
25	V_2	–1453	↓
26	↓	–1342	↓
27	↓	–1232	↓
28	↓	–1122	↓
29	V_1	–884	↓
30	↓	–774	↓
31	↓	–664	↓
32	↓	–554	↓
33	V_0	–316	↓
34	↓	–206	↓
35	↓	–96	↓
36	↓	14	↓
37	V_R	235	↓
38	↓	345	↓
39	↓	455	↓
40	↓	565	↓
41	V_{OUT}	803	↓
42	↓	913	↓
43	↓	1023	↓
44	↓	1133	↓
45	CAP2-	1354	↓
46	↓	1464	↓
47	↓	1574	↓
48	↓	1684	↓
49	CAP2+	1905	↓
50	↓	2015	↓
51	↓	2125	↓
52	↓	2235	↓
53	CAP1-	2473	↓
54	↓	2583	↓

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56	↓	2803	↓
57	CAP1+	3024	↓
58	↓	3134	↓
59	↓	3244	↓
60	↓	3354	↓
61	V_{SS}	3592	↓
62	↓	3702	↓
63	↓	3812	↓
64	↓	3923	↓
65	V_{DD}	4143	↓
66	↓	4253	↓
67	↓	4363	↓
68	↓	4474	↓
69	(NC)	4883	–1343
70	(NC)	↓	–1233
71	(NC)	↓	–1123
72	(NC)	↓	–1013
73	V_{S1}	4929	–902
74	P/S	↓	–186
75	IF	↓	–76
76	RES	↓	34
77	COMS1	↓	255
78	COMS2	↓	365
79	COM 1	↓	475
80	COM 2	↓	585
81	COM 3	↓	696
82	COM 4	↓	806
83	COM 5	↓	916
84	COM 6	↓	1026
85	COM 7	↓	1136
86	(NC)	4947	1382
87	↓	4836	↓
88	↓	4726	↓
89	↓	4616	↓
90	COM 8	4347	↓
91	COM 9	4237	↓
92	COM10	4127	↓
93	COM11	4017	↓
94	COM12	3906	↓
95	COM13	3796	↓
96	COM14	3686	↓
97	SEGS2	3576	↓
98	SEGS3	3466	↓
99	SEGS4	3355	↓
100	SEG 1	3245	↓
101	SEG 2	3135	↓
102	SEG 3	3025	↓
103	SEG 4	2915	↓
104	SEG 5	2804	↓
105	SEG 6	2694	↓
106	SEG 7	2584	↓
107	SEG 8	2474	↓
108	SEG 9	2364	↓

PAD		COORDINATES	
No.	Name	X	Y
109	SEG10	2253	–1382
110	SEG11	2143	
111	SEG12	2033	
112	SEG13	1923	
113	SEG14	1813	
114	SEG15	1702	
115	SEG16	1592	
116	SEG17	1482	
117	SEG18	1372	
118	SEG19	1262	
119	SEG20	1151	
120	SEG21	1041	
121	SEG22	931	
122	SEG23	821	
123	SEG24	711	
124	SEG25	600	
125	SEG26	490	
126	SEG27	380	
127	SEG28	270	
128	SEG29	160	
129	SEG30	49	
130	SEG31	–61	
131	SEG32	–171	
132	SEG33	–281	
133	SEG34	–391	
134	SEG35	–502	
135	SEG36	–612	
136	SEG37	–722	
137	SEG38	–832	
138	SEG39	–942	
139	SEG40	–1053	
140	SEG41	–1163	
141	SEG42	–1273	
142	SEG43	–1383	
143	SEG44	–1493	
144	SEG45	–1604	
145	SEG46	–1714	
146	SEG47	–1824	
147	SEG48	–1934	
148	SEG49	–2044	
149	SEG50	–2155	
150	SEG51	–2265	
151	SEG52	–2375	
152	SEG53	–2485	
153	SEG54	–2595	
154	SEG55	–2706	
155	SEG56	–2816	
156	SEG57	–2926	
157	SEG58	–3036	
158	SEG59	–3146	
159	SEG60	–3257	
160	SEGS4	–3367	
161	SEGS5	–3477	
162	SEGS6	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	COM28	–3697	1382
164	COM27	–3808	
165	COM26	–3918	
166	COM25	–4028	
167	COM24	–4138	
168	COM23	–4248	
169	COM22	–4359	
170	(NC)	–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM21	–4940	1136
175	COM20		1026
176	COM19		916
177	COM18		806
178	COM17		696
179	COM16		585
180	COM15		475
181	COMS3		365
182	SEGS1		255
183	A0		34
184	WR		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

<SED1231D**>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2	↓	–4683	↓
3	↓	–4572	↓
4	↓	–4462	↓
5	V_{DD}	–4242	↓
6	↓	–4132	↓
7	↓	–4021	↓
8	↓	–3911	↓
9	V_{SS}	–3691	↓
10	↓	–3581	↓
11	↓	–3470	↓
12	↓	–3360	↓
13	V_5	–3140	↓
14	↓	–3030	↓
15	↓	–2919	↓
16	↓	–2809	↓
17	V_4	–2589	↓
18	↓	–2479	↓
19	↓	–2368	↓
20	↓	–2258	↓
21	V_3	–2021	↓
22	↓	–1910	↓
23	↓	–1800	↓
24	↓	–1690	↓
25	V_2	–1453	↓
26	↓	–1342	↓
27	↓	–1232	↓
28	↓	–1122	↓
29	V_1	–884	↓
30	↓	–774	↓
31	↓	–664	↓
32	↓	–554	↓
33	V_0	–316	↓
34	↓	–206	↓
35	↓	–96	↓
36	↓	14	↓
37	V_R	235	↓
38	↓	345	↓
39	↓	455	↓
40	↓	565	↓
41	V_{OUT}	803	↓
42	↓	913	↓
43	↓	1023	↓
44	↓	1133	↓
45	CAP2-	1354	↓
46	↓	1464	↓
47	↓	1574	↓
48	↓	1684	↓
49	CAP2+	1905	↓
50	↓	2015	↓
51	↓	2125	↓
52	↓	2235	↓
53	CAP1-	2473	↓
54	↓	2583	↓

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56	↓	2803	↓
57	CAP1+	3024	↓
58	↓	3134	↓
59	↓	3244	↓
60	↓	3354	↓
61	V_{SS}	3592	↓
62	↓	3702	↓
63	↓	3812	↓
64	↓	3923	↓
65	V_{DD}	4143	↓
66	↓	4253	↓
67	↓	4363	↓
68	↓	4474	↓
69	(NC)	4883	–1343
70	(NC)	↓	–1233
71	(NC)	↓	–1123
72	(NC)	↓	–1013
73	V_{S1}	4929	–902
74	P/S	↓	–186
75	IF	↓	–76
76	RES	↓	34
77	COMS1	↓	255
78	COMS2	↓	365
79	COM 1	↓	475
80	COM 2	↓	585
81	COM 3	↓	696
82	COM 4	↓	806
83	COM 5	↓	916
84	COM 6	↓	1026
85	COM 7	↓	1136
86	(NC)	4947	1382
87	↓	4836	↓
88	↓	4726	↓
89	↓	4616	↓
90	COM 8	4347	↓
91	COM 9	4237	↓
92	COM10	4127	↓
93	COM11	4017	↓
94	COM12	3906	↓
95	COM13	3796	↓
96	COM14	3686	↓
97	SEGS2	3576	↓
98	SEGS3	3466	↓
99	SEGS4	3355	↓
100	SEG 1	3245	↓
101	SEG 2	3135	↓
102	SEG 3	3025	↓
103	SEG 4	2915	↓
104	SEG 5	2804	↓
105	SEG 6	2694	↓
106	SEG 7	2584	↓
107	SEG 8	2474	↓
108	SEG 9	2364	↓

PAD		COORDINATES	
No.	Name	X	Y
109	SEG10	2253	1382
110	SEG11	2143	
111	SEG12	2033	
112	SEG13	1923	
113	SEG14	1813	
114	SEG15	1702	
115	SEG16	1592	
116	SEG17	1482	
117	SEG18	1372	
118	SEG19	1262	
119	SEG20	1151	
120	SEG21	1041	
121	SEG22	931	
122	SEG23	821	
123	SEG24	711	
124	SEG25	600	
125	SEG26	490	
126	SEG27	380	
127	SEG28	270	
128	SEG29	160	
129	SEG30	49	
130	SEG31	–61	
131	SEG32	–171	
132	SEG33	–281	
133	SEG34	–391	
134	SEG35	–502	
135	SEG36	–612	
136	SEG37	–722	
137	SEG38	–832	
138	SEG39	–942	
139	SEG40	–1053	
140	SEG41	–1163	
141	SEG42	–1273	
142	SEG43	–1383	
143	SEG44	–1493	
144	SEG45	–1604	
145	SEG46	–1714	
146	SEG47	–1824	
147	SEG48	–1934	
148	SEG49	–2044	
149	SEG50	–2155	
150	SEG51	–2265	
151	SEG52	–2375	
152	SEG53	–2485	
153	SEG54	–2595	
154	SEG55	–2706	
155	SEG56	–2816	
156	SEG57	–2926	
157	SEG58	–3036	
158	SEG59	–3146	
159	SEG60	–3257	
160	SEGS4	–3367	
161	SEGS5	–3477	
162	SEGS6	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	(NC)	–3697	1382
164		–3808	
165		–3918	
166		–4028	
167		–4138	
168		–4248	
169		–4359	
170		–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM21	–4940	1136
175	COM20		1026
176	COM19		916
177	COM18		806
178	COM17		696
179	COM16		585
180	COM15		475
181	COMS3		365
182	SEGS1		255
183	A0		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

<SED1232D**>

Unit: µm

PAD		COORDINATES		PAD		COORDINATES	
No.	Name	X	Y	No.	Name	X	Y
1	(NC)	–4793	–1371	55	CAP1–	2693	–1371
2	↓	–4683	↓	56	↓	2803	↓
3	↓	–4572	↓	57	CAP1+	3024	↓
4	↓	–4462	↓	58	↓	3134	↓
5	V_{DD}	–4242	↓	59	↓	3244	↓
6	↓	–4132	↓	60	↓	3354	↓
7	↓	–4021	↓	61	V_{SS}	3592	↓
8	↓	–3911	↓	62	↓	3702	↓
9	V_{SS}	–3691	↓	63	↓	3812	↓
10	↓	–3581	↓	64	↓	3923	↓
11	↓	–3470	↓	65	V_{DD}	4143	↓
12	↓	–3360	↓	66	↓	4253	↓
13	V_5	–3140	↓	67	↓	4363	↓
14	↓	–3030	↓	68	↓	4474	↓
15	↓	–2919	↓	69	(NC)	4883	–1343
16	↓	–2809	↓	70	(NC)	↓	–1233
17	V_4	–2589	↓	71	(NC)	↓	–1123
18	↓	–2479	↓	72	(NC)	↓	–1013
19	↓	–2368	↓	73	V_{S1}	4929	–902
20	↓	–2258	↓	74	P/S	↓	–186
21	V_3	–2021	↓	75	IF	↓	–76
22	↓	–1910	↓	76	RES	↓	34
23	↓	–1800	↓	77	COMS1	↓	255
24	↓	–1690	↓	78	COMS2	↓	365
25	V_2	–1453	↓	79	COM 1	↓	475
26	↓	–1342	↓	80	COM 2	↓	585
27	↓	–1232	↓	81	COM 3	↓	696
28	↓	–1122	↓	82	COM 4	↓	806
29	V_1	–884	↓	83	COM 5	↓	916
30	↓	–774	↓	84	COM 6	↓	1026
31	↓	–664	↓	85	COM 7	↓	1136
32	↓	–554	↓	86	(NC)	4947	1382
33	V_0	–316	↓	87	↓	4836	↓
34	↓	–206	↓	88	↓	4726	↓
35	↓	–96	↓	89	↓	4616	↓
36	↓	14	↓	90	COM 8	4347	↓
37	V_R	235	↓	91	COM 9	4237	↓
38	↓	345	↓	92	COM10	4127	↓
39	↓	455	↓	93	COM11	4017	↓
40	↓	565	↓	94	COM12	3906	↓
41	V_{OUT}	803	↓	95	COM13	3796	↓
42	↓	913	↓	96	COM14	3686	↓
43	↓	1023	↓	97	SEGS2	3576	↓
44	↓	1133	↓	98	SEGS3	3466	↓
45	CAP2-	1354	↓	99	SEGS4	3355	↓
46	↓	1464	↓	100	SEG 1	3245	↓
47	↓	1574	↓	101	SEG 2	3135	↓
48	↓	1684	↓	102	SEG 3	3025	↓
49	CAP2+	1905	↓	103	SEG 4	2915	↓
50	↓	2015	↓	104	SEG 5	2804	↓
51	↓	2125	↓	105	SEG 6	2694	↓
52	↓	2235	↓	106	SEG 7	2584	↓
53	CAP1-	2473	↓	107	SEG 8	2474	↓
54	↓	2583	↓	108	SEG 9	2364	↓

PAD		COORDINATES	
No.	Name	X	Y
109	SEG10	2253	1382
110	SEG11	2143	↓
111	SEG12	2033	
112	SEG13	1923	
113	SEG14	1813	
114	SEG15	1702	
115	SEG16	1592	
116	SEG17	1482	
117	SEG18	1372	
118	SEG19	1262	
119	SEG20	1151	
120	SEG21	1041	
121	SEG22	931	
122	SEG23	821	
123	SEG24	711	
124	SEG25	600	
125	SEG26	490	
126	SEG27	380	
127	SEG28	270	
128	SEG29	160	
129	SEG30	49	
130	SEG31	–61	
131	SEG32	–171	
132	SEG33	–281	
133	SEG34	–391	
134	SEG35	–502	
135	SEG36	–612	
136	SEG37	–722	
137	SEG38	–832	
138	SEG39	–942	
139	SEG40	–1053	
140	SEG41	–1163	
141	SEG42	–1273	
142	SEG43	–1383	
143	SEG44	–1493	
144	SEG45	–1604	
145	SEG46	–1714	
146	SEG47	–1824	
147	SEG48	–1934	
148	SEG49	–2044	
149	SEG50	–2155	
150	SEG51	–2265	
151	SEG52	–2375	
152	SEG53	–2485	
153	SEG54	–2595	
154	SEG55	–2706	
155	SEG56	–2816	
156	SEG57	–2926	
157	SEG58	–3036	
158	SEG59	–3146	
159	SEG60	–3257	
160	SEGS4	–3367	
161	SEGS5	–3477	
162	SEGS6	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	(NC)	–3697	1382
164	↓	–3808	↓
165		–3918	
166		–4028	
167		–4138	
168		–4248	
169		–4359	
170		–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM14	–4940	1136
175	COM13	↓	1026
176	COM12		916
177	COM11		806
178	COM10		696
179	COM 9		585
180	COM 8		475
181	COMS3		365
182	SEGS1		255
183	A0		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

<SED1233D**>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2	↓	–4683	↓
3	↓	–4572	↓
4	↓	–4462	↓
5	V_{DD}	–4242	↓
6	↓	–4132	↓
7	↓	–4021	↓
8	↓	–3911	↓
9	V_{SS}	–3691	↓
10	↓	–3581	↓
11	↓	–3470	↓
12	↓	–3360	↓
13	V_5	–3140	↓
14	↓	–3030	↓
15	↓	–2919	↓
16	↓	–2809	↓
17	V_4	–2589	↓
18	↓	–2479	↓
19	↓	–2368	↓
20	↓	–2258	↓
21	V_3	–2021	↓
22	↓	–1910	↓
23	↓	–1800	↓
24	↓	–1690	↓
25	V_2	–1453	↓
26	↓	–1342	↓
27	↓	–1232	↓
28	↓	–1122	↓
29	V_1	–884	↓
30	↓	–774	↓
31	↓	–664	↓
32	↓	–554	↓
33	V_0	–316	↓
34	↓	–206	↓
35	↓	–96	↓
36	↓	14	↓
37	V_R	235	↓
38	↓	345	↓
39	↓	455	↓
40	↓	565	↓
41	V_{OUT}	803	↓
42	↓	913	↓
43	↓	1023	↓
44	↓	1133	↓
45	CAP2-	1354	↓
46	↓	1464	↓
47	↓	1574	↓
48	↓	1684	↓
49	CAP2+	1905	↓
50	↓	2015	↓
51	↓	2125	↓
52	↓	2235	↓
53	CAP1-	2473	↓
54	↓	2583	↓

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56	↓	2803	↓
57	CAP1+	3024	↓
58	↓	3134	↓
59	↓	3244	↓
60	↓	3354	↓
61	V_{SS}	3592	↓
62	↓	3702	↓
63	↓	3812	↓
64	↓	3923	↓
65	V_{DD}	4143	↓
66	↓	4253	↓
67	↓	4363	↓
68	↓	4474	↓
69	(NC)	4883	–1343
70	(NC)	↓	–1233
71	(NC)	↓	–1123
72	(NC)	↓	–1013
73	V_{S1}	4929	–902
74	P/S	↓	–186
75	IF	↓	–76
76	RES	↓	34
77	COMS1	↓	255
78	COMS2	↓	365
79	COM 1	↓	475
80	COM 2	↓	585
81	COM 3	↓	696
82	COM 4	↓	806
83	COM 5	↓	916
84	COM 6	↓	1026
85	COM 7	↓	1136
86	(NC)	4947	1382
87	↓	4836	↓
88	↓	4726	↓
89	↓	4616	↓
90	SEG 1	4347	↓
91	SEG 2	4237	↓
92	SEG 3	4127	↓
93	SEG 4	4017	↓
94	SEG 5	3906	↓
95	SEG 6	3796	↓
96	SEG 7	3686	↓
97	SEG 8	3576	↓
98	SEG 9	3466	↓
99	SEG10	3355	↓
100	SEG11	3245	↓
101	SEG12	3135	↓
102	SEG13	3025	↓
103	SEG14	2915	↓
104	SEG15	2804	↓
105	SEG16	2694	↓
106	SEG17	2584	↓
107	SEG18	2474	↓
108	SEG19	2364	↓

PAD		COORDINATES	
No.	Name	X	Y
109	SEG20	2253	1382
110	SEG21	2143	
111	SEG22	2033	
112	SEG23	1923	
113	SEG24	1813	
114	SEG25	1702	
115	SEG26	1592	
116	SEG27	1482	
117	SEG28	1372	
118	SEG29	1262	
119	SEG30	1151	
120	SEG31	1041	
121	SEG32	931	
122	SEG33	821	
123	SEG34	711	
124	SEG35	600	
125	SEG36	490	
126	SEG37	380	
127	SEG38	270	
128	SEG39	160	
129	SEG40	49	
130	SEG41	–61	
131	SEG42	–171	
132	SEG43	–281	
133	SEG44	–391	
134	SEG45	–502	
135	SEG46	–612	
136	SEG47	–722	
137	SEG48	–832	
138	SEG49	–942	
139	SEG50	–1053	
140	SEG51	–1163	
141	SEG52	–1273	
142	SEG53	–1383	
143	SEG54	–1493	
144	SEG55	–1604	
145	SEG56	–1714	
146	SEG57	–1824	
147	SEG58	–1934	
148	SEG59	–2044	
149	SEG60	–2155	
150	SEG61	–2265	
151	SEG62	–2375	
152	SEG63	–2485	
153	SEG64	–2595	
154	SEG65	–2706	
155	SEG66	–2816	
156	SEG67	–2926	
157	SEG68	–3036	
158	SEG69	–3146	
159	SEG70	–3257	
160	SEG71	–3367	
161	SEG72	–3477	
162	SEG73	–3587	↓

PAD		COORDINATES	
No.	Name	X	Y
163	SEG74	–3697	1382
164	SEG75	–3808	
165	SEG76	–3918	
166	SEG77	–4028	
167	SEG78	–4138	
168	SEG79	–4248	
169	SEG80	–4359	
170	(NC)	–4627	
171		–4738	
172		–4848	
173	↓	–4958	↓
174	COM14	–4940	1136
175	COM13		1026
176	COM12		916
177	COM11		806
178	COM10		696
179	COM 9		585
180	COM 8		475
181	COMS3		365
182	SEGS1		255
183	A0		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0	↓	–1068

DESCRIPTION OF PINS

Power Pins

Pin name	I/O	Description	Q'ty
V_{DD}	Power supply	Logic + power pin. Also used as MPU power pin V_{CC}.	2
V_{SS}	Power supply	Logic – power pin. Connected to the system GND.	2
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined in the liquid crystal cell is resistance-divided or impedance-converted by operational amplifier, and the resultant voltage is applied. The potential is determined on the basis of V_{DD} and the following equation must be respected. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to pins V_1 to V_4 by built-in power circuit: $V_1 = 1/5\ V_5$ $V_2 = 2/5\ V_5$ $V_3 = 3/5\ V_5$ $V_4 = 4/5\ V_5$	6
V_{S1}	O	Power supply voltage output pin for oscillating circuit. Don't connect this pin to an external load.	1

LCD Power Circuit Pins

Pin name	I/O	Description	Q'ty
CAP1+	O	Capacitor positive side connecting pin for boosting. This pin connects the capacitor with pin CAP1–.	1
CAP1–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP+.	1
CAP2+	O	Capacitor positive side connecting pin for boosting. This pin connects a capacitor with pin CAP2–.	1
CAP2–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP2+.	1
V_{OUT}	O	Output pin for boosting. This pin connects a smoothing capacitor with V_{SS} pin.	1
V_R	I	Voltage regulating pin. This pin gives a voltage between V_{DD} and V_5 by resistance-division of voltage.	1

Pins for System Bus Connection

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Q'ty</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 ~ D0</td><td>I</td><td>8-bit input data bus. These pins are connected to a 8-bit or 16-bit standard MPU data bus.
When P/S = “Low”, the D7 and D6 pins are operated as a serial data input and a serial clock input respectively.
<table>
<tr><td>P/S</td><td>D7</td><td>D6</td><td>D5 ~ D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>“Low”</td><td>SI</td><td>SCL</td><td>—</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>“High”</td><td>D7</td><td>D6</td><td>D5 ~ D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
</table></td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, this pin connects the least significant bit of the MPU address bus and identifies a data command.
0 : Indicates that D0 to D7 are a command.
1 : Indicates that D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>In case of a 68 series MPU, initialization can be performed by changing RES ⌐↓. In case of an 80 series MPU, initialization can be performed by changing ∟↑.
A reset operation is performed by edge sensing of the RES signal. An interface type for the 68/80 series MPU is selected by input level after initialization.
“L” : 68 series MPU interface
“H” : 80 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal. Usually, this pin inputs the signal obtained by decoding an address bus signal. At the “Low” level, this pin is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$

(E)</td><td>I</td><td><When connecting an 80 series MPU>
Active “Low”. This pin connects the $\overline{WR}$ signal of the 80 series MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ signal.
<When connecting a 68 series MPU>
Active “High”. This pin becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin switches between serial data input and parallel data input.
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Serial Clock</td></tr>
<tr><td>“High”</td><td>$\overline{CS}$</td><td>A0</td><td>D0~D7</td><td>–</td></tr>
<tr><td>“Low”</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>Interface data length select pin for parallel data input.
“High”: 8-bit parallel input
“Low”: 4-bit parallel input
When P/S = “Low”, connect this pin to V_{DD} or V_{SS}.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

SED1230, SED1231, SED1232

Pin name	I/O	Description	Q'ty
COM1~ COM28	O	Common signal output pin (for characters)	28
COMS1~ CMOS3	O	Common signal output pin (except for characters) CMOS1: Common output for static drive. In the standby mode only, a VSS amplitude is output. CMOS2, CMOS3: Common output for symbol display	3
SEG1~ SEG60	O	Segment signal output pin (for characters)	60
SEGS1~ SEGS6	O	Segment signal output pin (except for characters) SEGS1: Segment output for static drive. In the standby mode only, a VSS amplitude is output. SEGS2, SEGS6: Segment output for signal output	7

SED1233

Pin name	I/O	Description	Q'ty
COM1~ COM14	O	Common signal output pin (for characters)	14
COMS1~ CMOS3	O	Common signal output pin (except for characters) CMOS1: Common output for static drive. In the standby mode only, a VSS amplitude is output. CMOS2, CMOS3: Common output for symbol display	3
SEG1~ SEG80	O	Segment signal output pin (for characters)	80
SEGS1	O	Segment signal output pin (except for characters) SEGS1: Segment output for static drive. In the standby mode only, a VSS amplitude is output.	1

FUNCTIONAL DESCRIPTION

MPU Interface

Selection of interface type

In the SED1230 Series, data transfer is performed through a 8-bit or 4-bit data bus or a serial data input (SI). By selecting "High" or "Low" as P/S pin polarity, a parallel data input or a serial data input can be selected as shown in Table 1.

Table 1

P/S	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0~D7
"High"	Parallel Input	$\overline{CS}$	A0	$\overline{WR}$	—	—	D0~D7
"Low"	Serial Input	$\overline{CS}$	A0	—	SI	SCL	—

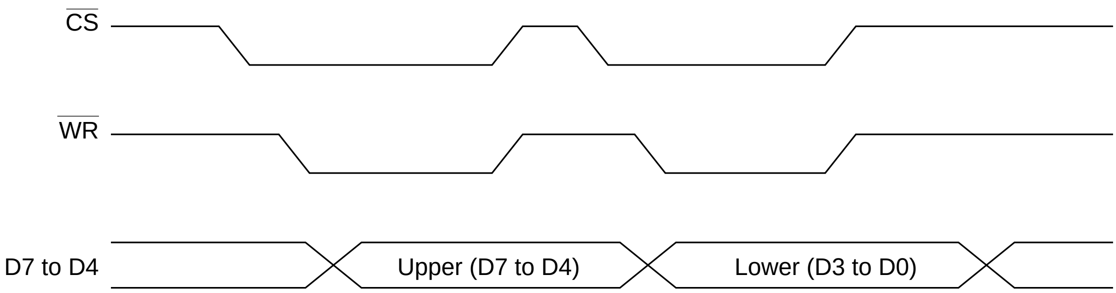
Parallel Input
In the SED1230 Series, when parallel input is selected (P/S = "High"), it can be directly connected to the 80 series MPU bus or 68 series MPU bus, as shown in Table 2, if either "High" or "Low" is selected as RES pin polarity after a reset input, because the RES pin has an MPU select function.
Selection between 8 bits and 4 bits is performed by command.

Table 2

RES input polarity	Type	A0	$\overline{WR}$	$\overline{CS}$	D0~D7
↓ active	68 series	A0	E	$\overline{CS}$	D0~D7
↑ active	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0~D7

Interface with 4-bit MPU interface

When data transfer is performed by 4-bit interface (IF = 0), an 8-bit command, data and address are divided into two parts.



Note: When performing writing in succession, reverse a time exceeding the system cycle time (t_{cyc}) and then perform writing.

Serial interface (P/S = "Low")

The serial interface consists of a 8-bit shift register and a 3-bit counter and acceptance of an SI input or SCL input is enabled in the ship selected status (CS = "Low").
When no chip is selected, the shift register and counter are reset to the initial status.
Serial data is input in the order of D7, D6 .... D0 from the serial data input pin (SI) at the rise of Serial Clock (SCL).
At the rising edge of the 8th serial clock, the serial data is converted into 8-bit parallel data and this data is processed.
The A0 input is used to identify whether the serial data input (SI) is display data or a command. That is, when A0 = "High", it is regarded as display data. When A0 = "Low", it is regarded as a command.
The A0 input is read in and identified at the rise of the 8 x n-th clock of Serial Clock (SCL) after chip selection.
Fig. 1 shows a timing chart of the serial interface.
Regarding the SCL signal, special care must be exercised about terminal reflection and external noise due to a wire length. We recommend the user to perform an operation check with a real machine.
We also recommend the user to periodically refresh the write status of each command to prevent a malfunction due to noise.

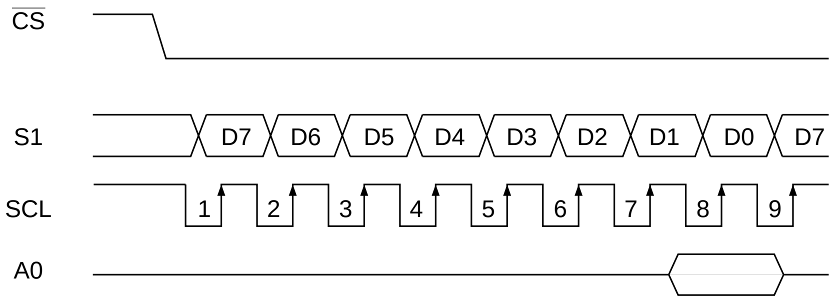


Fig. 1

Identification of data bus signals

The SED1230 series identifies data bus signals, as shown in Table 3, by combinations of A0 and $\overline{WR}$ (E).

Table 3

Common	68 series	80 series	Function
A0	E	$\overline{WR}$	
1	1	0	Writing to RAM and symbol register
0	1	0	Writing to internal register (command)

Chip select

The SED1230 series has a chip select pin ($\overline{CS}$). Only when $\overline{CS}$ = “Low”, MPU interfacing is enabled.
In any status other than Chip Select, D0 to D7 and A0, $\overline{WR}$, SI and SCL inputs are invalidated. When a serial input interface is selected, the shift register and counter are reset.

However, the Reset signal is input regardless of the $\overline{CS}$ status.

Power Circuit

This is a low-power-consumption power circuit that generates a voltage required for liquid crystal drive.
The power circuit consists of a boosting circuit, voltage regulating circuit and voltage follower.

The power circuit incorporated in the SED1230 Series is set for a small-scale liquid crystal panel, so that its display quality may be greatly deteriorated if it is used for a liquid crystal panel with a large display capacity.
In this case, an external power supply must be used.

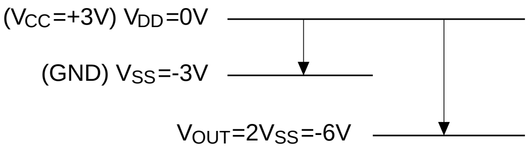
A power circuit function can be selected by power control command. With this, an external power supply and a part of the internal power supply can be used together.

	Boosting circuit	Voltage regulat-ing circuit	Voltage follower	External voltage input	Boosting system pin
	○	○	○	—	
Note 1	×	○	○	V_{OUT}	OPEN
Note 2	×	×	○	$V_5 = V_{OUT}$	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

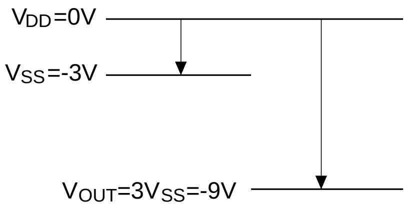
Note 1: When the boosting circuit is turned off, make boosting system pins (CAP1+, CAP1-, CAP2+, CAP2-) open and give a liquid crystal drive voltage to the VOUT pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, make the boosting system pins open, connect between the V5 pin and VOUT pin, and give a liquid crystal drive voltage from the outside.
Note 3: When all the internal power supplies are turned off, supply liquid crystal drive voltages V_1, V_2, V_3, V_4 and V_5 from the outside, and make the CAP1+, CAP1-, CAP2+, CAP2- and VOUT pins open.

Triple boosting circuit

When a capacitor is connected between CAP1+ and CAP1-, between CAP2+ and CAP2-, and between V_{SS} pin and V_{OUT} pin respectively, the potential between the V_{DD} pin and V_{SS} pin is boosted triple and output to the V_{OUT} pin. In case of double boosting, remove the capacitor between CAP2+ and CAP2- in connection for triple boosting operation and strap between CAP2- and V_{OUT} pin. Then, a double boosted output can be obtained from the V_{OUT} pin (CAP2-).
The boosting circuit uses a signal from the oscillator output.
Accordingly, it is necessary that the oscillating circuit must be in operation. The potential relationship of boosting is shown below.



Potential during double boosting



Potential during triple boosting

Voltage regulating circuit

The voltage regulation circuit regulates the boosted voltage developed at Vout. It outputs the regulated LCD driving voltage at the V_5 terminal. An internal resistor can be inserted into the regulation circuit feedback loop providing the following voltage levels at the V_5 terminal.

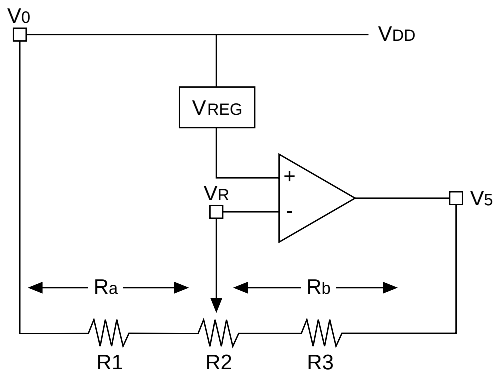
When V_5 is required to be different than the above case, leave the internal feedback resistor out of the circuit. V_5 can be regulated within a range of $|V_5|<|V_{OUT}|$. It may be calculated by the following formula:

$$V_5 = \left(1 + \frac{R_b}{R_a}\right) \cdot V_{REG} \quad \text{①}$$

Wherein, V_{REG} is the constant voltage source inside the SED1230 Series and the voltage is constant at $V_{REG} \fallingdotseq$ 3.1V. The voltage regulation $V_{REG} \fallingdotseq$ 2.1V (TYP.) in option 1, and $V_{REG} = V_{SS}$ in option 2. Voltage regulation of the V_5 output is accomplished by connecting a variable resistor between V_R, V_{DD} and V_5. For fine adjustment of the V_5 voltage, use a combination of fixed resistors R1 and R3 and a variable resistor R2.

The voltage regulator circuit carries a temperature gradient of about -0.17%/ °C under V_{REG} outputs (standard specification), about -0.04%/°C (option). When any other temperature gradient is required, connect a thermistor in series to the output voltage regulating register.

Since the V_R terminal has a high input impedance, it is necessary to take noise suppression measures such as shortening the input wiring and shielding the wiring run.



Example 1:
Condition: I(R1, R2, R3) ≤ 5µA V_5 = –6 to –8V

Setting:
R1+R2+R3 = 8V/5µA = 1.6MΩ
8V = (1+Rb/Ra) 3.0V Rb/Ra = 1.67
6V = (1+Rb/Ra) 3.0V Rb/Ra = 1
…. R1 = 600KΩ, R2 = 200KΩ, R3 = 800KΩ

● Voltage Regulation Circuit Using Electronic Contrast Control Register

The contrast control register controls the liquid crystal driving voltage (V_5). This is accomplished by an electronic volume control register set command that adjusts the contrast of the liquid crystal display (see section 1-22).

The commands provide 4-bits of voltage level data to the electronic volume control register. This provides for the selection of 16 different voltage levels for the liquid crystal driving voltage. When using the electronic volume control function, it is necessary to close the voltage regulation circuit using electronic control commands. For reference information, when the electronic volume control registor value is at (1, 1, 1, 1), the constant current value becomes: $I_{REF} \fallingdotseq 3.65uA$.

[An exemplary constant setting when the electronic volume control function is being used]

$$V_5 = \left(1 + \frac{R_b}{R_c}\right) \bullet V_{REG} \quad \cdots\cdots ②$$

$$\therefore\ R_c = \frac{R_a \times R_I}{R_a + R_I}$$

$$R_I = \frac{V_R}{I_{REF}}$$

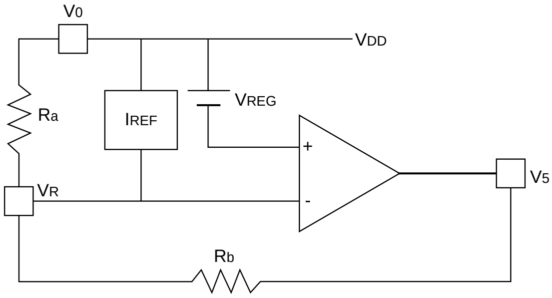


Fig. 9

(1) Determining the V_5 voltage setting range by the electronic volume control
Liquid crystal driving voltage V_5: max. -6V ~ min. -8V
V_5 variable voltage range: 2V

(2) Determining the R_b
R_b = V_5 variable voltage range/ I_{REF} ($I_{REF} \fallingdotseq 3.65\mu A$ Constant current)
= 2V/3.65µA
= 548KΩ

(3) Determining the R_a

$$R_a = \frac{V_{REG}}{(V_5 \text{ voltage setting max} - V_{REG}) / R_b}$$ (Use absolute values for V_{REG} and V_5 voltage settings.)

$$= \frac{3.1V}{(6V - 3.1V) / 548K\Omega}$$

= 585KΩ

(4) Regulating the R_a
Set the electronic volume control register to (D3, D2, D1, D0) = (1, 0, 0, 0) or (0, 1, 1, 1) before matching the R_a value to the optimum contrast.

Since I_{REF} is a simplified constant voltage source, fluctuations upto ± 40% must be taken into consideration, as a dispersion range during manufacture. Meanwhile, the temperature dependency of I_{REF} is: $\Delta I_{REF} \fallingdotseq -0.037\mu A/°C$. Determine the R_a and R_b for the using LCD panel in consideration of the above dispersion and the variation by the temperature.

When using the electronic volume control function, in order to compensate the V_5 voltage for dispersion of V_{REG} and I_{REF}, use a variable registor as R_a and perform optimum contrast adjustment according to the above item (4) with each IC chip.

When the electronic volume control function is not being used, set the electronic volume control register to (0, 0, 0, 0) using the RES signal or the electronic volume control register setting command.

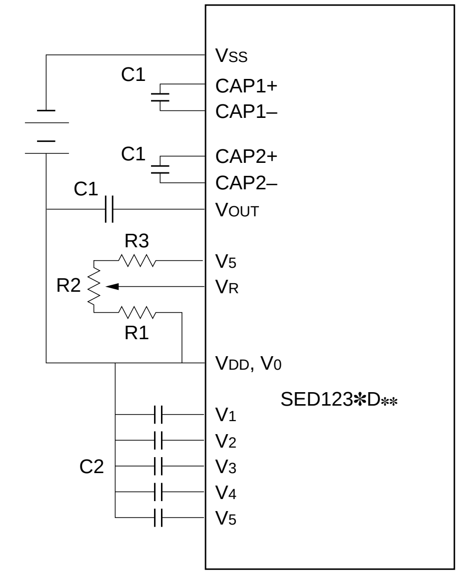
Liquid crystal voltage generating circuit

The V_5 potential is resistance-divided inside the IC so that V_1, V_2, V_3 and V_4 potentials are generated for liquid crystal drive.
Furthermore, the V_1, V_2, V_3 and V_4 are impedance-converted by voltage follower and the then supplied to the liquid crystal drive circuit.
The liquid crystal drive voltage is fixed to 1/5 bias.

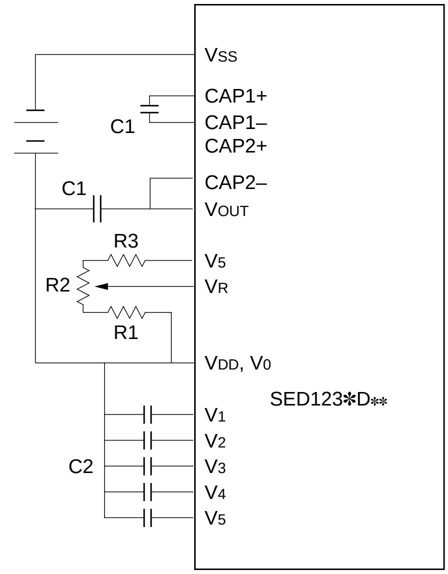
As shown in the diagrams below, the capacitor (C2) for voltage stabilization must be externally connected to the V1 to V5 pins of liquid crystal power pins.

When a built-in power supply is used

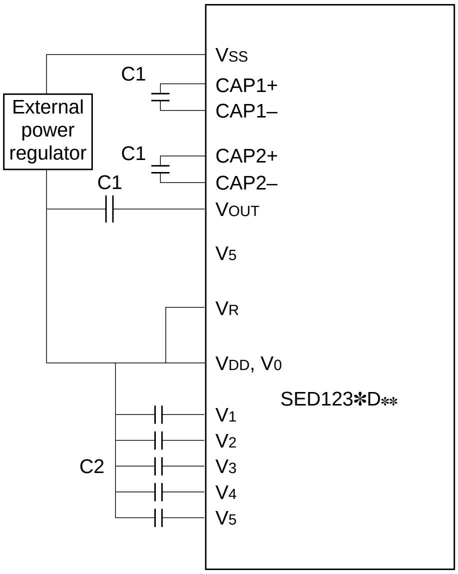
Under a triple boosting

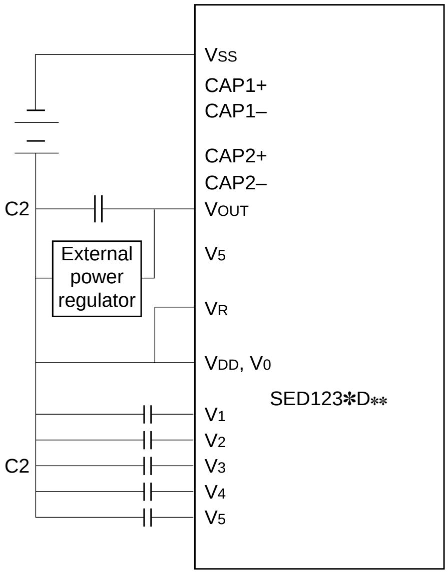


The diagram under a double boosting



When an external power regulator is used
(The built-in power regulator is not used)

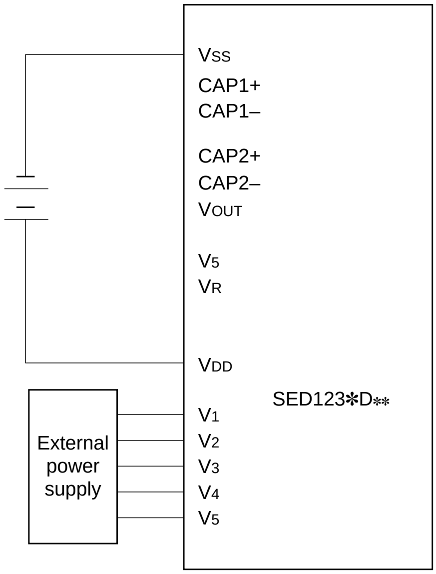




Reference setting values: C1: 0.1 - 4.7 µF
C2: 0.1 µF

We recommend the user to set the optimum values to capacitors C1 and C2 according to the panel size watching the liquid crystal display and drive waveforms.

When a built-in power supply is not used



Low Power Consumption Mode

The SED1230 Series is provided with the standby mode and sleep mode with the object of low power consumption when the unit is in the standby state.

◎ Standby Mode
The standby mode is turned on and off by power save command.
In the standby mode only, static display is enabled by CMOS1 and SEGS1.

1. Liquid crystal display output
   COM1 ~ COM28, COMS2, COMS3 : V_{DD} level
   SEG1 ~ SEG60, SEGS2 ~ SEGS6 : V_{DD} level
   COMS1, SEGS1 : Lighting is enabled by static drive.
   Perform display control using CMOS1 and SEGS1 by static display control command.
2. DD RAM, CG RAM and symbol register
   Written contents do not change and are stored regardless of whether the standby mode is turned on or off.
3. In the operation mode, the status precedent to execution of the standby mode is held.
   The internal circuit for dynamic display output stops.
4. Oscillating circuit
   For static display, the oscillating circuit must be ON.

◎ Sleep Mode
After the power circuit and oscillating circuit are turned off by command and the power save command is executed, the sleep mode is set. This mode permits reducing current consumption nearly to the static current value.

1. Liquid crystal display output
   COM1 ~ COM28, COMS2, COMS3 : V_{DD} level
   SEG1 ~ SEG60, SEGS2 ~ SEGS6 : V_{DD} level
   COMS1 ~ SEGS1 : V_{DD} level
2. DD RAM, CG RAM and symbol register
   Written contents do not change and are stored regardless of whether the sleep mode is turned on or off.
3. In the operation mode, the status precedent to execution of the sleep mode is held. All the internal circuits stops.
4. Power circuit and oscillating circuit
   Turn off the built-in power supply and oscillating circuit by power save command and power control command.

Reset Circuit

When the RES input goes active, this LSI enters the initialization status.

◎ Initialization status

1. Static display control
   SD0, SD1 = 0 : Display OFF
2. Display ON/OFF control
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
   DC = 0 : Double cursor OFF
   D = 0 : Display OFF
3. Power save
   O = 0 : Oscillating circuit OFF
   PS = 0 : Power save OFF
4. Power control
   VC = 0 : Voltage regulating circuit OFF
   VF = 0 : Voltage follower OFF
   P = 0 : Boosting circuit OFF
5. System set
   CG = 0 : Not use of CG RAM

As described in 6.1 MPU Interface, the RES pin is connected to the MPU reset pin and performs initialization concurrently with the MPU.
Regarding the reset signal, a pulse of at least 10 µs or more active level must be input as described in 9. DC Characteristics. Usually, the operation status is started in 1 µs from the edge of the RES signal.
In the SED1230 Series where the built-in liquid crystal power circuit is not used, the RES input must be active when the external liquid crystal power supply is turned on.
After the RES pin goes active, each register is cleared and set to the above set status.
Unless initialization is performed by the RES pin when a power supply voltage is applied, the clear disable status may be provided.

COMMANDS

Table 4 shows a command list. In the SED1230 Series, each data bus signal is identified by a combination of A0 and $\overline{WR}$ (E).
Command interpretation and execution are performed by only internal timing. This permits high-speed processing.

- **Outline of Commands**

Command type	Command name	A0	WR
Display control instruction	Cursor Home	0	0
	Static Display Control	0	0
	Display ON/OFF Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
	Electronic Volume Register Set	0	0
Address control instruction	Address Set	0	0
Data input instruction	Data Write	1	0

The execution time of each instruction is determined by the internal processing time of the SED1230 Series. Accordingly, to execute instructions in succession, reserve a time exceeding the cycle time (t_{cyc}) and execute the next instruction.

- **Outline of Commands**

(1) Cursor Home
This command presets the address counter to 30H. When the cursor is displayed, this command moves it to column 1 of line 1.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	*	*	*	*

* : Don't Care

(2) Static Display Control
This command selects display or non-display of static display symbol, and blink ON or OFF. This command is effective in the standby mode only.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	*	*	SD1	SD0

* : Don't Care

SD1, SD2 = 0, 0 : Display OFF
0, 1 : Blink (1 ~ 2 Hz)
SD1, SD2 = 1, 0 : Blink (3 ~ 4 Hz)
1, 1 : All Display ON

(3) Display ON/OFF Control
This command performs display and cursor setting.

Note: Control the symbols that are driven by COMS1 and SEGS1, by the Static Display Control command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	C	B	DC	D

D = 0 : Display OFF
1 : Display ON

DC = 0 : Double cursor OFF
1 : Double cursor ON

B = 0 : Cursor blink OFF
1 : Cursor blink ON

In the blink state, display characters in normal video and display characters in monochrome reverse video are displayed alternately.
The repetition cycle of alternate display is about 1 second.

C = 0 : Non-display of cursor
1 : Display of cursor

The relationship between C and B registers and cursor display is shown in the following table.

C	B	Cursor display
0	0	Non-display
0	1	Non-display
1	0	Display in monochrome reverse video
1	1	Alternate display of display characters in normal video and display characters in monochrome reverse video

The cursor display position corresponds to the position indicated by address counter.

Accordingly, to move the cursor, change the address counter value by the RAM Address Set command or auto increment by writing RAM data.

If the address counter is set at the symbol register position with (C, B) = (1, 0), symbols can be caused to blink selectively.

SED1230 Series

(4) Power Save
This command is used to control the oscillating circuit and set and reset the standby mode or sleep mode.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	*	*	O	PS

∗ : Don't Care

PS = 0 : Power save OFF (reset)
1 : Power save ON (set)

O = 0 : Oscillating circuit OFF (stop of oscillation)
1 : Oscillating circuit ON (oscilla tion)

(5) Power Control
This command is used to control the operation of the built-in power circuit.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	VC	VF	P

P = 0 : Boosting circuit OFF
1 : Boosting circuit ON

Note: To operate the boosting circuit of the SED1230 Series, the oscillating circuit must be in operation.

VF = 0 : Voltage follower OFF
1 : Voltage follower ON

VC = 0 : Voltage regulating circuit OFF
1 : Voltage regulating circuit ON

(6) System Set
This command set the use or non-use of display lines and CG RAM.
Execute this command first after turning on the power supply or after resetting.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	N2	N1	*	PS

∗ : Don't Care

CG = 0 : Non-use of CG RAM
1 : Use of CG RAM

N2	N1	
0	0	: 2 lines
0	1	: 3 lines
1	0	: 4 lines

(7) Electronic Volume Register Set
This command controls the liquid crystal driving voltage V_5 output from the voltage regulating circuit of the built-in liquid crystal power supply, thereby adjusting the gradation of liquid crystal display.
When data is set in the 4-bit register, the liquid crystal driving voltage can take one of 16 voltage states.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	MSB	*	*	LSB

Hex Code
70H ~7FH

MSB	.	.	LSB	$\lvert V_5 \rvert$	$\lvert I_{REF} \rvert$
0	0	0	0	Small	0.0 μA
		:		:	:
		. :		:	:
1	1	1	1	Large	About 3.65 μA

When the electronic volume function is not used, set (A3, A2, A1, A0) = (0, 0, 0, 0).

(8) RAM Address Set
This command sets addresses to write data into the DD RAM, CG RAM and symbol register in the address counter.

When the cursor is displayed, the cursor is displayed at the display position corresponding to the DDRAM address set by this command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ADDRESS						

① The settable address length is ADDRESS = 00H to 7FH.
② Before writing data into the RAM, set the data write address by this command. Next, when data is written in succession, the address is automatically incremented.

RAM Map (SED1230, SED1231, SED1232)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	CGRAM (00H)							–	CGRAM (01H)							–
10H	CGRAM (02H)							–	CGRAM (03H)							–
20H	Unused															
30H	DDRAM line 1													Unused		
40H	DDRAM line 2								For signals					"		
50H	DDRAM line 3													"		
60H	DDRAM line 4													"		
70H	Symbol register													"		

– : Unused
For signals : Output from SEGS2 to SEGS6.

RAM Map (SED1233)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	CGRAM (00H)							–	CGRAM (01H)							–
10H	CGRAM (02H)							–	CGRAM (03H)							–
20H	Unused															
30H	DDRAM line 1															
40H	DDRAM line 2															
50H	DDRAM line 3															
60H	DDRAM line 4															
70H	Symbol register															

–: Unused

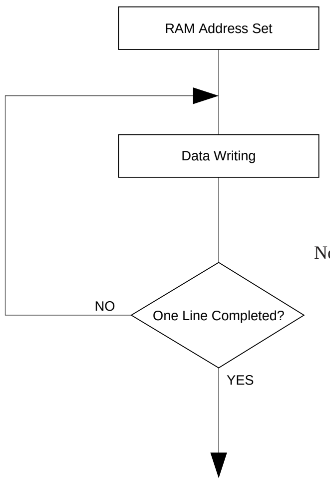
(9) Data Write

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DATA							

① This command writes data into the DD RAM, CG RAM or symbol register.
② After this command is executed, the address counter is automatically incremented by 1. This permits writing data in succession.

<Example of Data Writing>

The following is an example of writing one-line data into the DD RAM in succession.



Note: When executing instructions in succession, reserve a time exceeding t_{CYC} and execute the next instruction.

Table 4 SED1230 Series Command List

Command	Code										Function
	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position.
(2) Static Display Control	0	0	0	0	1	0	*	*	SD1	SD0	Sets the display mode of static display symbol SD1, SD0 = 0, 0 (display OFF), 0, 1 (1 - 2 Hz blink), 1, 0 (3 4 Hz blink), 1, 1 (all display ON)
(3) Display ON/OFF Control	0	0	0	0	1	1	C	B	DC	D	Sets cursor ON/OFF (C), cursor blink ON//OFF (B), double cursor ON/OFF (DC) and display ON/OFF (D). C = 1 (cursor ON) 0 (cursor OFF), B = 1 (blink ON) 0 (blink OFF) DC = 1 (double cursor ON) 0 (double cursor OFF), D = 1 (display ON) D = 0 (display OFF)
(4) Power Save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (0). PS = 1 (power save ON) 0 (power save OFF), 0 = 1 (oscillating circuit ON) 0 (oscillating circuit OFF)
(5) Power Control	0	0	0	1	0	1	0	VC	VF	P	Sets voltage regulating circuit ON/OFF and boosting circuit ON/OFF (P). VC = 1 (voltage regulating circuit ON) 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) 0 (voltage follower OFF), P = 1 (boosting circuit ON) 0 (boosting circuit OFF)
(6) System Set	0	0	0	1	1	0	N2	N1	*	CG	Sets the use or non-use of CG RAM and display lines (N2, N1). CG = 1 (use of CG RAM) 0 (non-use of CG RAM), N2, N1 = 0, 0 (2 lines) 0, 1 (3 lines) 1, 0 (4 lines)
(7) Electronic Volume Register	0	0	0	1	1	1	MSB			LSB	Sets the electronic volume register value.
(8) RAM Address Set	0	0	1	ADDRESS							Sets the DD RAM, CG RAM or symbol register address.
(9) RAM Write	1	0	DATA								Writes data into the DD RAM, CG RAM or symbol register address.
(10) NOP	0	0	0	0	0	0	0	0	0	0	Non-operation command
(11) Test Mode	0	0	0	0	0	0	1	0	1	0	Command for IC chip test. Don’t use this command.

CHARACTER GENERATOR

Character Generator ROM (CG ROM)

The SED1230 Series is provided with a character generator ROM consisting of a up to 256-type characters. Each character size is 5 × 7 dots.

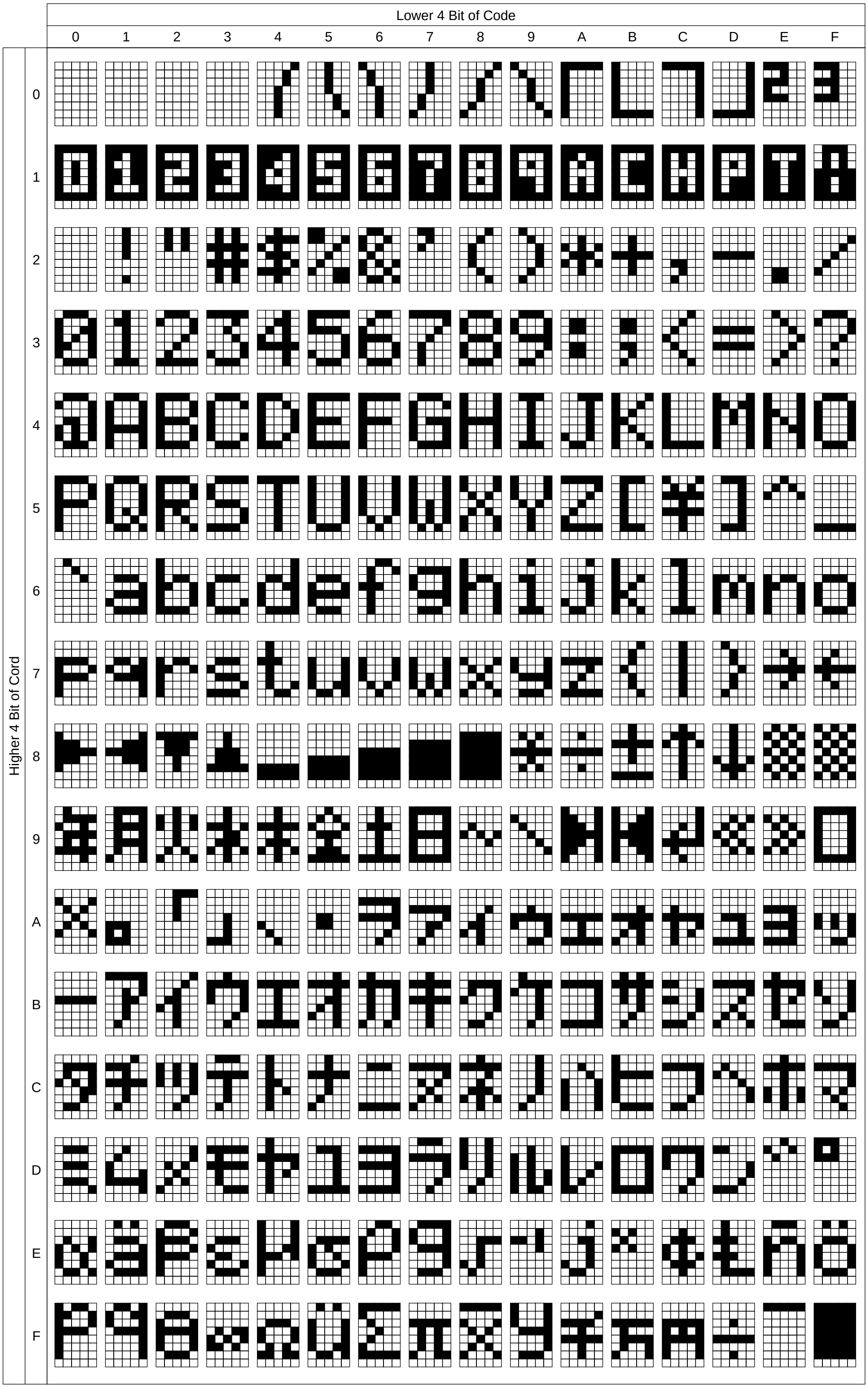
Table 5 shows a character code table of the SED1230 Series.
The 4 characters of character codes 00H to 03H are set by the System Set command to specify for which of CG ROM and CG RAM they are to be used.

The CG ROM of the SED1230 Series is a mask ROM and compatible with the user-dedicated CG ROM. Please ask us for further information of it.

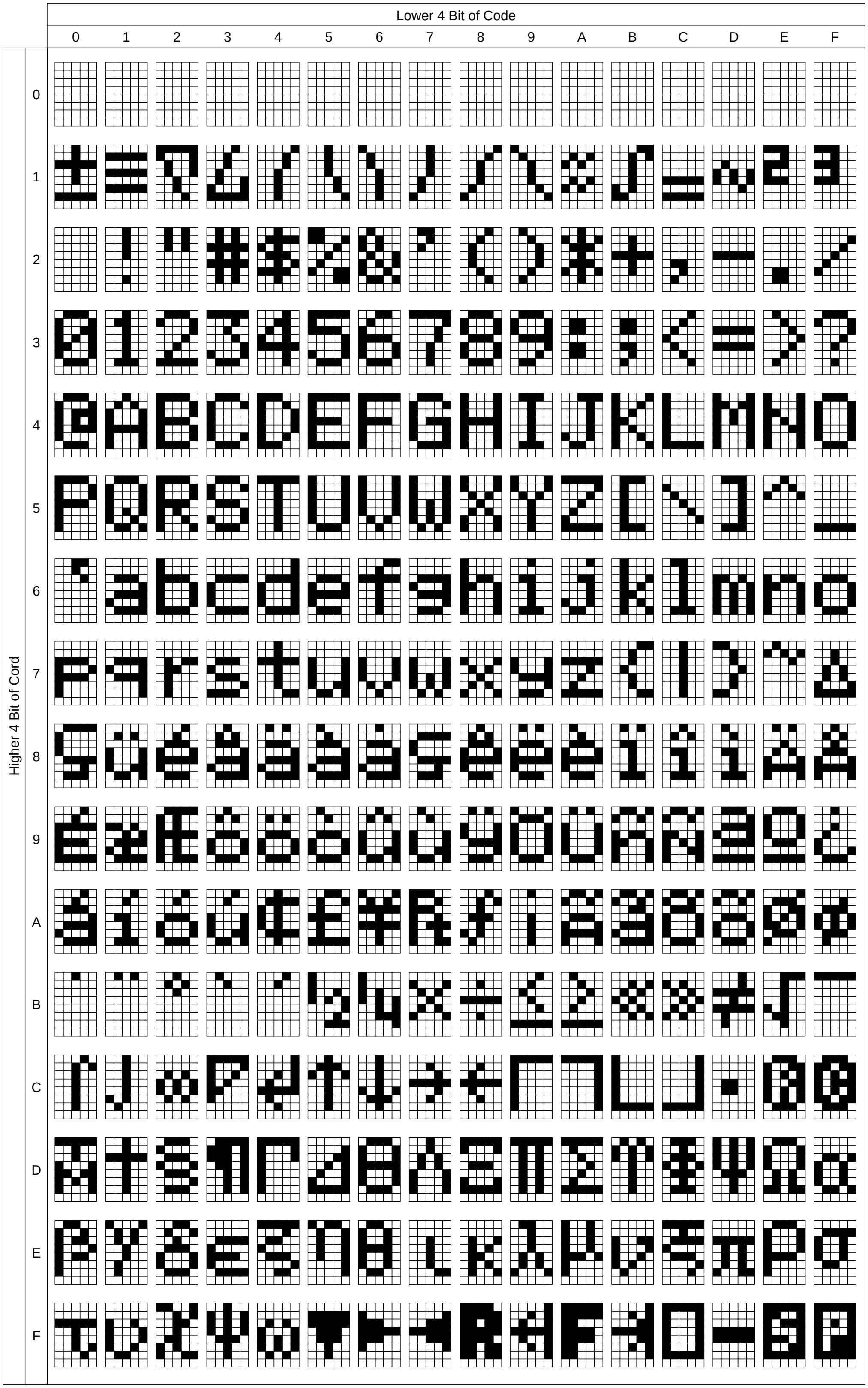
Regarding changed CG ROM, it is defined in product name as follows:

(Example) S E D 1 2 3 0 D 0 B
↑
Digit for CG ROM pattern change

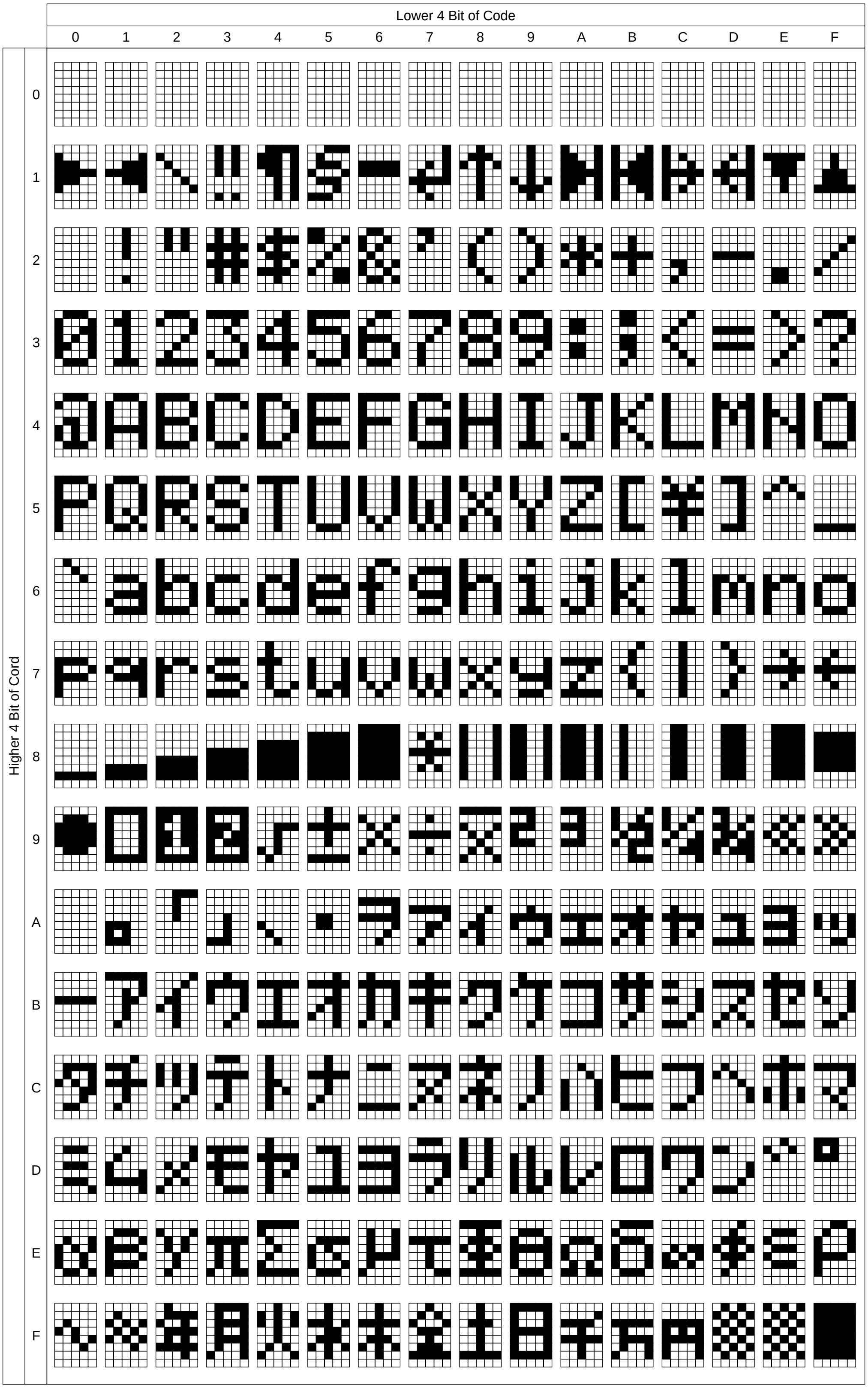
SED123✱ DA✱ Table 5



SED123* DB*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

SED123* DG*



Character Generator RAM (CG RAM)

The SED1230 Series is provided with a CG RAM that permits user-programming character patterns so that they can be displayed with a high degree of freedom for signal display.

Before using the CG RAM, select the use of CG RAM by the System Set command.

The capacity of the CG RAM is 140 bits and arbitrary patterns of 4 types consisting of 5 × 7 dots can be registered.

The relationship among CG RAM patterns, CG RAM addresses, and character codes is shown below.

Character code	RAM address		CGRAM data (character pattern)								Display
			D7							D0	
00H 02H	00H~06H 10H~16H	0	*	*	*	0	1	1	1	1	□■■■■
		1	*	*	*	1	0	0	0	0	■□□□□
		2	*	*	*	1	0	0	0	0	■□□□□
		3	*	*	*	0	1	1	1	1	□■■■■
		4	*	*	*	0	0	0	0	1	□□□□■
		5	*	*	*	0	0	0	0	1	□□□□■
		6	*	*	*	1	1	1	1	0	■■■■□
01H 03H	08H~0EH 18H~1EH	8	*	*	*	0	0	1	0	0	□□■□□
		9	*	*	*	0	0	1	0	0	□□■□□
		A	*	*	*	0	1	1	1	0	□■■■□
		B	*	*	*	0	1	1	1	0	□■■■□
		C	*	*	*	0	1	1	1	0	□■■■□
		D	*	*	*	1	1	1	1	1	■■■■■
		E	*	*	*	1	1	1	1	1	■■■■■

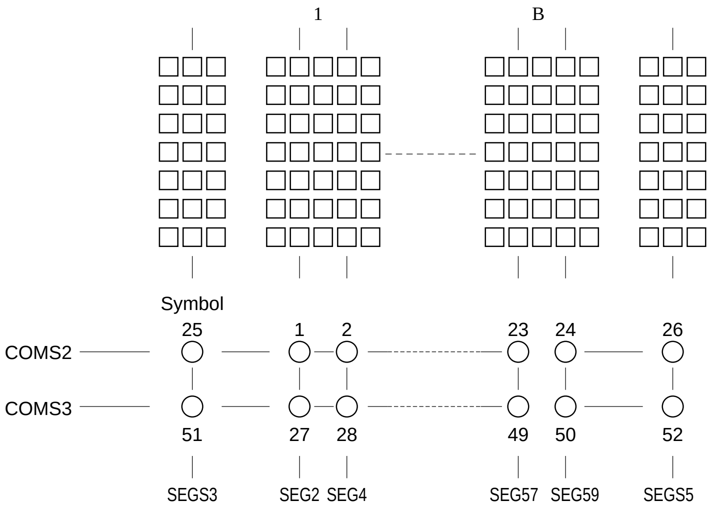
Unused (D7–D5)

Character data (D4–D0)
1: Display
0: Non-display

Symbol Register

The SED1230 Series is provided with a symbol register that permits displaying each symbol so that symbol display may be performed on the screen.
The capacity of the symbol register is 64 bits. In case of 12 digits, 48 symbols can be displayed. In case of 16 digits, 64 symbols can be displayed.
The relationship among symbol register display patterns, RAM addresses and write data is shown below.

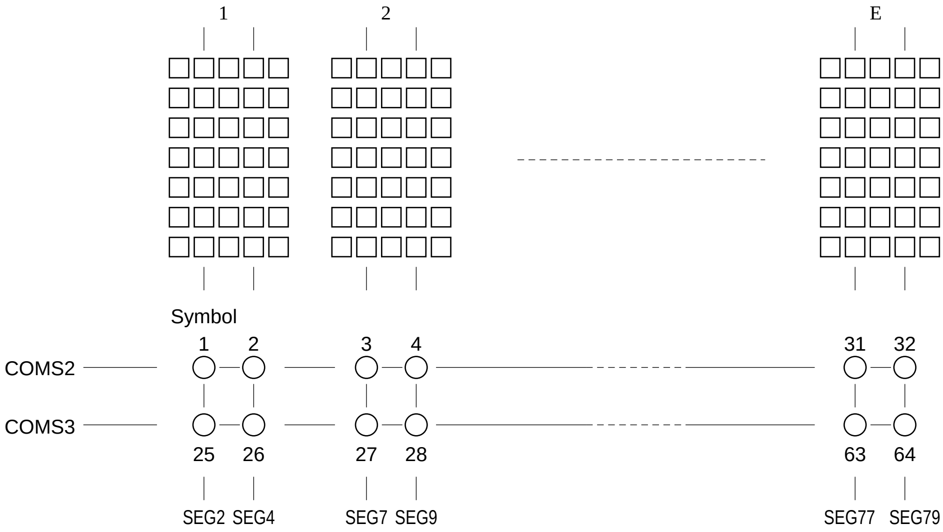
(1) SED1230, SED1231, SED1232



RAM address		Symbol Bits							
		D7							D0
70H~7CH	0	*	*	*	27	1	28	2	*
	1	*	*	*	29	3	30	4	*
	:	:							
	B	*	*	*	49	23	50	24	*
	C	*	*	*	51	25	52	26	*

Bit
1: Display
0: Not display

(2) SED1233



RAM address		Symbol Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
70H~7FH	0	*	*	*	33	1	34	2	*
	1	*	*	*	35	3	36	4	*
	:	:							
	E	*	*	*	61	29	62	30	*
	F	*	*	*	63	31	64	32	*

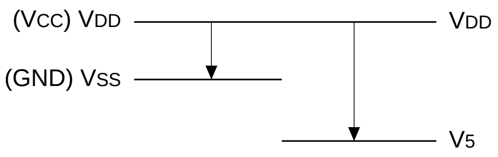
Bit
1: Display
0: Not display

Notes 1: If the symbol segment size is 1.5 times or more greater than the other dots, it is recommended to be divided into COMS2 and COMS3 and driven separately.

2: The segments other than symbol display must not be crossed through COMS2 or COMS3. The COMS3 symbol register must be set to all zeros if crossing.

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	–6.0~+0.3	V
Power supply voltage (2)		V_5	–12.0~+0.3	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	V_5~+0.3	V
Input voltage		V_{IN}	V_{SS}–0.3~+0.3	V
Output voltage		V_O	V_{SS}–0.3~+0.3	V
Operating temperature		T_{opr}	–30~+85	°C
Storage temperature	TCP	T_{str}	–55~+100	°C
	Bare chip		–65~+125	



Notes: 1. All the voltage values are based on V_{DD} = 0 V.
2. For voltages of V_1, V_2, V_3 and V_4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

DC CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.

Item		Symbol	Condition		min	typ	max	Unit	Applicable pin
Power supply voltage (1)	Recommended operation	V_{SS}			–3.6	–3.0	–2.4	V	V_{SS}
	Operable				–5.5	–3.0	–2.4		*1
Power supply voltage (2)	Recommended operation	V_5			–8.0		–5.0	V	V_5
	Operable				–11.0		–4.5		*2
	Operable	V_1, V_2			0.6×V_5		V_{DD}	V	V_1, V_2
	Operable	V_3, V_4			V_{DD}		0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHC}			0.2×V_{SS}		V_{DD}	V	*3
Low-level input voltage		V_{ILC}			V_{SS}		0.8×V_{SS}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS} –1.0			1.0	μA	*3	
LC driver ON resistance		R_{ON}	Ta=25°C ΔV=0.1V	V_5=–7.0V		20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}				0.1	5.0	μA	V_{DD}
Dynamic current consumption		I_{DD}	Display state	V_5 = –7 V without load			100	μA	V_{DD} *5
			Standby state	Oscillation ON, Power OFF			20	μA	V_{DD} *6
			Sleep state	Oscillation OFF, Power OFF			5	μA	V_{DD}
			Access state	f_{cyc}=200KHz			500	μA	V_{DD} *7
Frame frequency		f_{FR}	Ta=25°C	V_{SS}=–3.0V	70	100	130	Hz	*11
Input pin capacity		C_{IN}	Ta=25°C	f=1MHz		5.0	8.0	pF	*3

Item	Symbol	Condition	min	typ	max	Unit	Applicable pin
Reset time	t_R		1.0			μs	*8
Reset pulse width	t_{RW}		10			μs	*9
Reset start time	t_{RES}		50			ns	*9

Item		Symbol	Condition	min	typ	max	Unit	Applicable pin
Built-in power supply	Input voltage	V_{SS}		–3.6		–2.4	V	*10
	Booster output voltage	V_{OUT}	Double boosting state	–7.2			V	V_{OUT}
			Triple boosting state	–10.8				
	Voltage follower operating voltage	V_5		–11.0		–4.5	V	
	Reference voltage (standard)	V_{REG}	Ta = 25°C	–3.5	–3.1	–2.7	V	*12
	Reference voltage (option 1)	$V_{REG(VS1)}$	Ta = 25°C	–2.4	–2.1	–1.8	V	*12
	Reference voltage (option 2)	$V_{REG(VSS)}$	Ta = 25°C	V_{SS}	V_{SS}	V_{SS}	V	*12

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

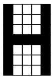
*2: The operating voltage range is applicable to the case where an external power supply is used.

*3: D0 ~ D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).

R_{ON} = 0.1 V / ΔI

(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Character "  " display. This is applicable to the case where no access is made from the MPU and the built-in power circuit and oscillating circuit are in operation.

*6: This is applicable to the case where the built-in power circuit is OFF and the oscillating circuit is in operation in the standby mode.

*7: Current consumption when data is always written by f_{cyc}.
The current consumption in the access state is almost proportional to the access frequency (f_{cyc}).
When no access is made, only I_{DD} (I) occurs.

*8: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the SED123✻ usually enters the operating state after t_R.

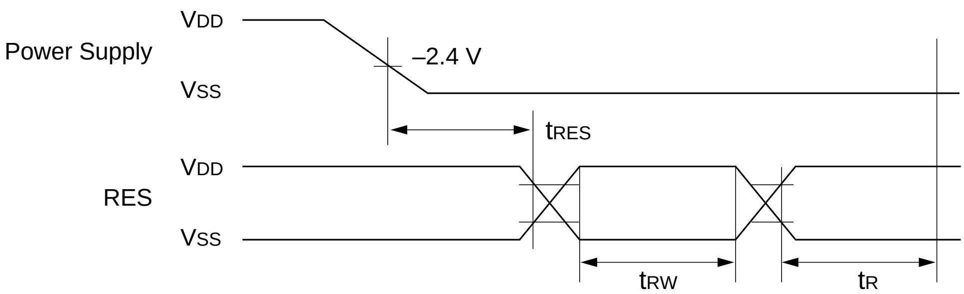
*9: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.

*10: When operating the boosting circuit, the power supply V_{SS} must be used within the input voltage range.

*11: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}
Example: The SED1230 has 13 digits of display and 1/30 duty.
$f_{OSC} = 13 \times 30 \times 100 = 39$ kHz
$f_{BST} = (1/2) \times (1/13) \times 39$ K = 1.5 kHz

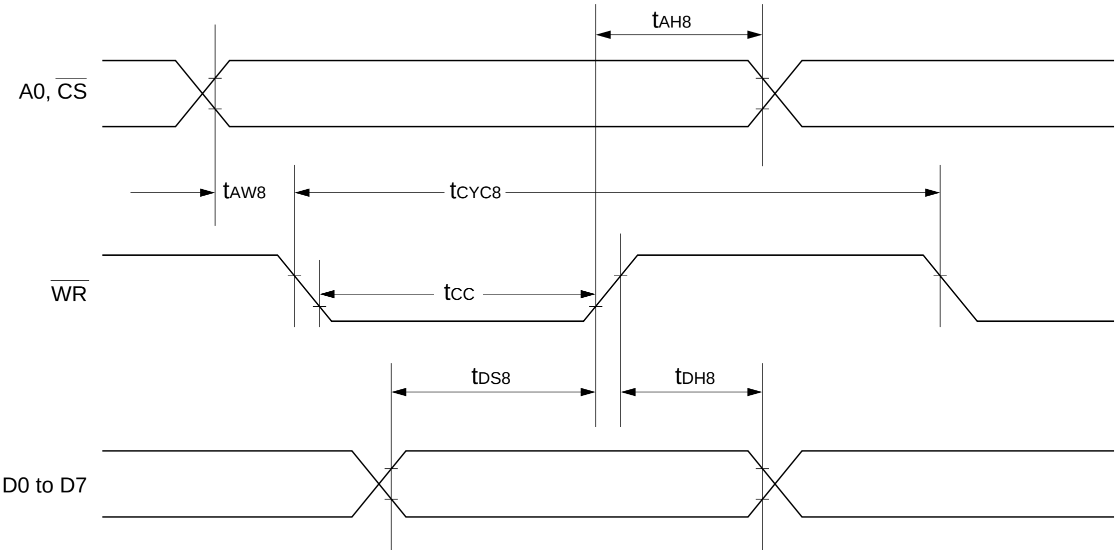
*12: The V_{REG} reference voltage has the temperature characteristics of approximately –0.17%/°C (standard specifications). An optional model having the temperature characteristics of approximately –0.04%/°C is also available. The voltage of power supply terminal V_{SS} can be selected as the reference power supply as an option without using the reference voltage inside the IC. In this case, however, a regulator is used for the external power supply (V_{DD} – V_{SS}). The voltage accuracy of V5 depends on that of the regulator used. The CGROM modification rules apply to the optional models.



All signal timings are based on 20% and 80% of V_{SS} signals.

TIMING CHARACTERISTICS

(1) System Bus Write Characteristic I (80 series MPU)

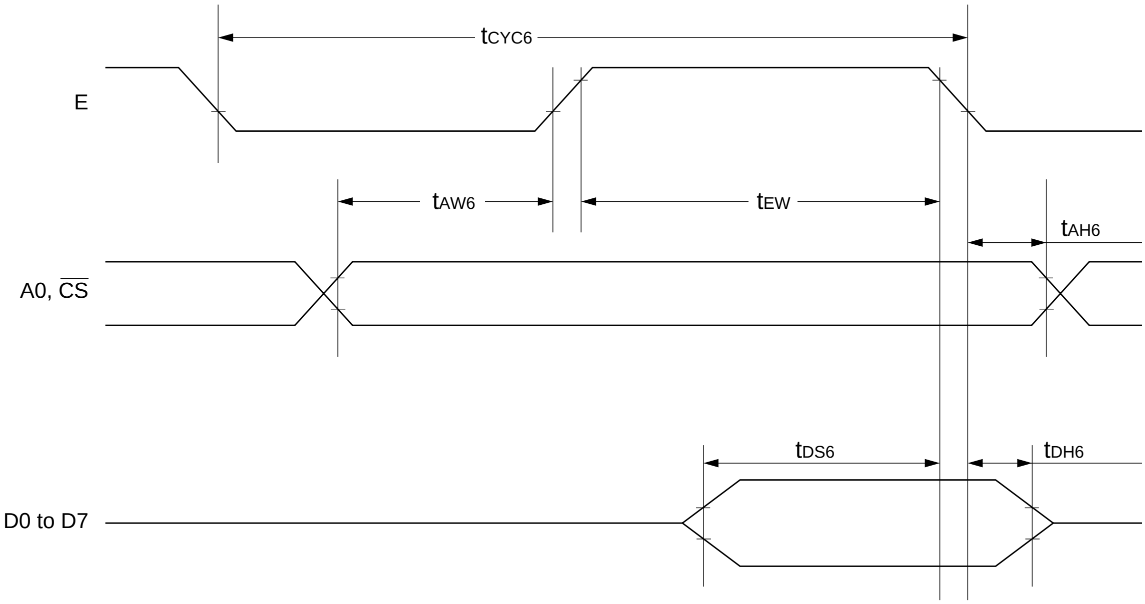


[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		30		ns
Address setup time		t_{AW8}		60		ns
System cycle time	$\overline{WR}$	t_{CYC8}	VSS = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Control pulse width ($\overline{WR}$)		t_{CC}	VSS = –3.0	100		ns
			–2.7	120		
			–2.4	150		
Data setup time	D0 ~ D7	t_{DS8}		100		ns
Data hold time		t_{DH8}		50		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of VSS.
*3: For A0 and $\overline{CS}$, the same time is not required. Input signals so that A0 and $\overline{CS}$ may satisfy t_{AW8} and t_{AH8} respectively.

(2) System Bus Write Characteristic II (68 series MPU)

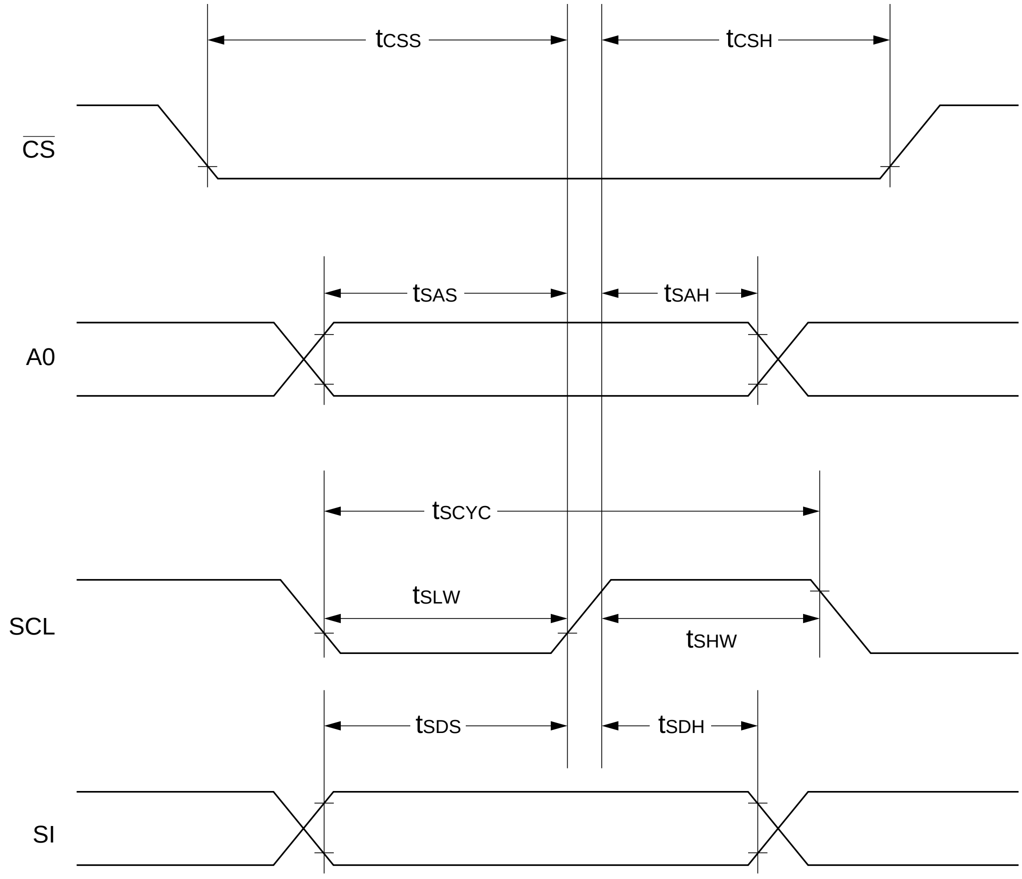


[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, CS	t CYC6	VSS = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Address setup time		t AW6		60		
Address hold time		t AH6		30		ns
Data setup time	D0 ~ D7	t DS6		100		ns
Data hold time		t DH6		50		ns
Enable pulse width	E	t EW	VSS = –3.0	100		ns
			–2.7	120		
			–2.4	150		

*1: tCYC6 denotes the cycle of the E signal in the CS active state. tCYC6 must be reserved after CS becomes active.
*2: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*3: Every timing is specified on the basis of 20% and 80% of VSS.
*4: For A0 and CS, the same timing is not required. Input signals so that A0 and CS may satisfy tAW6 and tAH6 respectively.

(3) Serial Interface



[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C]

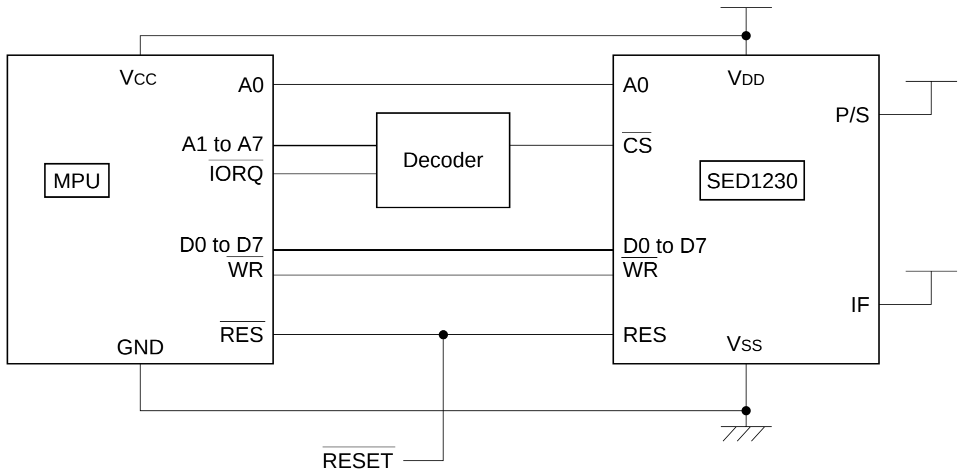
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	VSS = –3.0	700		ns
			–2.7	800		ns
			–2.4	1000		ns
SCL "H" pulse width		tSHW		300		ns
SCL "L" pulse width		tSLW		300		ns
Address setup time	A0	tSAS		50		ns
Address hold time		tSAH	VSS = –3.0	350		ns
			–2.7	400		ns
			–2.4	500		ns
Data setup time	SI	tSDS		50		ns
Data hold time		tSDH		50		ns
CS-SCL time	CS	tCSS		150		ns
		tCSH	VSS = –3.0	550		ns
			–2.7	650		ns
			–2.4	700		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of VSS.

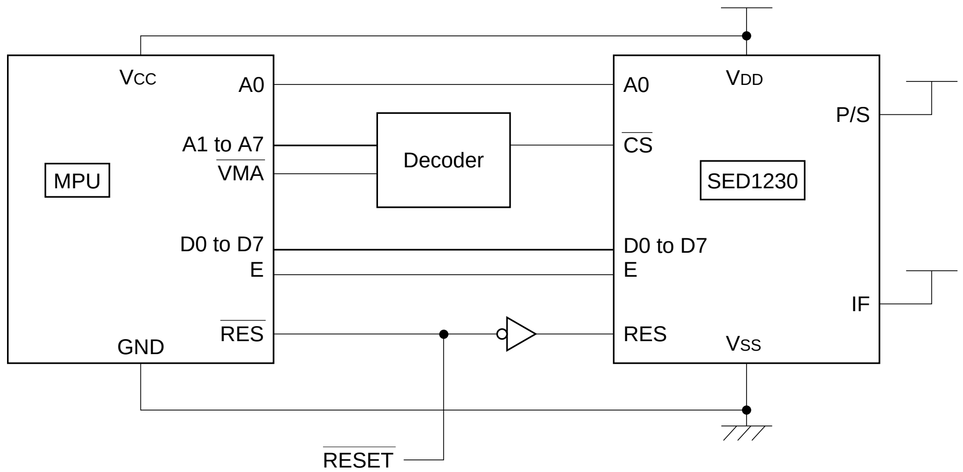
MPU INTERFACE (REFERENCE EXAMPLES)

The SED1230 Series can be connected to the 80 series MPU and 68 series MPU. When an serial interface is used, the SED1230 Series can be operated by less signal lines.

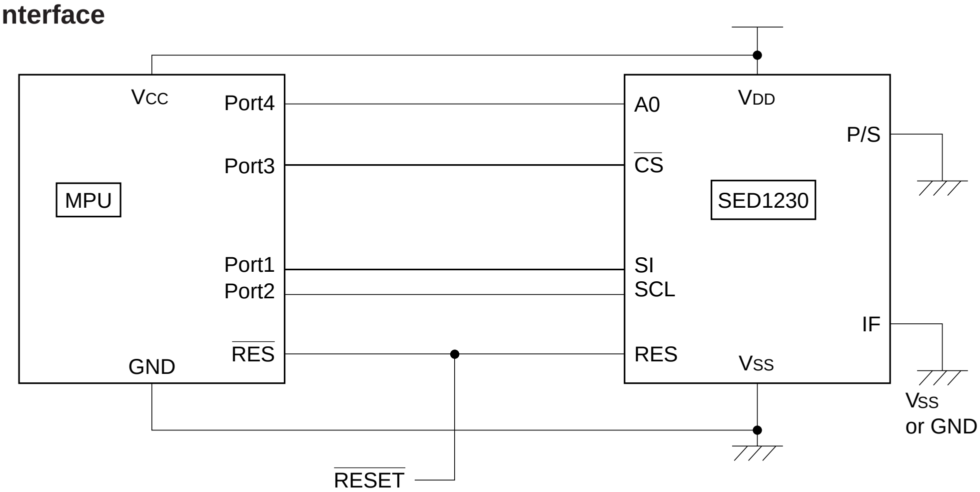
80 Series MPU



68 Series MPU

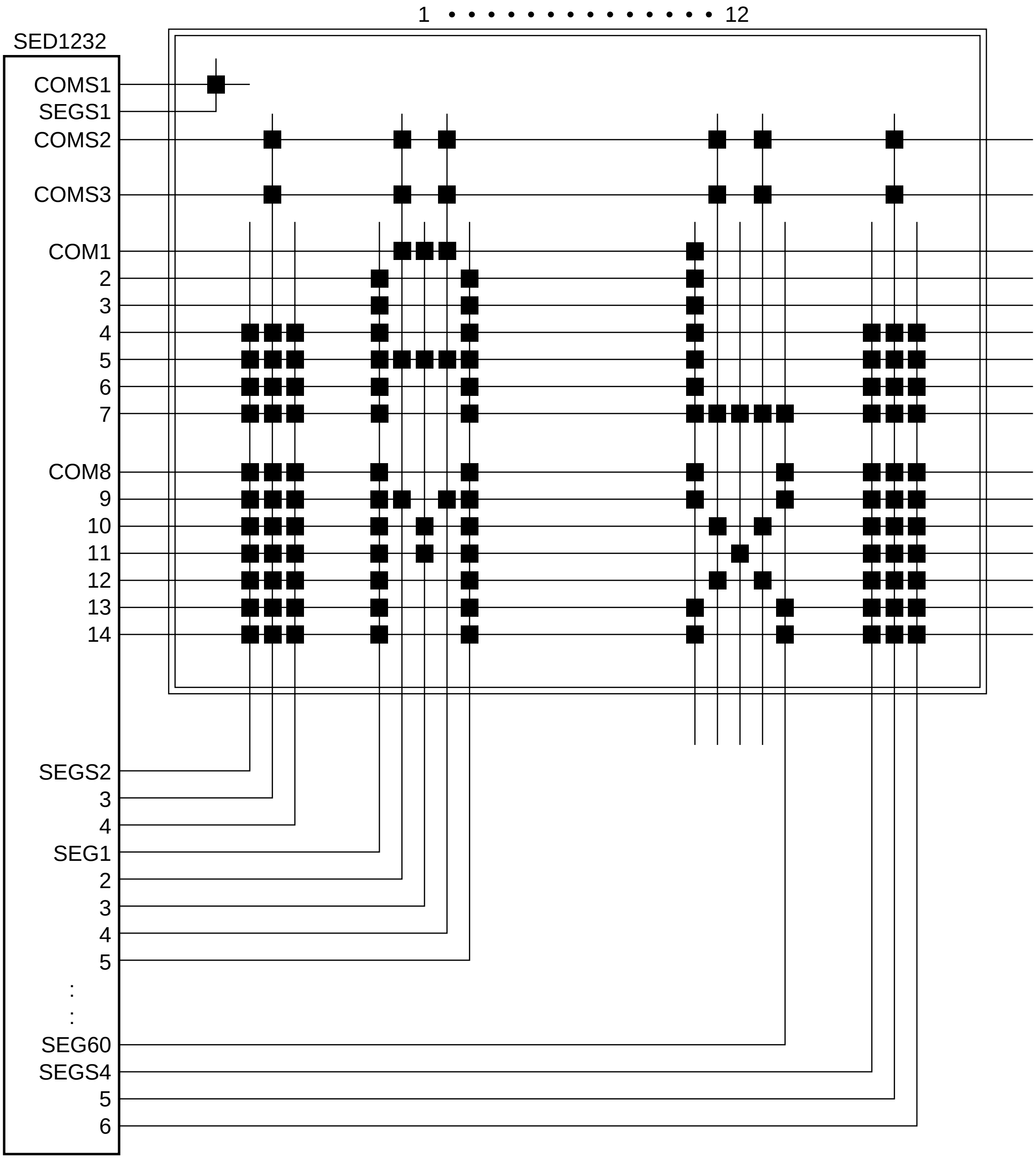


Serial Interface



INTERFACE TO LCD CELLS (REFERENCE)

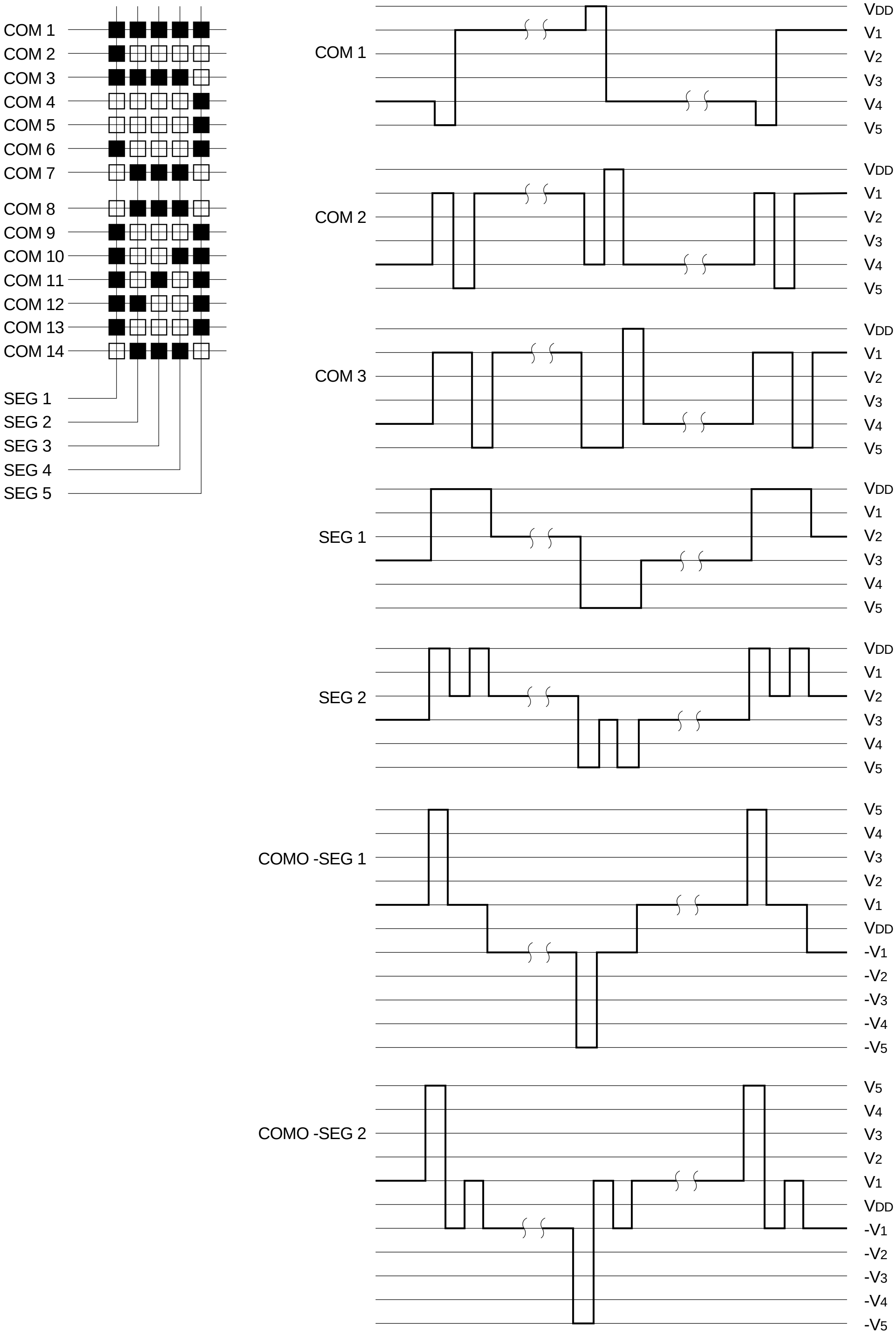
12 columns by 2 lines, 5 × 7-dot matrix segments and symbols



■ **System Setup**

N2	N1
0	0

LIQUID CRYSTAL DRIVE WAVEFORMS (B WAVEFORMS)



Instruction Setup Example (Reference Only)

(1) Initial setup

- VDD-VSS power ON
- Power regulation
- Input of reset signal
- Command status
  - • Static display control : Off
  - • Display on/off control : Off
  - • Power save : Off
  - • Power control : Off
  - • System reset : CG=0
  - • Others are undefined.
- Waiting for 10 μsec or more
- Command input: (Asterisk indicates any command sequence.)
  - (1) System setup command
  - (*) Static display control command (Valid in Standby mode only)
  - (*) Display on/off control command
    - • D: On (Display)
  - (*) Electronic volume register setup
    - • Data: (0, 0, 0, 0)
  - (*) Power save command
    - • PS: Off (Power save)
    - • O: On (Oscillation)
  - (6) RAM address setup (Note 1)
  - (7) Data writing (Note 1)
- Waiting for 20 msec or more
- Command input
  - (8) Power control commands
    - • P, VF, VC: On
- Command input:
  - (9) Electronic volume register setup
    - • Data: Appropriate value
- End of initialization

(2) Display mode

- End of initialization
- Input of RAM address setup command
- Input of RAM (data) write command
- Display of written data

Note 1: Commands (6) and (7) initialize the RAM. The display contents must first be set. The non-display area must satisfy the following conditions (for RAM clear).
• DDRAM: Write the 20H data (character code).
• CGRAM: Write the 00H data (null data).
• Symbol register: Write the 00H data (null data).
As the RAM data is unstable during reset signal input (after power-on), null data must be written. If not, unexpected display may result.

(3-1) Selecting the Standby mode

End of initialization

Normal operation
(Power Save is released and oscillator circuit is turned ON.)

Command input:
(1) Display on/off control command (Note 2)
- D: Off (Display)
(2) Power save command (Note 2)
- PS: On (Power save)
- O: On (Oscillation)
(3) Power control commands
- P, VF, VC: Off

Standby status

Static display control commands can be used.

(3-2) Releasing the Standby mode

Standby mode

Command input:
(1) Display on/off control command (Note 2)
- D: On (Display)
(2) Power save command (Note 2)
- PS: Off (Power save)
- O: On (Oscillation)

Input of electronic volume register command
- Data: (0, 0, 0, 0)

Input of power control commands
- P, VF, VC: Off

Input of electronic volume register command
- Data: Appropriate value

Return to normal operation (initial status).

Note 2: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

(4-1) Selecting the Sleep mode

End of initialization

Normal operation
(Power Save is released and oscillator circuit is turned ON.)

Command input:
(1) Display on/off control command (Note 3)
- D: Off (Display)
(2) Power save command (Note 3)
- PS: On (Power save)
- O: Off (Oscillation)
(3) Power control commands
- P, VF, VC: Off

Enter the Sleep mode.

(4-2) Releasing the Sleep mode

Sleep mode

Command input:
(1) Display on/off control command (Note 3)
- D: On (Display)
(2) Power save command (Note 3)
- PS: Off (Power save)
- O: On (Oscillation)

Wait for 20 msec or more.

Input of electronic volume register command
- Data: (0, 0, 0, 0)

Input of power control commands
- P, VF, VC: On

Input of electronic volume register command
- Data: Appropriate value

Return to normal operation
(initial status).

Note 3: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

SED1234/35 Series
LCD Controller/Drivers

Technical Manual

Contents

OVERVIEW

The SED1234, 1235 Series is a dot matrix LCD controller driver for character display, and can display a maximum of 48 characters, 4 user-defined characters, and a maximum of 48 symbols by means of 4-bit, 8-bit or serial data sent from a microcomputer.

A built-in character generator ROM is prepared for 256 character types, and each character font consists of 5 × 7 dots. A user-defined character RAM for four characters of 5 × 7 dots are incorporated, and a symbol register is also incorporated. With these, it is possible to apply this Series to display with a high degree of freedom. This Series can operate handy units with a minimum power consumption by means of its low power consumption and sleep mode.

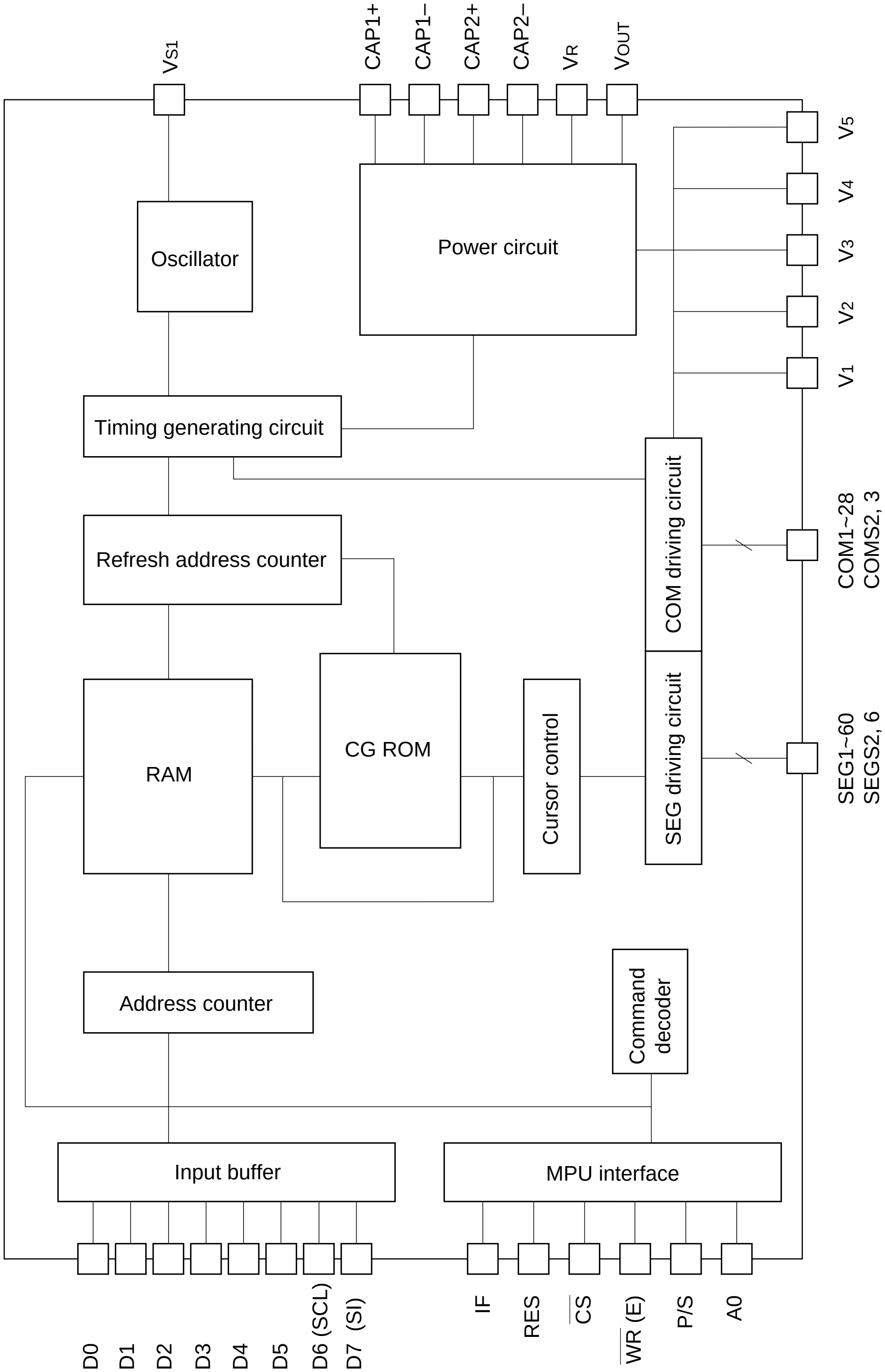
SED1234, and 1235 depending on the duty of use and the number of display columns.

FEATURES

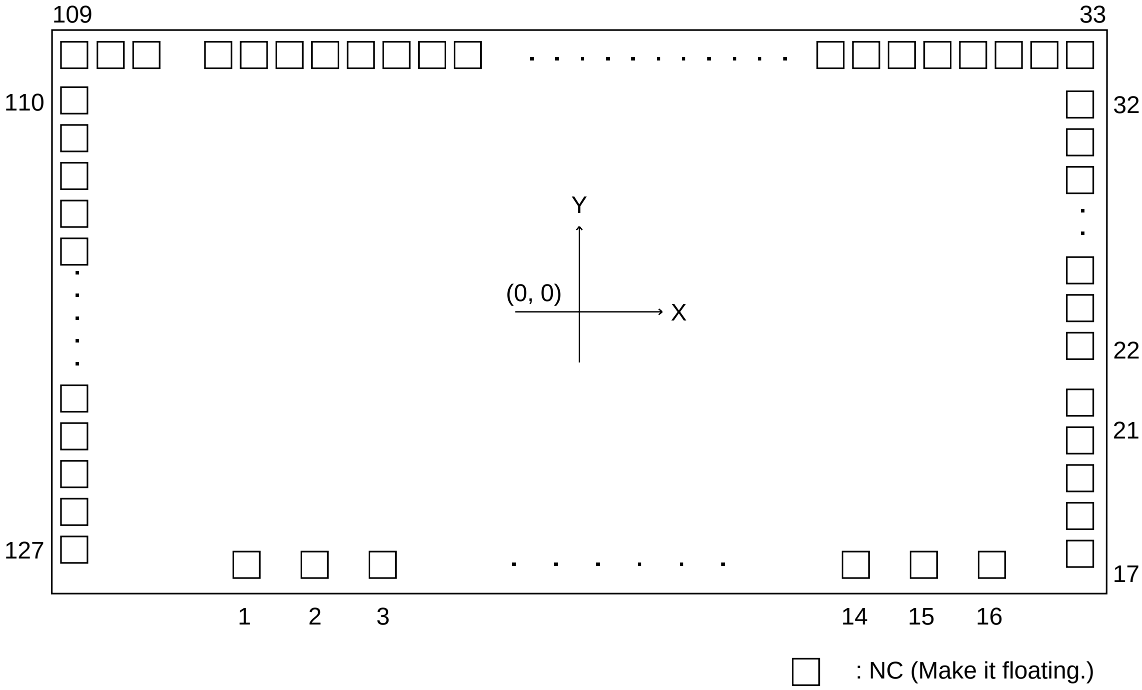
- Built-in diplay RAM
  48 characters + 4 user-defined characters + 48 symbols
- CG ROM (for up to 256 characters), CG RAM (4 characters), and symbol register (48 symbols)
- Number of display columns × number of lines
  (12 columns + 2 segment for signal) × 4 lines + 48 symbols: SED1234
  (12 columns + 2 segment for signal) × 2 lines + 48 symbols: SED1235
- CR oscillation circuit (on-chip C and R)
- High-speed MPU interface
  Interfacing with both 68 series and 80 series MPU
  Interfacing in 4 bits/8 bits
- Serial interface
- Character font 5 × 7 dots
- Duty ratio 1/16 (SED1235)
  1/30 (SED1234)
- Simple command setting
- Built-in liquid crystal driving power circuit
  Power boosting circuit, power regulating circuit, voltage follower × 4
- Built-in electronic volume function
- Low power consumption
  100 µA Max. (In normal operation mode: Including the operating current of the built-in power supply)
- Power supply
  V_{DD} - V_{SS} (logic section): –2.4 V to –3.6 V
  V_{DD} - V_5 (liquid crystal drive section)
  : –5.0 V to –8.0 V
- Wide operating temperature range
  Ta = -30 to 85°C
- CMOS process
  (Pad Pitch)
- COB assemble 126 µm min.
- Delivery form: Chip SED123✻D✻A, SED123✻D✻C
- This IC is not designed with a protection against radioactive rays.

SED1234/35 Series

BLOCK DIAGRAM



SED1234/35 SERIES, CHIP SPECIFICATION



SED1234D** 1/30 duty
SED1235D** 1/16 duty
#1 Column for CG ROM pattern change

Chip size: 10.23 × 3.11 mm
Pad pitch: 126 µm (Min.)
Chip thickness: 625 ± 25 µm (SED123∗D∗A)
525 ± 25 µm (SED123∗D∗C)

1) A1 pad specification
Pad size: A 91 µm × 90 µm
B 114 µm × 114 µm

<SED1234D$_{**}$> (1/2)

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	V_{DD}	–4077	–1371
2	V_{SS}	–3526	
3	V_5	–2975	
4	V_4	–2424	
5	V_3	–1855	
6	V_2	–1287	
7	V_1	–719	
8	V_0	–151	
9	V_R	400	
10	V_{OUT}	968	
11	CAP2–	1519	
12	CAP2+	2070	
13	CAP1–	2638	
14	CAP1+	3189	
15	V_{SS}	3757	
16	V_{DD}	4308	
17	(NC)	4883	
18	(NC)	4883	
19	(NC)	4883	
20	(NC)	4883	
21	V_{S1}	4929	
22	P/S	4924	
23	IF	4924	
24	RES	4924	
25	COMS2	4950	
26	COM1	4950	
27	COM2	4950	
28	COM3	4950	
29	COM4	4950	
30	COM5	4950	
31	COM6	4950	
32	COM7	4950	
33	COM8	4896	
34	COM9	4769	
35	COM10	4642	
36	COM11	4515	
37	COM12	4388	
38	COM13	4262	
39	COM14	4135	
40	SEGS2	4008	
41	SEG1	3881	
42	SEG2	3754	
43	SEG3	3627	
44	SEG4	3501	
45	SEG5	3374	
46	SEG6	3247	
47	SEG7	3120	
48	SEG8	2993	
49	SEG9	2866	
50	SEG10	2740	
51	SEG11	2613	
52	SEG12	2486	
53	SEG13	2359	
54	SEG14	2232	↓

PAD		COORDINATES	
No.	Name	X	Y
55	SEG15	2106	1406
56	SEG16	1979	
57	SEG17	1852	
58	SEG18	1725	
59	SEG19	1598	
60	SEG20	1471	
61	SEG21	1345	
62	SEG22	1218	
63	SEG23	1091	
64	SEG24	964	
65	SEG25	837	
66	SEG26	710	
67	SEG27	584	
68	SEG28	457	
69	SEG29	330	
70	SEG30	203	
71	SEG31	76	
72	SEG32	–51	
73	SEG33	–177	
74	SEG34	–304	
75	SEG35	–431	
76	SEG36	–558	
77	SEG37	–685	
78	SEG38	–812	
79	SEG39	–938	
80	SEG40	–1065	
81	SEG41	–1192	
82	SEG42	–1319	
83	SEG43	–1446	
84	SEG44	–1572	
85	SEG45	–1699	
86	SEG46	–1826	
87	SEG47	–1953	
88	SEG48	–2080	
89	SEG49	–2207	
90	SEG50	–2333	
91	SEG51	–2460	
92	SEG52	–2587	
93	SEG53	–2714	
94	SEG54	–2841	
95	SEG55	–2968	
96	SEG56	–3094	
97	SEG57	–3221	
98	SEG58	–3348	
99	SEG59	–3475	
100	SEG60	–3602	
101	SEGS6	–3729	
102	COM28	–3855	
103	COM27	–3982	
104	COM26	–4109	
105	COM25	–4236	
106	COM24	–4363	↓
107	COM23	–4679	1405
108	COM22	–4806	1405

<SED1234D**> (2/2)

PAD		COORDINATES	
No.	Name	X	Y
109	COM21	–4933	1405
110	COM20	–4964	1094
111	COM19		966
112	COM18		839
113	COM17		712
114	COM16		584
115	COM15		457
116	COMS3		330
117	A0		202
118	$\overline{WR}$		75
119	$\overline{CS}$		–52
120	D7		–180
121	D6		–307
122	D5		–434
123	D4		–562
124	D3		–689
125	D2		–816
126	D1		–943
127	D0	↓	–1071

<SED1235D**> (1/2)

Unit: µm

PAD		COORDINATES		PAD		COORDINATES	
No.	Name	X	Y	No.	Name	X	Y
1	V_{DD}	–4077	–1371	55	SEG15	2106	–1406
2	V_{SS}	–3526		56	SEG16	1979	
3	V_5	–2975		57	SEG17	1852	
4	V_4	–2424		58	SEG18	1725	
5	V_3	–1855		59	SEG19	1598	
6	V_2	–1287		60	SEG20	1471	
7	V_1	–719		61	SEG21	1345	
8	V_0	–151		62	SEG22	1218	
9	V_R	400		63	SEG23	1091	
10	V_{OUT}	968		64	SEG24	964	
11	CAP2–	1519		65	SEG25	837	
12	CAP2+	2070		66	SEG26	710	
13	CAP1–	2638		67	SEG27	584	
14	CAP1+	3189		68	SEG28	457	
15	V_{SS}	3757		69	SEG29	330	
16	V_{DD}	4308		70	SEG30	203	
17	(NC)	4883	–1343	71	SEG31	76	
18	(NC)	4883	–1233	72	SEG32	–51	
19	(NC)	4883	–1123	73	SEG33	–177	
20	(NC)	4883	–1013	74	SEG34	–304	
21	V_{S1}	4929	–903	75	SEG35	–431	
22	P/S	4924	–184	76	SEG36	–558	
23	IF	4924	–57	77	SEG37	–685	
24	RES	4924	70	78	SEG38	–812	
25	COMS2	4950	255	79	SEG39	–938	
26	COM1	4950	382	80	SEG40	–1065	
27	COM2	4950	510	81	SEG41	–1192	
28	COM3	4950	637	82	SEG42	–1319	
29	COM4	4950	764	83	SEG43	–1446	
30	COM5	4950	891	84	SEG44	–1572	
31	COM6	4950	1019	85	SEG45	–1699	
32	COM7	4950	1146	86	SEG46	–1826	
33	COM8	4896	1406	87	SEG47	–1953	
34	COM9	4769		88	SEG48	–2080	
35	COM10	4642		89	SEG49	–2207	
36	COM11	4515		90	SEG50	–2333	
37	COM12	4388		91	SEG51	–2460	
38	COM13	4262		92	SEG52	–2587	
39	COM14	4135		93	SEG53	–2714	
40	SEGS2	4008		94	SEG54	–2841	
41	SEG1	3881		95	SEG55	–2968	
42	SEG2	3754		96	SEG56	–3094	
43	SEG3	3627		97	SEG57	–3221	
44	SEG4	3501		98	SEG58	–3348	
45	SEG5	3374		99	SEG59	–3475	
46	SEG6	3247		100	SEG60	–3602	
47	SEG7	3120		101	SEGS6	–3729	
48	SEG8	2993		102	(NC)	–3855	
49	SEG9	2866		103	(NC)	–3982	
50	SEG10	2740		104	(NC)	–4109	
51	SEG11	2613		105	(NC)	–4236	
52	SEG12	2486		106	(NC)	–4363	
53	SEG13	2359		107	(NC)	–4679	1405
54	SEG14	2232		108	(NC)	–4806	1405

<SED1235D**> (2/2)

PAD		COORDINATES	
No.	Name	X	Y
109	COM14	–4933	1405
110	COM13	–4964	1094
111	COM12	↓	966
112	COM11		839
113	COM10		712
114	COM9		584
115	COM8		457
116	COMS3		330
117	A0		202
118	$\overline{WR}$		75
119	$\overline{CS}$		–52
120	D7		–180
121	D6		–307
122	D5		–434
123	D4		–562
124	D3		–689
125	D2		–816
126	D1		–943
127	D0		–1071

DESCRIPTION OF PINS

Power Pins

Pin name	I/O	Description	Q'ty
V_{DD}	Power supply	Logic + power pin. Also used as MPU power pin V_{CC}.	2
V_{SS}	Power supply	Logic – power pin. Connected to the system GND.	2
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined in the liquid crystal cell is resistance-divided or impedance-converted by operational amplifier, and the resultant voltage is applied. The potential is determined on the basis of V_{DD} and the following equation must be respected. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$, $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to pins V_1 to V_4 by built-in power circuit: $V_1 = 1/5\ V_5$ $V_2 = 2/5\ V_5$ $V_3 = 3/5\ V_5$ $V_4 = 4/5\ V_5$	6
V_{S1}	O	Power supply voltage output pin for oscillating circuit. Don't connect this pin to an external load.	1

LCD Power Circuit Pins

Pin name	I/O	Description	Q'ty
CAP1+	O	Capacitor positive side connecting pin for boosting. This pin connects the capacitor with pin CAP1–.	1
CAP1–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP+.	1
CAP2+	O	Capacitor positive side connecting pin for boosting. This pin connects a capacitor with pin CAP2–.	1
CAP2–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP2+.	1
V_{OUT}	O	Output pin for boosting. This pin connects a smoothing capacitor with VSS pin.	1
V_R	I	Voltage regulating pin. This pin gives a voltage between V_{DD} and V_5 by resistance-division of voltage.	1

Pins for System Bus Connection

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Q’ty</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 ~ D0</td><td>I</td><td>8-bit input data bus. These pins are connected to a 8-bit or 16-bit standard MPU data bus.
When P/S = “Low”, the D7 and D6 pins are operated as a serial data input and a serial clock input respectively.
<table>
<tr><td>P/S</td><td>D7</td><td>D6</td><td>D5 ~ D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>“Low”</td><td>SI</td><td>SCL</td><td>—</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>“High”</td><td>D7</td><td>D6</td><td>D5 ~ D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
</table></td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, this pin connects the least significant bit of the MPU address bus and identifies a data command.
0 : Indicates that D0 to D7 are a command.
1 : Indicates that D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>In case of a 68 series MPU, initialization can be performed by changing RES ↓. In case of an 80 series MPU, initialization can be performed by changing ↑.
A reset operation is performed by edge sensing of the RES signal. An interface type for the 68/80 series MPU is selected by input level after initialization.
“L” : 80 series MPU interface
“H” : 68 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal. Usually, this pin inputs the signal obtained by decoding an address bus signal. At the “Low” level, this pin is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$

(E)</td><td>I</td><td><When connecting an 80 series MPU>
Active “Low”. This pin connects the $\overline{WR}$ signal of the 80 series MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ signal.
<When connecting a 68 series MPU>
Active “High”. This pin becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin switches between serial data input and parallel data input.
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Serial Clock</td></tr>
<tr><td>“High”</td><td>$\overline{CS}$</td><td>A0</td><td>D0~D7</td><td>–</td></tr>
<tr><td>“Low”</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>Interface data length select pin for parallel data input.
“High”: 8-bit parallel input
“Low”: 4-bit parallel input
When P/S = “Low”, connect this pin to V_{DD} or V_{SS}.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

SED1234

Pin name	I/O	Description	Q’ty
COM1~ COM28	O	Common signal output pin (for characters)	28
COMS2, CMOS3	O	Common signal output pin (except for characters) CMOS2, CMOS3: Common output for symbol display	2
SEG1~ SEG60	O	Segment signal output pin (for characters)	60
SEGS2, SEGS6	O	Segment signal output pin (except for characters) SEGS2, SEGS6: Segment output for signal output	2

SED1235

Pin name	I/O	Description	Q’ty
COM1~ COM14	O	Common signal output pin (for characters) COM8~COM14:W output	14 (21)
COMS2, CMOS3	O	Common signal output pin (except for characters) CMOS2, CMOS3: Common output for symbol display	2
SEG2~ SEG60	O	Segment signal output pin (for characters)	60
SEGS2, SEGS6	O	Segment signal output pin (except for characters) SEGS2, SEGS6: Segment output for signal output	2

FUNCTIONAL DESCRIPTION

MPU Interface

Selection of interface type

In the SED1234, SED1235, data transfer is performed through a 8-bit or 4-bit data bus or a serial data input (SI). By selecting “High” or “Low” as P/S pin polarity, a parallel data input or a serial data input can be selected as shown in Table 1.

Table 1

P/S	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0~D7
“High”	Parallel Input	$\overline{CS}$	A0	$\overline{WR}$	—	—	D0~D7
“Low”	Serial Input	$\overline{CS}$	A0	—	SI	SCL	—

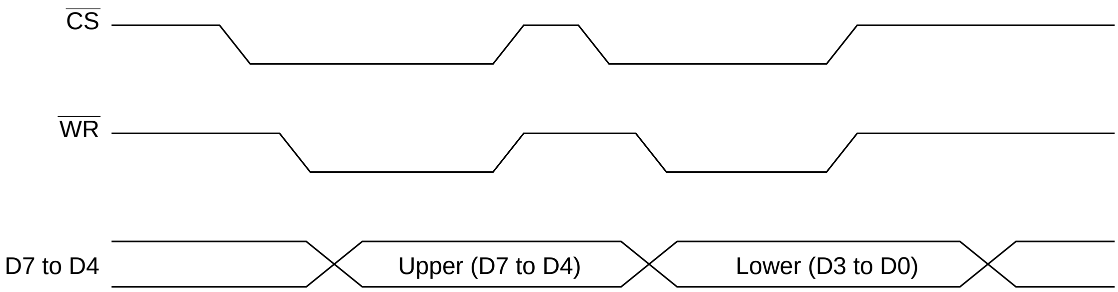
Parallel Input
In the SED1234, SED1235, when parallel input is selected (P/S = “High”), it can be directly connected to the 80 series MPU bus or 68 series MPU bus, as shown in Table 2, if either “High” or “Low” is selected as RES pin polarity after a reset input, because the RES pin has an MPU select function.
Selection between 8 bits and 4 bits is performed by command.

Table 2

RES input polarity	Type	A0	$\overline{WR}$	$\overline{CS}$	D0~D7
High-to-low active	68 series	A0	E	$\overline{CS}$	D0~D7
Low-to-high active	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0~D7

Interface with 4-bit MPU interface

When data transfer is performed by 4-bit interface (IF = 0), an 8-bit command, data and address are divided into two parts.



Note: When performing writing in succession, reverse a time exceeding the system cycle time (t_{cyc}) and then perform writing.

Serial interface (P/S = “Low”)

The serial interface consists of a 8-bit shift register and a 3-bit counter and acceptance of an SI input or SCL input is enabled in the ship selected status (CS = “Low”).
When no chip is selected, the shift register and counter are reset to the initial status.
Serial data is input in the order of D7, D6 .... D0 from the serial data input pin (SI) at the rise of Serial Clock (SCL).
At the rising edge of the 8th serial clock, the serial data is converted into 8-bit parallel data and this data is processed.
The A0 input is used to identify whether the serial data input (SI) is display data or a command. That is, when A0 = “High”, it is regarded as display data. When A0 = “Low”, it is regarded as a command.
The A0 input is read in and identified at the rise of the 8 x n-th clock of Serial Clock (SCL) after chip selection.
Fig. 1 shows a timing chart of the serial interface.
Regarding the SCL signal, special care must be exercised about terminal reflection and external noise due to a wire length.
We recommend the user to perform an operation check with a real machine.
We also recommend the user to periodically refresh the write status of each command to prevent a malfunction due to noise.

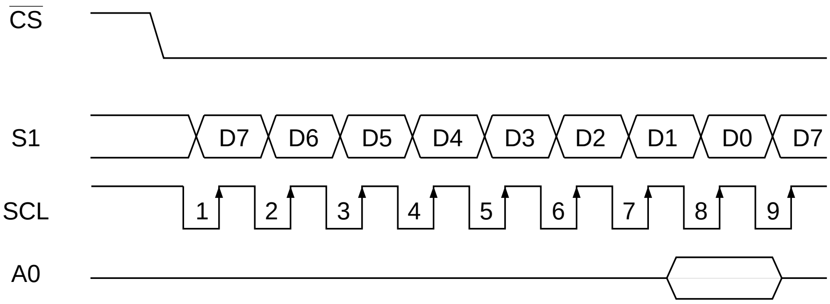


Fig. 1

Identification of data bus signals

The SED1234, SED1235 series identifies data bus signals, as shown in Table 3, by combinations of A0 and $\overline{\text{WR}}$ (E).

Table 3

Common	68 series	80 series	Function
A0	E	$\overline{\text{WR}}$	
1	1	0	Writing to RAM and symbol register
0	1	0	Writing to internal register (command)

Chip select

The SED1234, SED1235 series has a chip select pin ($\overline{\text{CS}}$). Only when $\overline{\text{CS}}$ = “Low”, MPU interfacing is enabled. In any status other than Chip Select, D0 to D7 and A0, $\overline{\text{WR}}$, SI and SCL inputs are invalidated. When a serial input interface is selected, the shift register and counter are reset.

However, the Reset signal is input regardless of the $\overline{\text{CS}}$ status.

Power Circuit

This is a low-power-consumption power circuit that generates a voltage required for liquid crystal drive.
The power circuit consists of a boosting circuit, voltage regulating circuit and voltage follower.

The power circuit incorporated in the SED1234, SED1235 Series is set for a small-scale liquid crystal panel, so that its display quality may be greatly deteriorated if it is used for a liquid crystal panel with a large display capacity.
In this case, an external power supply must be used.

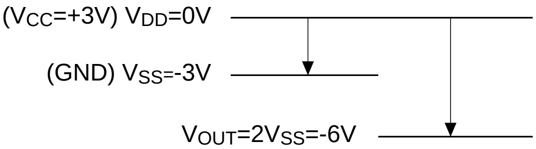
A power circuit function can be selected by power control command. With this, an external power supply and a part of the internal power supply can be used together.

	Boosting circuit	Voltage regulating circuit	Voltage follower	External voltage input	Boosting system pin
	○	○	○	—	
Note 1	×	○	○	V_{OUT}	OPEN
Note 2	×	×	○	$V_5 = V_{OUT}$	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

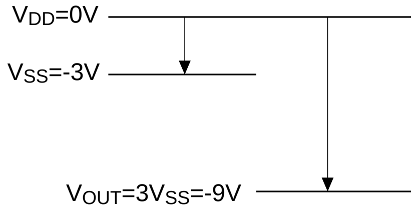
Note 1: When the boosting circuit is turned off, make boosting system pins (CAP1+, CAP1-, CAP2+, CAP2-) open and give a liquid crystal drive voltage to the V_{OUT} pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, make the boosting system pins open, connect between the V_5 pin and V_{OUT} pin, and give a liquid crystal drive voltage from the outside.
Note 3: When all the internal power supplies are turned off, supply liquid crystal drive voltages V_1, V_2, V_3, V_4 and V_5 from the outside, and make the CAP1+, CAP1-, CAP2+, CAP2- and V_{OUT} pins open.

Triple boosting circuit

When a capacitor is connected between CAP1+ and CAP1-, between CAP2+ and CAP2-, and between V_{SS} pin and V_{OUT} pin respectively, the potential between the V_{DD} pin and V_{SS} pin is boosted triple and output to the V_{OUT} pin. In case of double boosting, remove the capacitor between CAP2+ and CAP2- in connection for triple boosting operation and strap between CAP2- and V_{OUT} pin. Then, a double boosted output can be obtained from the V_{OUT} pin (CAP2-).
The boosting circuit uses a signal from the oscillator ourput.
Accordingly, it is necessary that the oscillating circuit must be in operation. The potential relationship of boosting is shown below.



Potential during double boosting



Potential during triple boosting

Voltage regulating circuit

The voltage regulation circuit regulates the boosted voltage developed at Vout. It outputs the regulated LCD driving voltage at the V_5 terminal. An internal resistor can be inserted into the regulation circuit feedback loop providing the following voltage levels at the V_5 terminal.

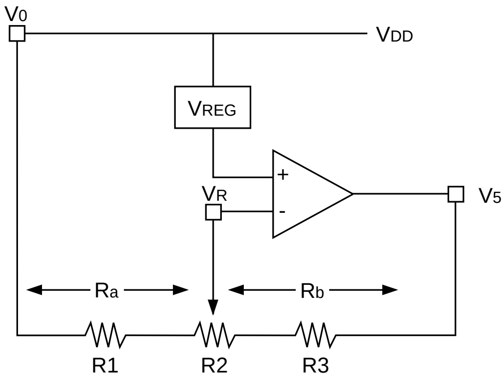
When V_5 is required to be different than the above case, leave the internal feedback resistor out of the circuit. V_5 can be regulated within a range of $|V_5|<|V_{OUT}|$. It may be calculated by the following formula:

$$V_5 = \left(1+\frac{R_b}{R_a}\right) \bullet V_{REG} \cdots\cdots\cdots\cdots\cdots (1) \cdots$$

Wherein, V_{REG} is the constant voltage source inside the SED1230 Series and the voltage is constant at $V_{REG} \fallingdotseq$ 3.1V. Voltage regulation of the V_5 output is accomplished by connecting a variable resistor between V_R, V_{DD} and V_5. For fine adjustment of the V_5 voltage, use a combination of fixed resistors R1 and R3 and a variable resistor R2.

The voltage regulator circuit carries a temperature gradient of about -0.17%/°C under V_{REG} outputs. When any other temperature gradient is required, connect a thermistor in series to the output voltage regulating register.

Since the V_R terminal has a high input impedance, it is necessary to take noise suppression measures such as shortening the input wiring and shielding the wiring run.



Example 1:
Condition: I(R1, R2, R3) ≤ 5µA V_5 = –6 to –8V

Setting: R1+R2+R3 = 8V/5µA = 1.6MΩ
8V = (1+R_b/R_a) 3.0V R_b/R_a = 1.67
6V = (1+R_b/R_a) 3.0V R_b/R_a = 1
} ···· { R1 = 600KΩ, R2 = 200KΩ, R3 = 800KΩ

● Voltage Regulation Circuit Using Electronic Contrast Control Register

The contrast control register controls the liquid crystal driving voltage (V_5). This is accomplished by an electronic volume control register set command that adjusts the contrast of the liquid crystal display (see section 1-22).

The commands provide 4-bits of voltage level data to the electronic volume control register. This provides for the selection of 16 different voltage levels for the liquid crystal driving voltage. When using the electronic volume control function, it is necessary to close the voltage regulation circuit using electronic control commands. For reference information, when the electronic volume control registor value is at (1, 1, 1, 1), the constant current value becomes: $I_{REF} \fallingdotseq 3.65\mu A$.

[An exemplary constant setting when the electronic volume control function is being used]

$$V_5 = \left(1 + \frac{R_b}{R_c}\right) \cdot V_{REG} \cdots\cdots\cdots\cdots\cdots\cdots ②$$

$$R_c = \frac{R_a \times R_I}{R_a + R_I}$$

$$R_I = \frac{V_R}{I_{REF}}$$

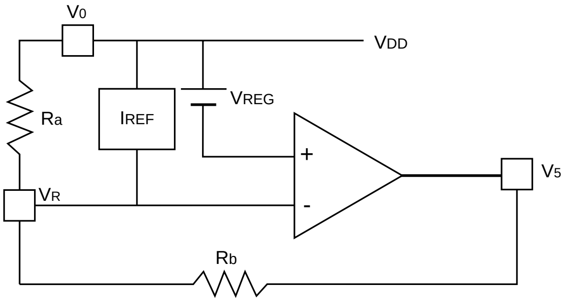


Fig. 9

(1) Determining the V_5 voltage setting range by the electronic volume control
Liquid crystal driving voltage V_5: max. -6v ~ min. -8V
V_5 variable voltage range: 2V

(2) Determinig the R_b
R_b = V_5 variable voltage range/ I_{REF}
= 2V/3.65µA
= 548KΩ

(3) Determining the R_a

$$R_a = \frac{V_{REG}}{(V_5 \text{ voltage setting max} - V_{REG}) / R_b}$$ (Use absolute values for V_{REG} and V_5 voltage settings.)

$$= \frac{3.1V}{(6V - 3.1V) / 548K\Omega}$$

= 585KΩ

(4) Regulating the R_a
Set the electronic volume control register to (D3, D2, D1, D0) = (1, 0, 0, 0) or (0, 1, 1, 1) before matching the R_a value to the optimum contrast.

Since I_{REF} is a simplified constant voltage source, fluctuations upto ± 40% must be taken into consideration, as a dispersion range during manufacture. Meanwhile, the temperature dependency of I_{REF} is : $\Delta I_{REF} \fallingdotseq -0.037\mu A/°C$. Determine the R_a and R_b for the using LCD panel in consideration of the above dispersion and the variation by the temperature.

When using the electronic volume control function, in order to compensate the V_5 voltage for dispersion of V_{REG} and I_{REF}, use a variable registor as Ra and perform optimum contrast adjustment according to the above item (4) with each IC chip.

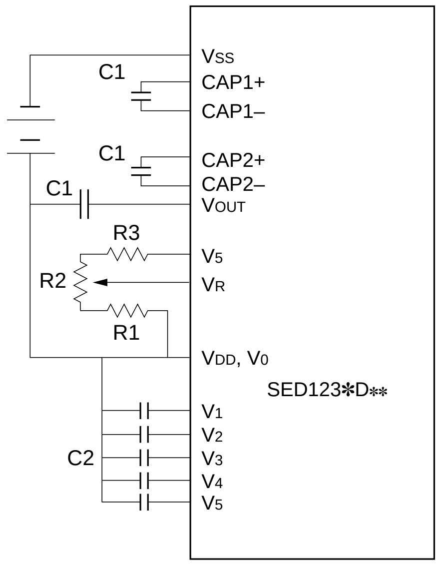
When the electronic volume control function is not being used, set the electronic volume control register to (0, 0, 0, 0) using the RES signal or the electronic volume control register setting command.

Liquid crystal voltage generating circuit

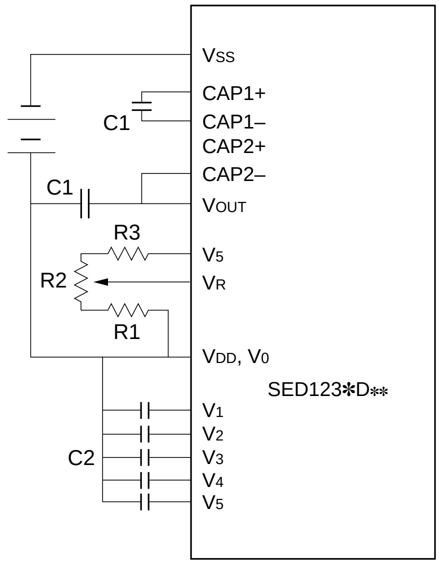
The V_5 potential is resistance-divided inside the IC so that V_1, V_2, V_3 and V_4 potentials are generated for liquid crystal drive.
Furthermore, the V_1, V_2, V_3 and V_4 are impedance-converted by voltage follower and the then supplied to the liquid crystal drive circuit.
The liquid crystal drive voltage is fixed to 1/5 bias.

As shown in the diagrams below, the capacitor (C2) for voltage stabilization must be externally connected to the V_1 to V_5 pins of liquid crystal power pins.

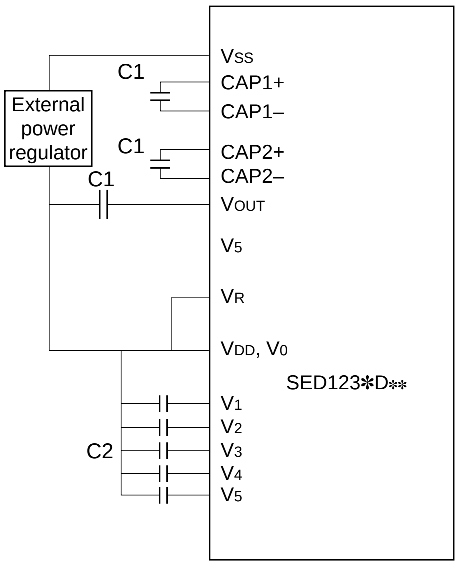
When a built-in power supply is used
Under a triple boosting



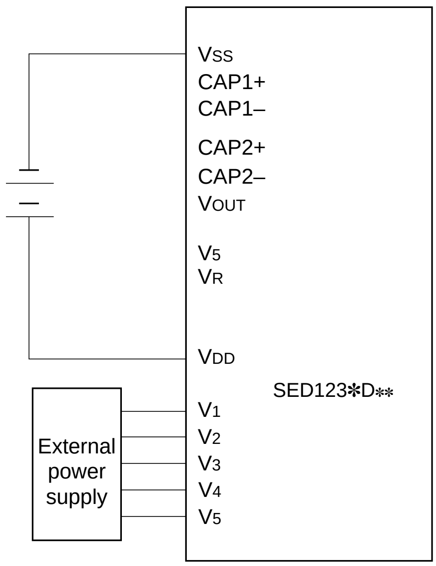
The diagram under a double boosting



When an external power regulator is used
(The built-in power regulator is not used)



When a built-in power supply is not used



Reference setting values: C1: 0.1 - 4.7 µF
C2: 0.1 µF

We recommend the user to set the optimum values to capacitors C1 and C2 according to the panel size watching the liquid crystal display and drive waveforms.

Low Power Consumption Mode

The SED1234, SED1235 Series is provided with the standby mode and sleep mode with the object of low power consumption when the unit is in the standby state.

● Sleep Mode

After the power circuit and oscillating circuit are turned off by command and the power save command is executed, the sleep mode is set. This mode permits reducing current consumption nearly to the static current value.

1. Liquid crystal display output
   COM1 ~ COM28, COMS2, COMS3 : V_{DD} level
   SEG1 ~ SEG60, SEGS2, SEGS6 : V_{DD} level
2. DD RAM, CG RAM and symbol register
   Written contents do not change and are stored regardless of whether the sleep mode is turned on or off.
3. In the operation mode, the status precedent to execution of the sleep mode is held. All the internal circuits stops.
4. Power circuit and oscillating circuit
   Turn off the built-in power supply and oscillating circuit by power save command and power control command.

Reset Circuit

When the RES input goes active, this LSI enters the initialization status.

1. Display ON/OFF control
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
   DC = 0 : Double cursor OFF
   D = 0 : Display OFF
2. Power save
   O = 0 : Oscillating circuit OFF
   PS = 0 : Power save OFF
3. Power control
   VC = 0 : Voltage regulating circuit OFF
   VF = 0 : Voltage follower OFF
   P = 0 : Boosting circuit OFF
4. System set
   CG = 0 : No use of CG RAM

As described in 6.1 MPU Interface, the RES pin is connected to the MPU reset pin and performs initialization concurrently with the MPU.
Regarding the reset signal, a pulse of at least 10 µs or more active level must be input as described in 9. DC Characteristics. Usually, the operation status is started in 1 µs from the edge of the RES signal.
In the SED 1230 Series where the built-in liquid crystal power circuit is not used, the RES input must be active when the external liquid crystal power supply is turned on.

COMMANDS

Table 4 shows a command list. In the SED1230 Series, each data bus signal is identified by a combination of A0 and $\overline{WR}$ (E).
Command interpretation and execution are performed by only internal timing. This permits high-speed processing.

- **Outline of Commands**

Command type	Command name	A0	WR
Display control instruction	Cursor Home	0	0
	Display ON/OFF Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
	Electronic Volume Register Set	0	0
Address control instruction	Address Set	0	0
Data input instruction	Data Write	1	0

The execution time of each instruction is determined by the internal processing time of the SED1230 Series. Accordingly, to execute instructions in succession, reserve a time exceeding the cycle time (tcyc) and execute the next instruction.

- **Outline of Commands**

(1) Cursor Home
This command presets the address counter to 30H. When the cursor is displayed, this command moves it to column 1 of line 1.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	*	*	*	*

* : Don't Care

(2) Display ON/OFF Control
This command performs display and cursor setting.

Note: Control the symbols that are driven by COMS1 and SEGS1, by the Static Display Control command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	C	B	DC	D

D = 0 : Display OFF
1 : Display ON

DC = 0 : Double cursor OFF
1 : Double cursor ON

B = 0 : Cursor blink OFF
1 : Cursor blink ON

In the blink state, display characters in normal video and display characters in monochrome reverse video are displayed alternately.
The repetition cycle of alternate display is about 1 second.

C = 0 : Non-display of cursor
1 : Display of cursor

The relationship between C and B registers and cursor display is shown in the following table.

C	B	Cursor display
0	0	Non-display
0	1	Non-display
1	0	Display in monochrome reverse video
1	1	Alternate display of display charac ters in normal video and display characters in monochrome reverse video

The cursor display position corresponds to the position indicated by address counter.

Accordingly, to move the cursor, change the address counter value by the RAM Address Set command or auto increment by writing RAM data.

If the address counter is set at the symbol register position with (C, B) = (1, 0), symbols can be caused to blink selectively.

(3) Power Save
This command is used to control the oscillating circuit and set and reset sleep mode.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	*	*	O	PS

* : Don't Care

PS = 0 : Power save OFF (reset)
1 : Power save ON (set)

O = 0 : Oscillating circuit OFF (stop of oscillation)
1 : Oscillating circuit ON (oscilla tion)

(4) Power Control

This command is used to control the operation of the built-in power circuit.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	VC	VF	P

P = 0 : Boosting circuit OFF
1 : Boosting circuit ON

Note: To operate the boosting circuit the oscillating circuit must be in operation.

VF = 0 : Voltage follower OFF
1 : Voltage follower ON

VC = 0 : Voltage regulating circuit OFF
1 : Voltage regulating circuit ON

(5) System Set

This command set the use or non-use of display lines and CG RAM.

Execute this command first after turning on the power supply or after resetting.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	N2	N1	*	PS

* : Don't Care

CG = 0 : Use of CG RAM
1 : Non-use of CG RAM

N2	N1	
0	0	: 2 lines
0	1	: 3 lines
1	0	: 4 lines

(6) Electronic Volume Register Set

This command controls the liquid crystal driving voltage V_5 output from the voltage regulating circuit of the built-in liquid crystal power supply, thereby adjusting the gradation of liquid crystal display.

When data is set in the 4-bit register, the liquid crystal driving voltage can take one of 16 voltage states.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	MSB	*	*	LSB

Hex Code
70H ~7FH

MSB	.	.	LSB	$\lvert V_5 \rvert$	$\lvert I_{REF} \rvert$
0	0	0	0	Small	0.0μA
			:	:	:
		.	:	:	:
1	1	1	1	Large	3.65μA

When the electronic volume function is not used, set (A3, A2, A1, A0) = (0, 0, 0, 0).

(7) RAM Address Set

This command sets addresses to write data into the DD RAM, CG RAM and symbol register in the address counter.

When the cursor is displayed, the cursor is displayed at the display position corresponding to the DDRAM address set by this command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ADDRESS						

① The settable address length is ADDRESS = 00H to 7FH.

② Before writing data into the RAM, set the data write address by this command. Next, when data is written in succession, the address is automatically incremented.

RAM Map

<table>
<tr><th></th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>F</th></tr>
<tr><td>00H</td><td colspan="7">CGRAM(00H)</td><td>–</td><td colspan="7">CGRAM(01H)</td><td>–</td></tr>
<tr><td>10H</td><td colspan="7">CGRAM(02H)</td><td>–</td><td colspan="7">CGRAM(03H)</td><td>–</td></tr>
<tr><td>20H</td><td colspan="16">Unused</td></tr>
<tr><td>30H</td><td colspan="13">DDRAM line 1</td><td colspan="3">Unused</td></tr>
<tr><td>40H</td><td colspan="13">DDRAM line 2   For signals</td><td colspan="3">"</td></tr>
<tr><td>50H</td><td colspan="13">DDRAM line 3</td><td colspan="3">"</td></tr>
<tr><td>60H</td><td colspan="13">DDRAM line 4</td><td colspan="3">"</td></tr>
<tr><td>70H</td><td colspan="13">Symbol register</td><td colspan="3">"</td></tr>
</table>

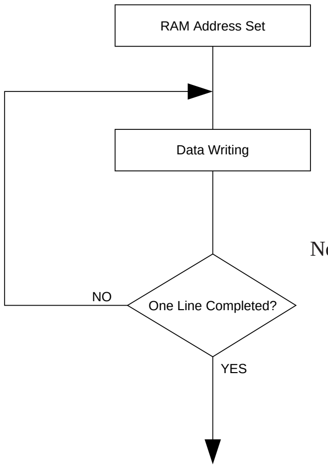
– : Unused
For signals : Output from SEGS2 to SEGS6.

(8) Data Write

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DATA							

① This command writes data into the DD RAM, CG RAM or symbol register.
② After this command is executed, the address counter is automatically incremented by 1. This permits writing data in succession.

<Example of Data Writing>
The following is an example of writing one-line data into the DD RAM in succession.



Note: When executing instructions in succession, reserve a time exceeding t_{CYC} and execute the next instruction.

Table 4 SED1234/SED1235 Command List

Command	Code										Function
	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position.
(2) Display ON/OFF Control	0	0	0	0	1	1	C	B	DC	D	Sets cursor ON/OFF (C), cursor blink ON//OFF (B), double cursor ON/OFF (DC) and display ON/OFF (D). C = 1 (cursor ON) 0 (cursor OFF), B = 1 (blink ON) 0 (blink OFF) DC = 1 (double cursor ON) 0 (double cursor OFF), D = 1 (display ON) D = 0 (display OFF)
(3) Power Save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (0). PS = 1 (power save ON) 0 (power save OFF), 0 = 1 (oscillating circuit ON) 0 (oscillating circuit OFF)
(4) Power Control	0	0	0	1	0	1	0	VC	VF	P	Sets voltage regulating circuit ON/OFF and boosting circuit ON/OFF (P). VC = 1 (voltage regulating circuit ON) 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) 0 (voltage follower OFF), P = 1 (boosting circuit ON) 0 (boosting circuit OFF)
(5) System Set	0	0	0	1	1	0	N2	N1	*	CG	Sets the use or non-use of CG RAM and display lines (N2, N1). CG = 1 (use of CG RAM) 0 (non-use of CG RAM), N2, N1 = 0, 0 (2 lines) 0, 1 (3 lines) 1, 0 (4 lines)
(6) Electronic Volume Register	0	0	0	1	1	1	MSB			LSB	Sets the electronic volume register value.
(7) RAM Address Set	0	0	1	ADDRESS							Sets the DD RAM, CG RAM or symbol register address.
(8) RAM Write	1	0	DATA								Writes data into the DD RAM, CG RAM or symbol register address.
(9) NOP	0	0	0	0	0	0	0	0	0	0	Non-operation command
(10) Test Mode	0	0	0	0	0	0	1	0	1	0	Command for IC chip test. Don’t use this command.

CHARACTER GENERATOR

Character Generator ROM (CG ROM)

The SED1234/1235 is provided with a character generator ROM consisting of a up to 256-type characters. Each character size is 5 × 7 dots.

Table 5 shows a character code table of the SED1230 Series.
The 4characters of character codes 00H to 03H are set by the System Set command to specify for which of CG ROM and CG RAM they are to be used.

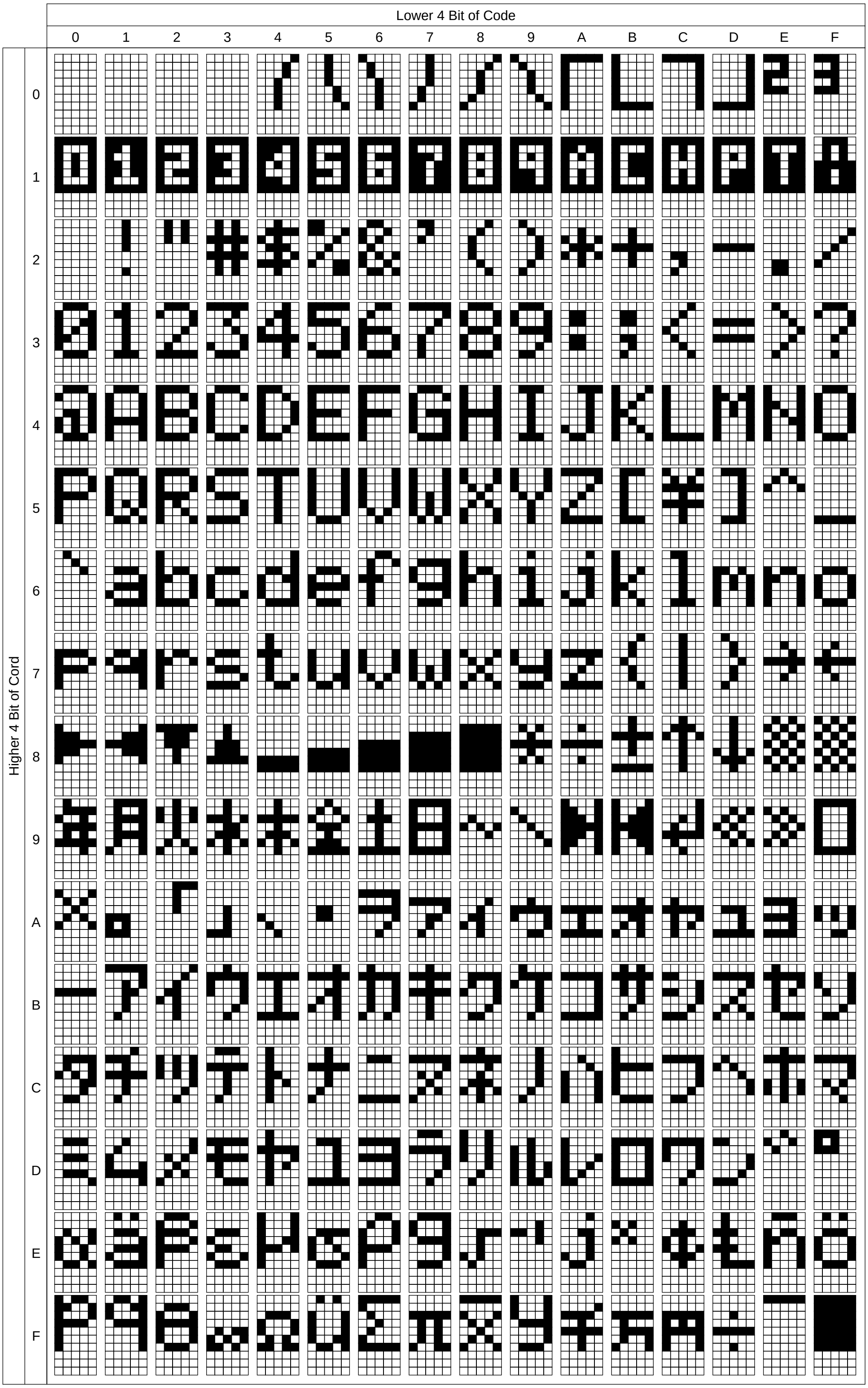
The CG ROM of the SED1234/1235 is a mask ROM and compatible with the use-dedicated CG ROM. Please ask us for further information of it.

Regarding changed CG ROM, it is defined in product name as follows:

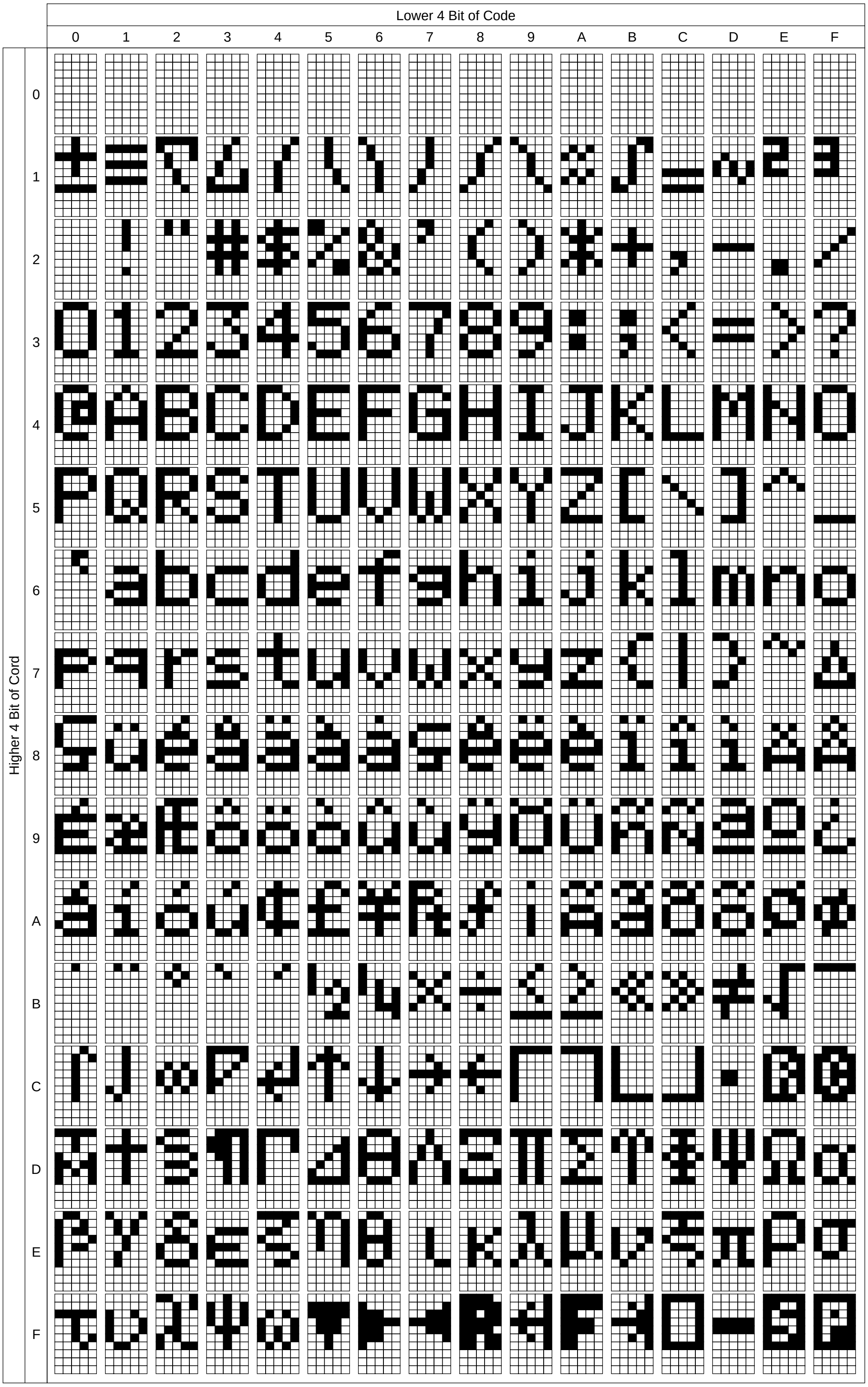
(Example) S E D 1 2 3 4 D 0 A
↑
Digit for CG ROM pattern change

SED123✱DA✱

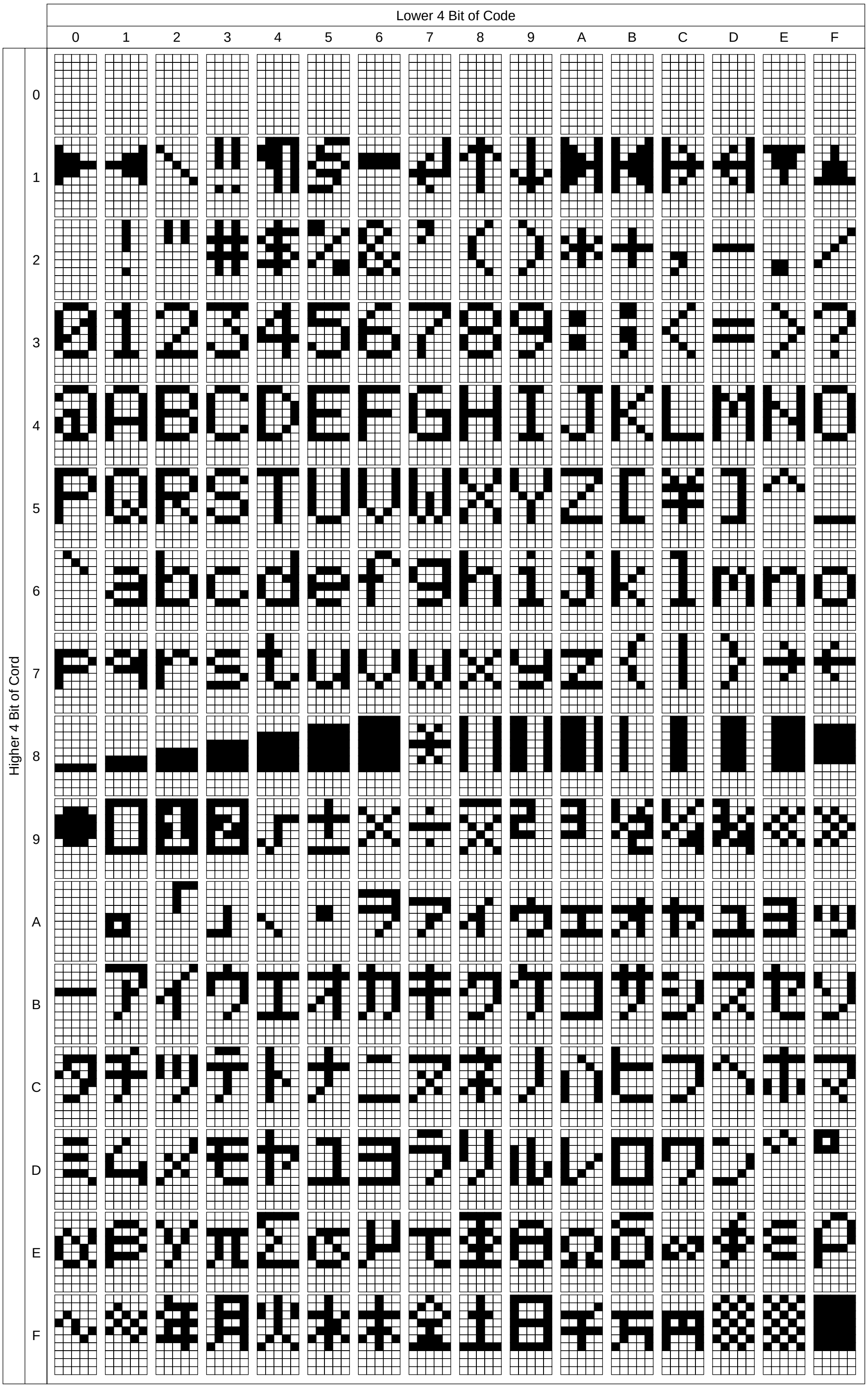
Table 5



SED123*DB*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

SED123*DG*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

Character Generator RAM (CG RAM)

The SED1230 Series is provided with a CG RAM that permits user-programming character patterns so that they can be displayed with a high degree of freedom for signal display.

Before using the CG RAM, select the use of CG RAM by the System Set command.

The capacity of the CG RAM is 140 bits and arbitrary patterns of 4 types consisting of 5 × 7 dots can be registered.

The relationship among CG RAM patterns, CG RAM addresses, and character codes is shown below.

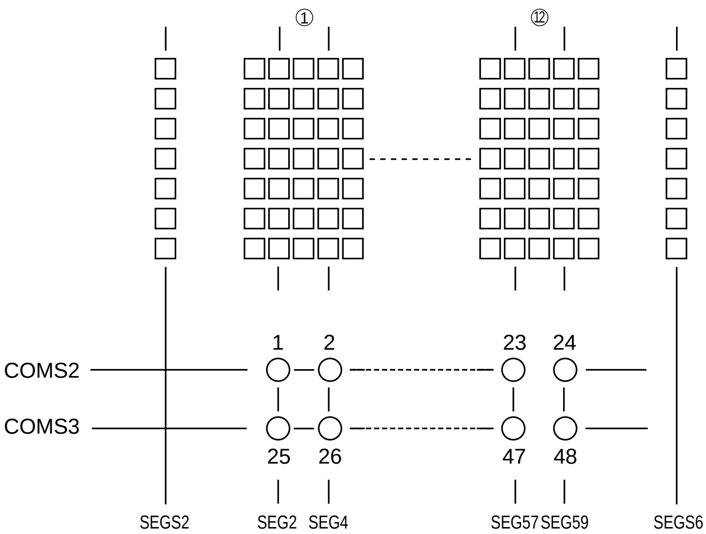
Character code	RAM address		CGRAM data (character pattern)								Display
			D7							D0	
00H 02H	00H~06H 10H~16H	0	*	*	*	0	1	1	1	1	□■■■■
		1	*	*	*	1	0	0	0	0	■□□□□
		2	*	*	*	1	0	0	0	0	■□□□□
		3	*	*	*	0	1	1	1	1	□■■■■
		4	*	*	*	0	0	0	0	1	□□□□■
		5	*	*	*	0	0	0	0	1	□□□□■
		6	*	*	*	1	1	1	1	0	■■■■□
01H 03H	08H~0EH 18H~1EH	8	*	*	*	0	0	1	0	0	□□■□□
		9	*	*	*	0	0	1	0	0	□□■□□
		A	*	*	*	0	1	1	1	0	□■■■□
		B	*	*	*	0	1	1	1	0	□■■■□
		C	*	*	*	0	1	1	1	0	□■■■□
		D	*	*	*	1	1	1	1	1	■■■■■
		E	*	*	*	1	1	1	1	1	■■■■■

Unused (D7–D5)

Character data (D4–D0)
1: Display
0: Non-display

Symbol Register

The SED1234, 1235 provided with a symbol register that permits displaying each symbol so that symbol display may be performed on the screen.
The capacity of the symbol register is 48 bits. In case of 48 symbols can be displayed.
The relationship among symbol register display patterns, RAM addresses and write data is shown below.



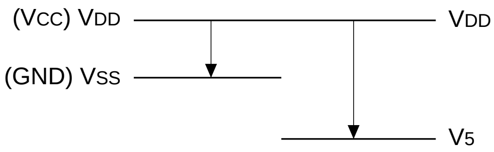
RAM address		Symbol Bits							
		D7							D0
70H~7BH	0	*	*	*	25	1	26	2	*
	1	*	*	*	27	3	28	4	*
	:	:							
	B	*	*	*	47	23	48	24	*

Bit
1: Display
0: Not display

Notes: 1. We recommend to drive a symbol by dividing it into COMS2 and COMS3 separately if it is larger than other dots for 1.5 times or more.
2. Do not cross a segment (other than those used for symbol display) with COMS2 or COMS3. If segment crossing is required, set the symbol registers of COMS3 to all zeros (0s).

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	–6.0~+0.3	V
Power supply voltage (2)		V_5	–16.0~+0.3	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	V_5~+0.3	V
Input voltage		V_{IN}	V_{SS}–0.3~+0.3	V
Output voltage		V_O	V_{SS}–0.3~+0.3	V
Operating temperature		T_{opr}	–30~+85	°C
Storage temperature	TCP	T_{str}	–55~+100	°C
	Bare chip		–65~+125	



Notes: 1. All the voltage values are based on V_{DD} = 0 V.
2. For voltages of V_1, V_2, V_3 and V4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction.
In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

DC CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.

Item		Symbol	Condition		min	typ	max	Unit	Applicable pin
Power supply voltage (1)	Recommended operation	V_{SS}			–3.6	–3.0	–2.4	V	V_{SS}
	Operable				–5.5	–3.0	–2.4		*1
Power supply voltage (2)	Recommended operation	V_5			–8.0		–5.0	V	V_5
	Operable				–11.0		–4.5		*2
	Operable	V_1, V_2			0.6×V_5		V_{DD}	V	V_1, V_2
	Operable	V_3, V_4			V_{DD}		0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHC}			0.2×V_{SS}		V_{DD}	V	*3
Low-level input voltage		V_{ILC}			V_{SS}		0.8×V_{SS}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS} –1.0			1.0	µA	*3	
LC driver ON resistance		R_{ON}	Ta=25°C ΔV=0.1V	V_5=–7.0V		20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}				0.1	5.0	µA	V_{DD}
Dynamic current consumption		I_{DD}	Display state	V_5 = –7 V without load			100	µA	V_{DD} *5
			Standby state	Oscillation ON, Power OFF			20	µA	V_{DD} *6
			Sleep state	Oscillation OFF, Power OFF			5	µA	V_{DD}
			Access state	f_{cyc}=200KHz			500	µA	V_{DD} *7
Frame frequency		f_{FR}	Ta=25°C V_{SS}=–3.0V		70	100	130	Hz	*11
Input pin capacity		C_{IN}	Ta=25°C f=1MHz			5.0	8.0	pF	*3

	Symbol	Condition	min	typ	max	Unit	Applicable pin
Reset time	t_R		1.0			µs	*8
Reset pulse width	t_{RW}		10			µs	*9
Reset start time	t_{RES}		50			ns	*9

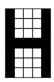
Built-in power supply	Input voltage	V_{SS}		–3.6		–2.4	V	*10
	Booster output voltage	V_{OUT}	Double boosting state	–7.2			V	V_{OUT}
			Triple boosting state	–10.8				
	Voltage follower operating voltage	V_5		–11.0		–4.5	V	
	Reference voltage (standard)	V_{REG}	Ta = 25°C	–3.5	–3.1	–2.7	V	*12
	Reference voltage (option)	$V_{REG(VS1)}$	Ta = 25°C	–2.4	–2.1	–1.8	V	*12

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

*2: The operating voltage range is applicable to the case where an external power supply is used.

*3: D0 ~ D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).
R_{ON} = 0.1 V / ΔI
(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Character "  " display. This is applicable to the case where no access is made from the MPU and the built-in power circuit and oscillating circuit are in operation.

*6: This is applicable to the case where the built-in power circuit is OFF and the oscillating circuit is in operation in the standby mode.

*7: Current consumption when data is always written by f_{cyc}.
The current consumption in the access state is almost proportional to the access frequency (f_{cyc}).
When no access is made, only I_{DD} (I) occurs.

*8: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the SED123✻ usually enters the operating state after t_R.

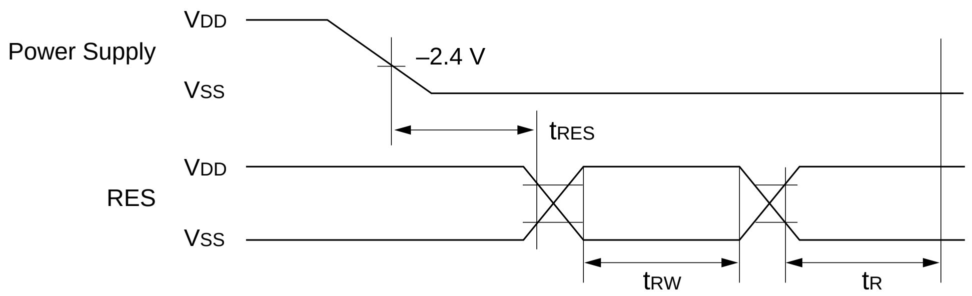
*9: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.

*10: When operating the boosting circuit, the power supply V_{SS} must be used within the input voltage range.

*11: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}
Example: The SED1230 has 13 digits of display and 1/30 duty.
f_{OSC} = 13 × 30 × 100 = 39 kHz
f_{BST} = (1/2) × (1/13) × 39 K = 1.5 kHz

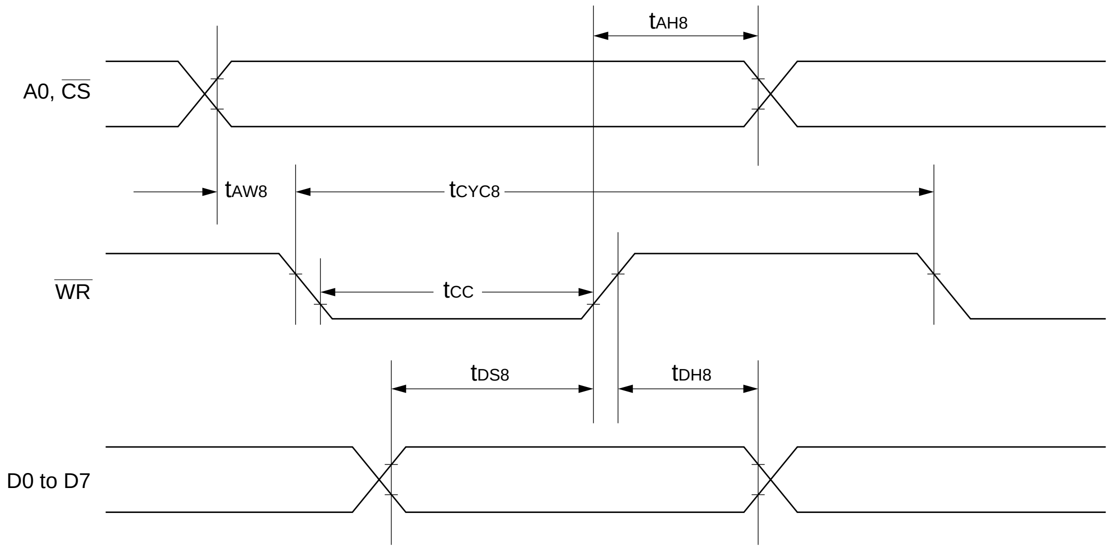
*12: The V_{REG} reference voltage has the temperature characteristics of approximately –0.17%/°C (standard specifications). An optional model having the temperature characteristics of approximately –0.04%/°C is also available. The CGROM modification rules apply to the optional models.



All signal timings are based on 20% and 80% of V_{SS} signals.

TIMING CHARACTERISTICS

(1) System Bus Write Characteristic I (80 series MPU)

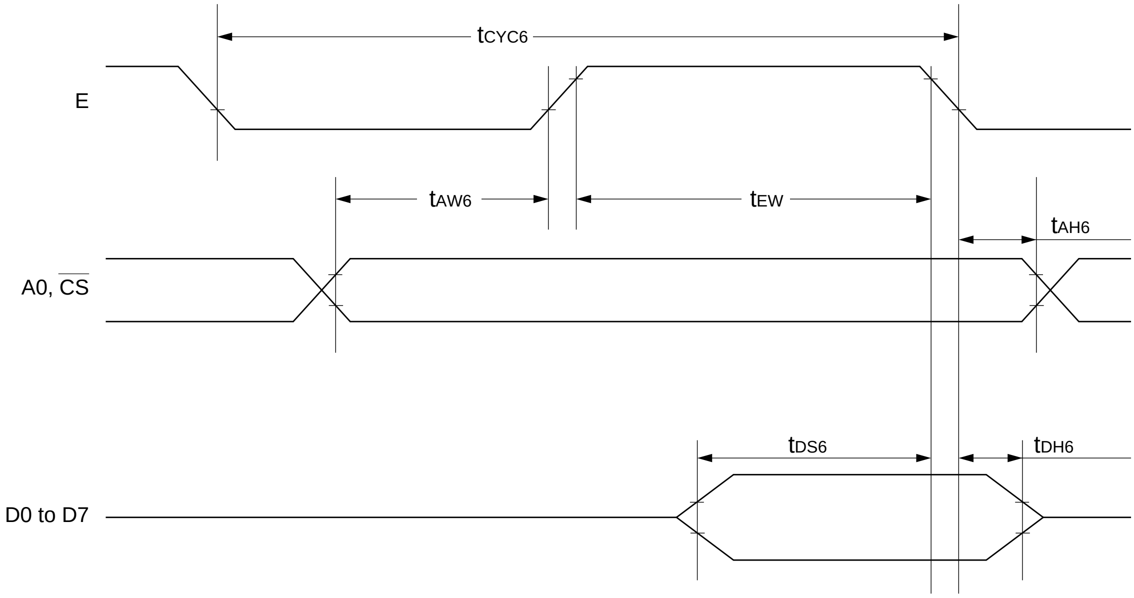


[V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		30		ns
Address setup time		t_{AW8}		60		ns
System cycle time	$\overline{WR}$	t_{CYC8}	V_{SS} = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Control pulse width ($\overline{WR}$)		t_{CC}	V_{SS} = –3.0	100		ns
			–2.7	120		
			–2.4	150		
Data setup time	D0 ~ D7	t_{DS8}		100		ns
Data hold time		t_{DH8}		50		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of V_{SS}.
*3: For A0 and $\overline{CS}$, the same time is not required. Input signals so that A0 and $\overline{CS}$ may satisfy t_{AW8} and t_{AH8} respectively.

(2) System Bus Write Characteristic II (68 series MPU)



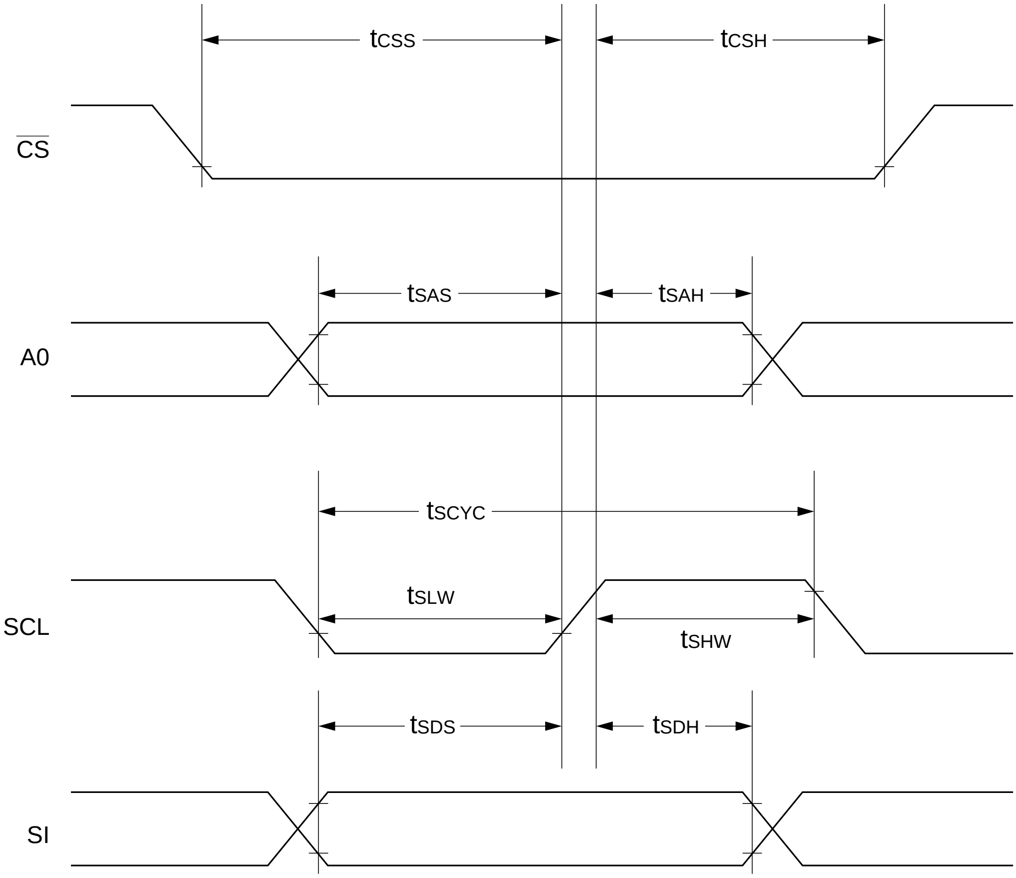
[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	t CYC6	VSS = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Address setup time		t AW6		60		
Address hold time		t AH6		30		ns
Data setup time	D0 ~ D7	t DS6		100		ns
Data hold time		t DH6		50		ns
Enable pulse width	E	t EW	VSS = –3.0	100		ns
			–2.7	120		
			–2.4	150		

*1: tCYC6 denotes the cycle of the E signal in the $\overline{CS}$ active state. tCYC6 must be reserved after $\overline{CS}$ becomes active.
*2: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*3: Every timing is specified on the basis of 20% and 80% of VSS.
*4: For A0 and $\overline{CS}$, the same timing is not required. Input signals so that A0 and $\overline{CS}$ may satisfy tAW6 and tAH6 respectively.

SED1234/35 Series

(3) Serial Interface



[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C]

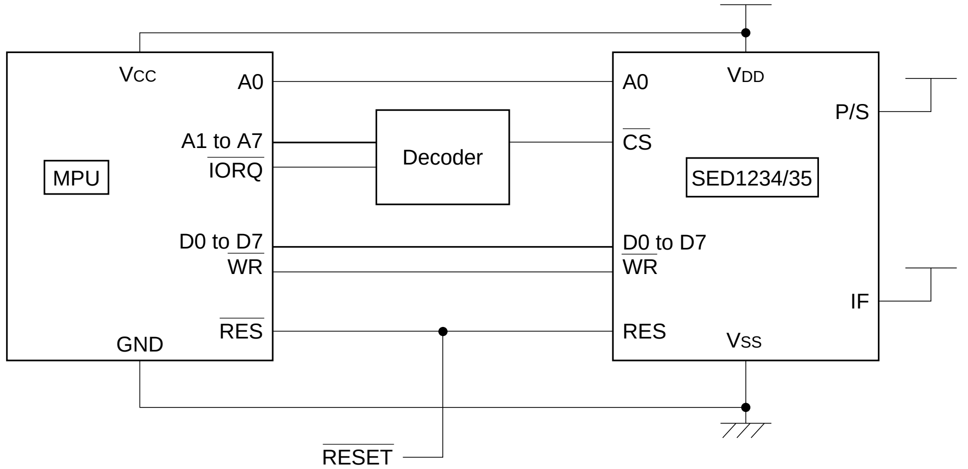
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	VSS = –3.0	700		ns
			–2.7	800		ns
			–2.4	1000		ns
SCL “H” pulse width		tSHW		300		ns
SCL “L” pulse width		tSLW		300		ns
Address setup time	A0	tSAS		50		ns
Address hold time		tSAH	VSS = –3.0	350		ns
			–2.7	400		ns
			–2.4	500		ns
Data setup time	SI	tSDS		50		ns
Data hold time		tSDH		50		ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS		150		ns
		tCSH	VSS = –3.0	550		ns
			–2.7	650		ns
			–2.4	700		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of VSS.

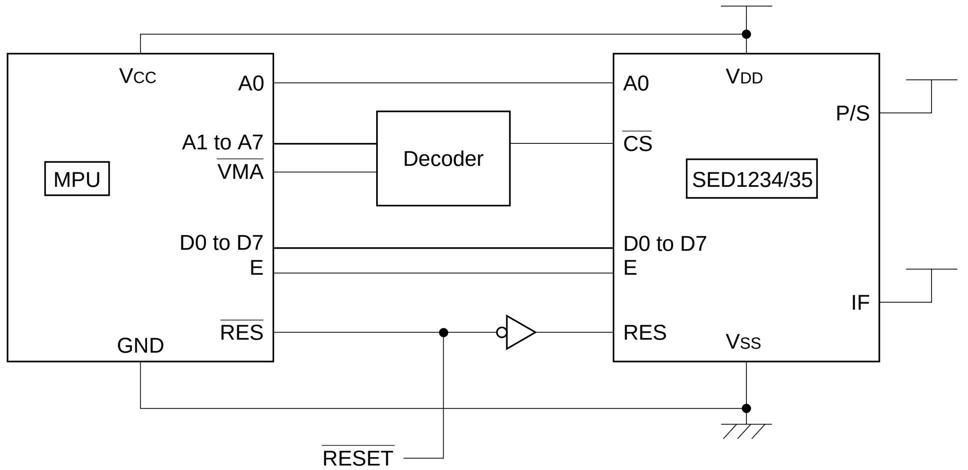
MPU INTERFACE (REFERENCE EXAMPLES)

The SED1234, 1235 can be connected to the 80 series MPU and 68 series MPU. When an serial interface is used, the SED1234, 1235 Series can be operated by less signal lines.

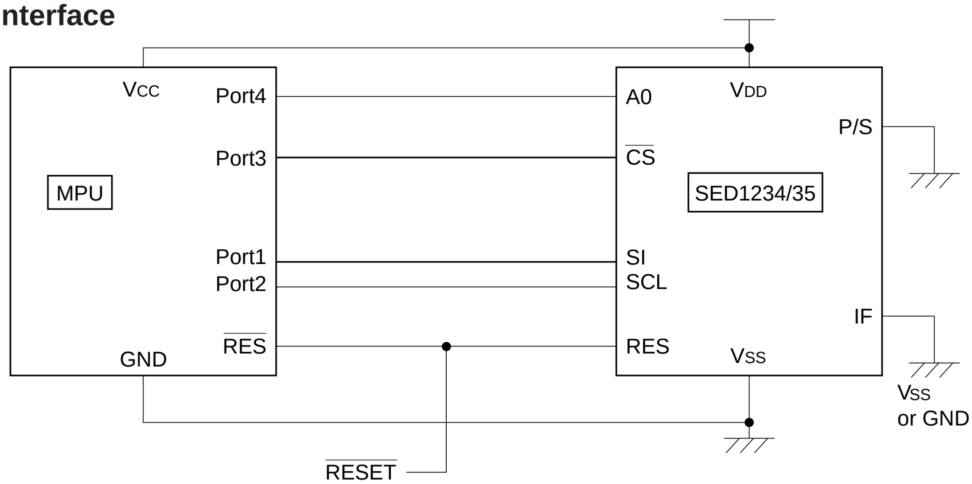
80 Series MPU



68 Series MPU

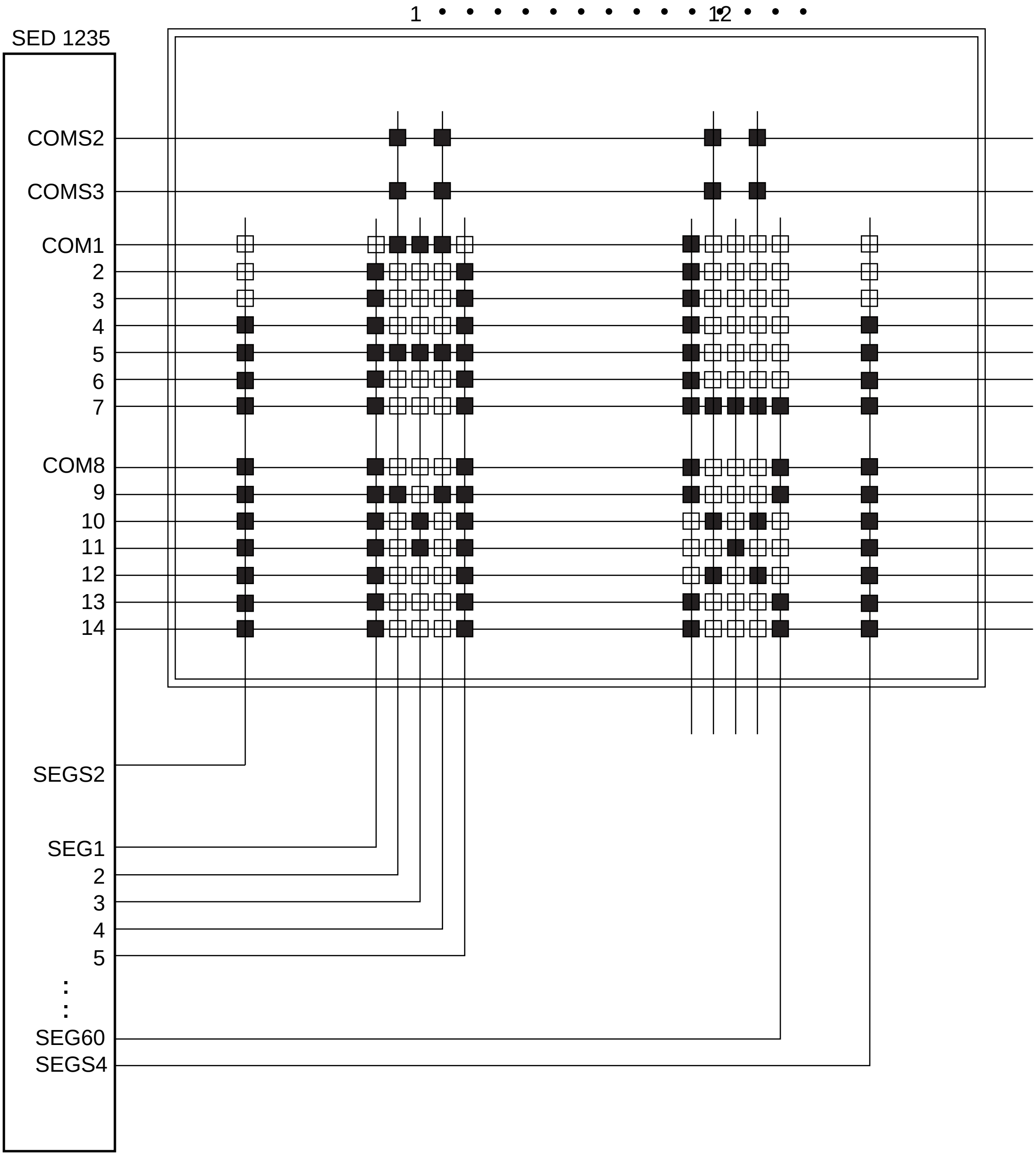


Serial Interface



INTERFACE TO LCD CELLS (REFERENCE)

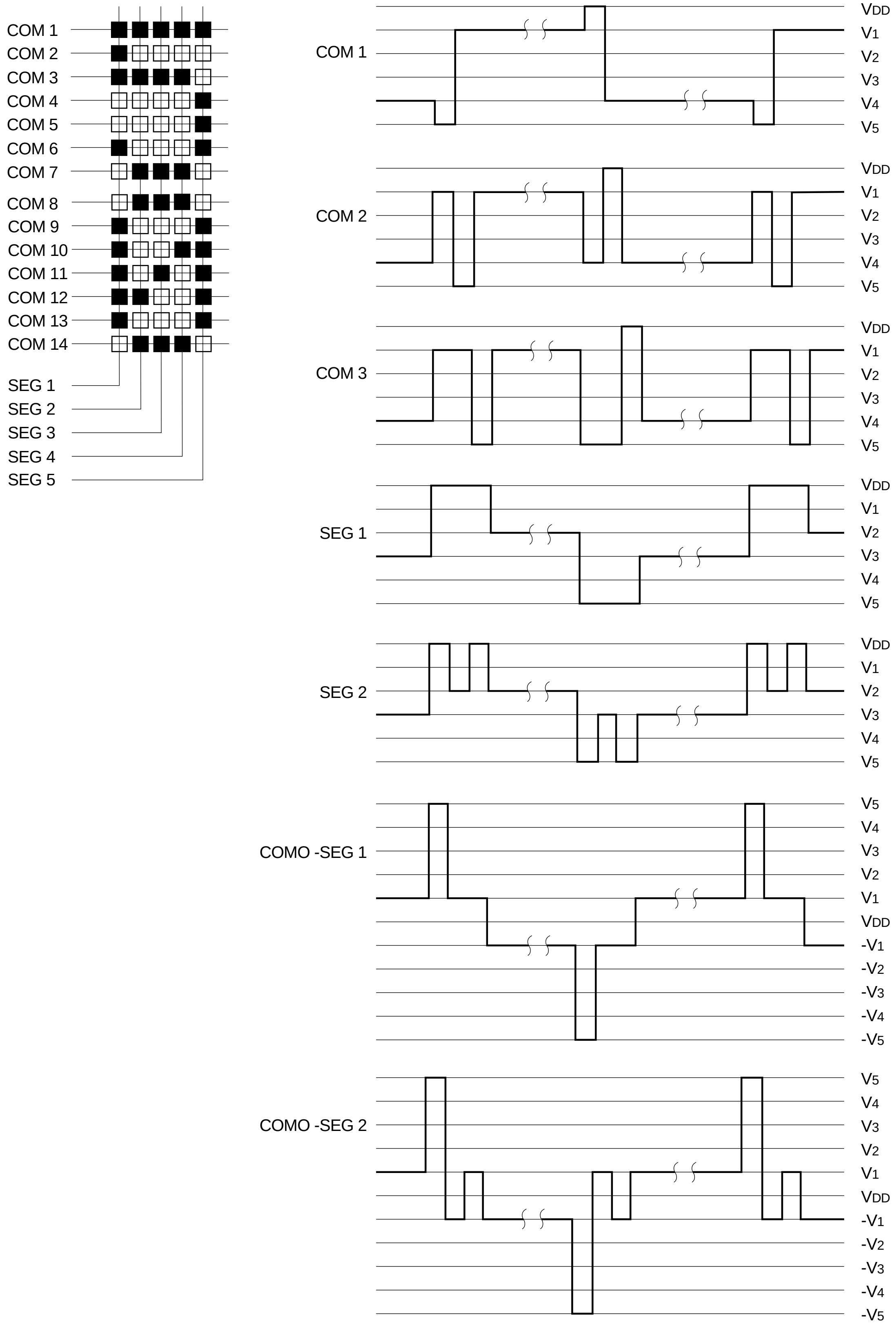
12 columns by 2 lines, 5×7-dot matrix segments and symbols



■ System Setup

N2	N1
0	0

LIQUID CRYSTAL DRIVE WAVEFORMS (B WAVEFORMS)



Instruction Setup Example (Reference Only)

(1) Initial setup

V_{DD}-V_{SS} power ON

Power regulation

Input of reset signal

Command status
- Static display control : Off
- Display on/off control : Off
- Power save : Off
- Power control : Off
- System reset : CG=0
- Others are undefined.

Waiting for 10 µsec or more

Command input: (Asterisk indicates any command sequence.)
(1) System setup command
(*) Static display control command
(Valid in Standby mode only)
(*) Display on/off control command
• D: On (Display)
(*) Electronic volume register setup
• Data: (0, 0, 0, 0)
(*) Power save command
• PS: Off (Power save)
• O: On (Oscillation)
(6) RAM address setup (Note 1)
(7) Data writing (Note 1)

Waiting for 20 msec or more

Command input
(8) Power control commands
• P, VF, VC: On

Command input:
(9) Electronic volume register setup
• Data: Appropriate value

End of initialization

(2) Display mode

End of initialization

Input of RAM address setup command

Input of RAM (data) write command

Display of written data

Note 1: Commands (6) and (7) initialize the RAM. The display contents must first be set. The non-display area must satisfy the following conditions (for RAM clear).
- DDRAM: Write the 20H data (character code).
- CGRAM: Write the 00H data (null data).
- Symbol register: Write the 00H data (null data).

As the RAM data is unstable during reset signal input (after power-on), null data must be written. If not, unexpected display may result.

(3-1) Selecting the Standby mode

- End of initialization
- Normal operation (Power Save is released and oscillator circuit is turned ON.)
- Command input:
  - (1) Display on/off control command (Note 2)
    - • D: Off (Display)
  - (2) Power save command (Note 2)
    - • PS: On (Power save)
    - • O: On (Oscillation)
  - (3) Power control commands
    - • P, VF, VC: Off
- Standby status
- Static display control commands can be used.

(3-2) Releasing the Standby mode

- Standby mode
- Command input:
  - (1) Display on/off control command (Note 2)
    - • D: On (Display)
  - (2) Power save command (Note 2)
    - • PS: Off (Power save)
    - • O: On (Oscillation)
- Input of electronic volume register command
  - • Data: (0, 0, 0, 0)
- Input of power control commands
  - • P, VF, VC: Off
- Input of electronic volume register command
  - • Data: Appropriate value
- Return to normal operation (initial status).

Note 2: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

(4-1) Selecting the Sleep mode

- End of initialization
- Normal operation (Power Save is released and oscillator circuit is turned ON.)
- Command input:
  - (1) Display on/off control command (Note 3)
    - • D: Off (Display)
  - (2) Power save command (Note 3)
    - • PS: On (Power save)
    - • O: Off (Oscillation)
  - (3) Power control commands
    - • P, VF, VC: Off
- Enter the Sleep mode.

(4-2) Releasing the Sleep mode

- Sleep mode
- Command input:
  - (1) Display on/off control command (Note 3)
    - • D: On (Display)
  - (2) Power save command (Note 3)
    - • PS: Off (Power save)
    - • O: On (Oscillation)
- Wait for 20 msec or more.
- Input of electronic volume register command
  - • Data: (0, 0, 0, 0)
- Input of power control commands
  - • P, VF, VC: On
- Input of electronic volume register command
  - • Data: Appropriate value
- Return to normal operation (initial status).

Note 3: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

SED1240 Series
LCD Controller/Drivers

Technical Manual

Contents

OVERVIEW

The SED1240 Series is a character display dot matrix LCD controller driver. This driver can display up to 64 characters and 6 user-defined characters, and up to 160 symbols according to the 4-bit, 8-bit or serial data which is sent from a microcomputer.

The built-in character generator ROM is provided with up to 544 types of character fonts having a structure of 5 × 8 dots. Up to 256 types can be continuously called by register option selection. This can cope with many different character fonts by uses and countries and permits a wider range of use. This driver incorporates a user-defined character RAM for 6 characters of 5 × 8 dots and can be used for the display of higher degree of freedom by means of a symbol register.

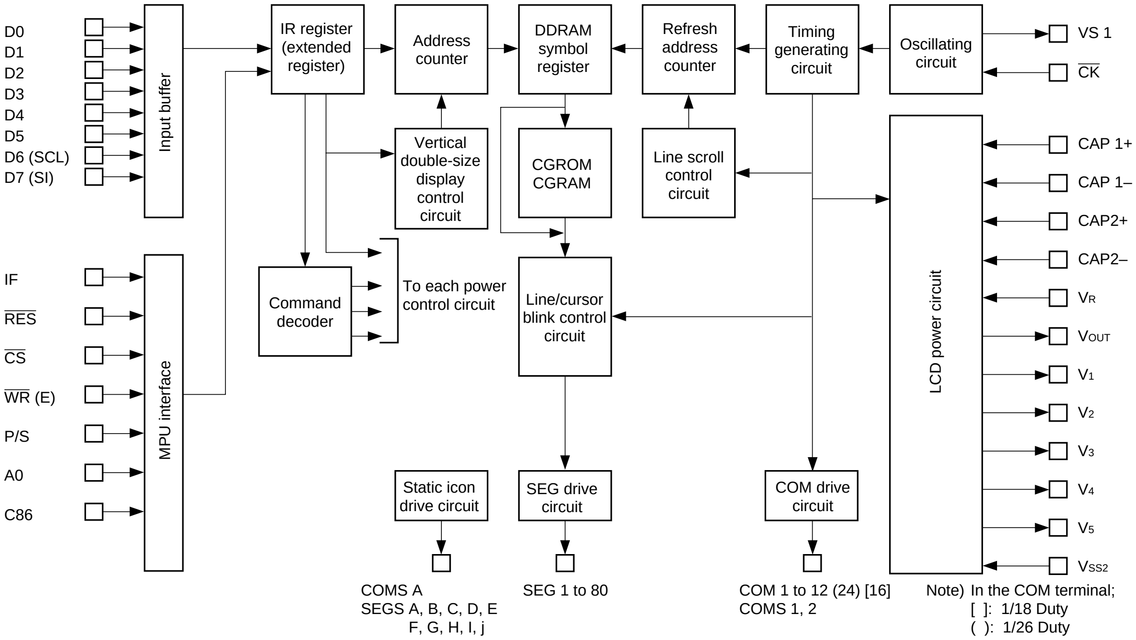
The driver can operate handy units at the minimum power consumption by using its merit of lower power consumption, standby mode, and sleep mode.

FEATURES

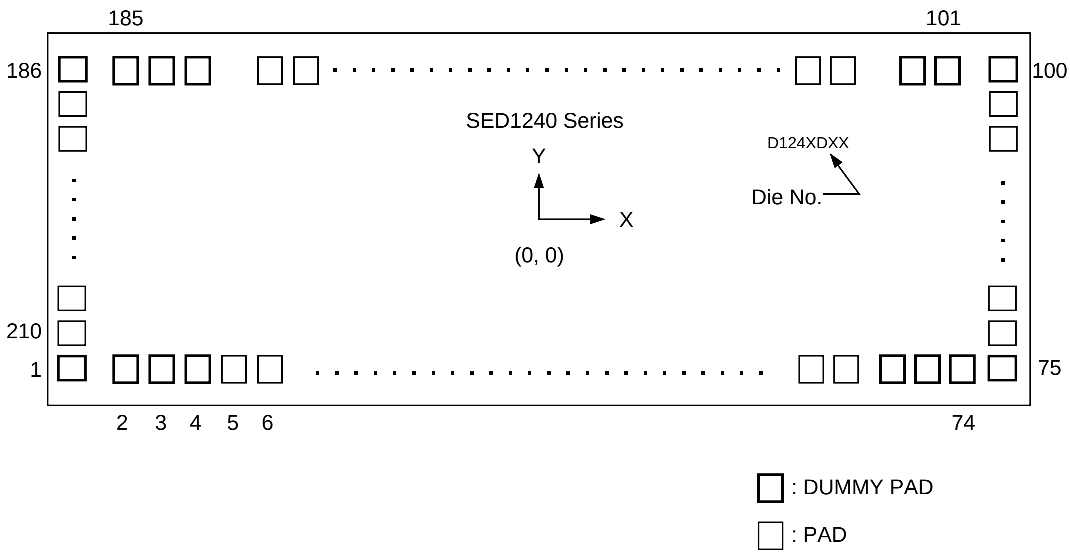
- Built-in display data RAM 80-character + 6-character user-defined characters + 160 symbols
- CGROM (for up to 544 characters), CGRAM (6 characters), symbol register (160 symbols)
- Display digits × Number of lines
  <Ordinary mode>
  ① (16 digits) × 4 lines + 160 symbols + 10 static irons (SED1240)
  ② (16 digits) × 3 lines + 160 symbols + 10 static icons (SED1241)
  ③ (16 digits) × 2 lines + 160 symbols + 10 static icons (SED1242)
  <Standby mode>
  ① 10 static icons (SED1240)
  ② 10 static icons (SED1241)
  ③ 10 static icons (SED1242)
- Vertical double-size display function
- Line vertical scroll function
- Line blink function
- Symbol blink function
- Built-in CR oscillating circuit (Built-in C, R)
- External clock input
- High-speed MPU interface
  Interface with both MPUs of 68 series/80 series
  Interface by 4 bits/8 bits
- Serial interface
- Character font 5 × 8 dots
- Duty ratio ① 1/34 (SED1240)
  ② 1/26 (SED1241)
  ③ 1/18 (SED1242)
- Simple command setup
- Built-in liquid crystal drive power circuit
  The boosting circuit, voltage regulating circuit, voltage follower × 4, and resistor for power regulating circuit for bias select commands are incorporated.
- Built-in electronic volume function
- Lower power consumption
  - 80 µA max (at ordinary operation (during display): Including the internal power supply operating current)
  - 500 µA max (at ordinary operation (during access): fcyc = 200 KHz, including the internal power supply operating current)
  - 20 µA max (in standby mode: Oscillation ON, power OFF, static icon display)
  - 5 µA max (in sleep mode: oscillation OFF, power OFF, display OFF)
- Power supply:
  - V_{DD} - V_{SS} 1.8 V to 5.5 V
  - V_{DD} - V_{SS2} 1.8 V to 5.5 V
  - V_{DD} - V_5 5.5 V to 16.0 V
- Wide operating temperature range
  Ta = –30 to +85°C
- CMOS process
- Pad pitch 90 µm Min
- Delivery form
  - Chip (gold bump product) SED124∗D∗∗
  - TCP SED124∗T∗∗
- This IC is not designed against radiation and strong light and noise.

SED1240 Series

BLOCK DIAGRAM



CHIP SPECIFICATIONS



SED124∗∗∗∗

- Digits for CGROM pattern change
- Number of display lines
  - 0: 4-line display
  - 1: 3-line display
  - 2: 2-line display

Chip size:	8.70 × 2.80 mm
Pad pitch:	90 µm (Min.)
Chip thickness (reference value):	625 ± 50 µm (SED124∗D∗∗)

Au bump specifications

Bump size	A TYPE	60.0 µm × 81.5 µm
	B TYPE	81.5 µm × 60.0 µm
	C TYPE	85.0 µm × 85.0 µm
	D TYPE	60.0 µm × 85.0 µm
Bump height (reference value)		22.5 µm ± 5.5 µm

(For bump types, refer to the pad coordinate diagram.)

Note: The board of this IC has VDD potential. It is recommended to stabilize power supply by connecting the board to the VDD potential at the time of mounting.

<Pad Coordinates> SED1240$_{***}$

PAD			COORDINATES	
No.	Name	[BUMP TYPE]	X	Y
1	NC	[B TYPE]	–4191	–1250
2	NC	[C TYPE]	–3941	–1237
3	NC	[C TYPE]	–3836	↓
4	NC	[C TYPE]	–3555	
5	A0	[C TYPE]	–3403	
6	$\overline{WR}$	[C TYPE]	–3283	
7	$\overline{CS}$	[C TYPE]	–3163	
8	D7	[C TYPE]	–3043	
9	D6	[C TYPE]	–2922	
10	D5	[C TYPE]	–2802	
11	D4	[C TYPE]	–2682	
12	D3	[C TYPE]	–2562	
13	D2	[C TYPE]	–2441	
14	D1	[C TYPE]	–2321	
15	D0	[C TYPE]	–2201	
16	V_{DD}	[D TYPE]	–2089	
17	V_{DD}	[D TYPE]	–1999	
18	V_{DD}	[D TYPE]	–1909	
19	V_{SS}	[D TYPE]	–1820	
20	V_{SS}	[D TYPE]	–1730	
21	V_5	[D TYPE]	–1641	
22	V_5	[D TYPE]	–1551	
23	V_4	[D TYPE]	–1461	
24	V_4	[D TYPE]	–1371	
25	V_3	[D TYPE]	–1282	
26	V_3	[D TYPE]	–1192	
27	V_2	[D TYPE]	–1102	
28	V_2	[D TYPE]	–1013	
29	V_1	[D TYPE]	–923	
30	V_1	[D TYPE]	–833	
31	V_0	[D TYPE]	–744	
32	V_0	[D TYPE]	–654	
33	V_R	[D TYPE]	–564	
34	V_R	[D TYPE]	–474	
35	V_{OUT}	[D TYPE]	–385	
36	V_{OUT}	[D TYPE]	–295	
37	CAP2–	[D TYPE]	–205	
38	CAP2–	[D TYPE]	–116	
39	CAP2+	[D TYPE]	–26	
40	CAP2+	[D TYPE]	64	
41	CAP1–	[D TYPE]	153	
42	CAP1–	[D TYPE]	243	
43	CAP1+	[D TYPE]	333	
44	CAP1+	[D TYPE]	423	
45	V_{SS}	[D TYPE]	512	
46	V_{SS}	[D TYPE]	602	
47	V_{SS2}	[D TYPE]	692	
48	V_{SS2}	[D TYPE]	781	
49	V_{DD}	[D TYPE]	871	
50	V_{DD}	[D TYPE]	961	
51	V_{DD}	[D TYPE]	1050	
52	$\overline{CK}$	[C TYPE]	1183	
53	V_{S1}	[C TYPE]	1303	
54	V_{SS}	[C TYPE]	1423	↓

PAD			COORDINATES	
No.	Name	[BUMP TYPE]	X	Y
55	P/S	[C TYPE]	1543	–1237
56	V_{DD}	[C TYPE]	1664	↓
57	IF	[C TYPE]	1784	
58	V_{SS}	[C TYPE]	1904	
59	C86	[C TYPE]	2024	
60	V_{DD}	[C TYPE]	2145	
61	$\overline{RES}$	[C TYPE]	2265	
62	V_{DD}	[C TYPE]	2385	
63	(FSA)	[C TYPE]	2505	
64	(FSB)	[C TYPE]	2636	
65	(FSC)	[C TYPE]	2767	
66	(FS0)	[C TYPE]	2897	
67	(FS1)	[C TYPE]	3028	
68	(FS2)	[C TYPE]	3159	
69	(FS3)	[C TYPE]	3289	
70	V_{DD}	[C TYPE]	3420	
71	V_{DD}	[C TYPE]	3550	
72	NC	[C TYPE]	3689	
73	NC	[C TYPE]	3794	
74	NC	[C TYPE]	3899	↓
75	NC	[B TYPE]	4191	–1250
76	COMSA	[B TYPE]	↓	–1098
77	SEGSF	[B TYPE]		–978
78	SEGSG	[B TYPE]		–858
79	SEGSH	[B TYPE]		–737
80	SEGSI	[B TYPE]		–617
81	SEGSJ	[B TYPE]		–497
82	COMS1	[B TYPE]		–394
83	COM1	[B TYPE]		–305
84	COM2	[B TYPE]		–215
85	COM3	[B TYPE]		–125
86	COM4	[B TYPE]		–36
87	COM5	[B TYPE]		54
88	COM6	[B TYPE]		144
89	COM7	[B TYPE]		234
90	COM8	[B TYPE]		323
91	COM9	[B TYPE]		413
92	COM10	[B TYPE]		503
93	COM11	[B TYPE]		592
94	COM12	[B TYPE]		682
95	COM13	[B TYPE]		772
96	COM14	[B TYPE]		861
97	COM15	[B TYPE]		951
98	COM16	[B TYPE]		1041
99	COMS1	[B TYPE]		1131
100	NC	[B TYPE]	↓	1251
101	NC	[A TYPE]	3915	1240
102	NC	[A TYPE]	3810	↓
103	SEG1	[A TYPE]	3547	
104	SEG2	[A TYPE]	3458	
105	SEG3	[A TYPE]	3368	
106	SEG4	[A TYPE]	3278	
107	SEG5	[A TYPE]	3188	
108	SEG6	[A TYPE]	3099	↓

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
109	SEG7 [A TYPE]	3009	1240
110	SEG8 [A TYPE]	2919	
111	SEG9 [A TYPE]	2830	
112	SEG10 [A TYPE]	2740	
113	SEG11 [A TYPE]	2650	
114	SEG12 [A TYPE]	2561	
115	SEG13 [A TYPE]	2471	
116	SEG14 [A TYPE]	2381	
117	SEG15 [A TYPE]	2291	
118	SEG16 [A TYPE]	2202	
119	SEG17 [A TYPE]	2112	
120	SEG18 [A TYPE]	2022	
121	SEG19 [A TYPE]	1933	
122	SEG20 [A TYPE]	1843	
123	SEG21 [A TYPE]	1753	
124	SEG22 [A TYPE]	1664	
125	SEG23 [A TYPE]	1574	
126	SEG24 [A TYPE]	1484	
127	SEG25 [A TYPE]	1394	
128	SEG26 [A TYPE]	1305	
129	SEG27 [A TYPE]	1215	
130	SEG28 [A TYPE]	1125	
131	SEG29 [A TYPE]	1036	
132	SEG30 [A TYPE]	946	
133	SEG31 [A TYPE]	856	
134	SEG32 [A TYPE]	767	
135	SEG33 [A TYPE]	677	
136	SEG34 [A TYPE]	587	
137	SEG35 [A TYPE]	497	
138	SEG36 [A TYPE]	408	
139	SEG37 [A TYPE]	318	
140	SEG38 [A TYPE]	228	
141	SEG39 [A TYPE]	139	
142	SEG40 [A TYPE]	49	
143	SEG41 [A TYPE]	–41	
144	SEG42 [A TYPE]	–130	
145	SEG43 [A TYPE]	–220	
146	SEG44 [A TYPE]	–310	
147	SEG45 [A TYPE]	–400	
148	SEG46 [A TYPE]	–489	
149	SEG47 [A TYPE]	–579	
150	SEG48 [A TYPE]	–669	
151	SEG49 [A TYPE]	–758	
152	SEG50 [A TYPE]	–848	
153	SEG51 [A TYPE]	–938	
154	SEG52 [A TYPE]	–1027	
155	SEG53 [A TYPE]	–1117	
156	SEG54 [A TYPE]	–1207	
157	SEG55 [A TYPE]	–1297	
158	SEG56 [A TYPE]	–1386	
159	SEG57 [A TYPE]	–1476	

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
160	SEG58 [A TYPE]	–1566	1240
161	SEG59 [A TYPE]	–1655	
162	SEG60 [A TYPE]	–1745	
163	SEG61 [A TYPE]	–1835	
164	SEG62 [A TYPE]	–1924	
165	SEG63 [A TYPE]	–2014	
166	SEG64 [A TYPE]	–2104	
167	SEG65 [A TYPE]	–2194	
168	SEG66 [A TYPE]	–2283	
169	SEG67 [A TYPE]	–2373	
170	SEG68 [A TYPE]	–2463	
171	SEG69 [A TYPE]	–2552	
172	SEG70 [A TYPE]	–2642	
173	SEG71 [A TYPE]	–2732	
174	SEG72 [A TYPE]	–2821	
175	SEG73 [A TYPE]	–2911	
176	SEG74 [A TYPE]	–3001	
177	SEG75 [A TYPE]	–3091	
178	SEG76 [A TYPE]	–3180	
179	SEG77 [A TYPE]	–3270	
180	SEG78 [A TYPE]	–3360	
181	SEG79 [A TYPE]	–3449	
182	SEG80 [A TYPE]	–3539	
183	NC [A TYPE]	–3704	
184	NC [A TYPE]	–3810	
185	NC [A TYPE]	–3915	
186	NC [B TYPE]	–4191	1251
187	COMS2 [B TYPE]		1131
188	COM32 [B TYPE]		1041
189	COM31 [B TYPE]		951
190	COM30 [B TYPE]		861
191	COM29 [B TYPE]		772
192	COM28 [B TYPE]		682
193	COM27 [B TYPE]		592
194	COM26 [B TYPE]		503
195	COM25 [B TYPE]		413
196	COM24 [B TYPE]		323
197	COM23 [B TYPE]		234
198	COM22 [B TYPE]		144
199	COM21 [B TYPE]		54
200	COM20 [B TYPE]		–36
201	COM19 [B TYPE]		–125
202	COM18 [B TYPE]		–215
203	COM17 [B TYPE]		–305
204	COMS2 [B TYPE]		–394
205	SEGSA [B TYPE]		–497
206	SEGSB [B TYPE]		–617
207	SEGSC [B TYPE]		–737
208	SEGSD [B TYPE]		–858
209	SEGSE [B TYPE]		–978
210	COMSA [B TYPE]		–1098

($\overline{FS}$*) : This is a FUSE adjusting pin. Set it is the floating state.
$\overline{CK}$ pin : Fix it to V_{DD} when it is not used.

<Pad coordinates> SED1241$_{***}$

PAD No.	PAD Name	[BUMP TYPE]	COORDINATES X	COORDINATES Y
1	NC	[B TYPE]	–4191	–1250
2	NC	[C TYPE]	–3941	–1237
3	NC	[C TYPE]	–3836	↓
4	NC	[C TYPE]	–3555	
5	A0	[C TYPE]	–3403	
6	$\overline{WR}$	[C TYPE]	–3283	
7	$\overline{CS}$	[C TYPE]	–3163	
8	D7	[C TYPE]	–3043	
9	D6	[C TYPE]	–2922	
10	D5	[C TYPE]	–2802	
11	D4	[C TYPE]	–2682	
12	D3	[C TYPE]	–2562	
13	D2	[C TYPE]	–2441	
14	D1	[C TYPE]	–2321	
15	D0	[C TYPE]	–2201	
16	V_{DD}	[D TYPE]	–2089	
17	V_{DD}	[D TYPE]	–1999	
18	V_{DD}	[D TYPE]	–1909	
19	V_{SS}	[D TYPE]	–1820	
20	V_{SS}	[D TYPE]	–1730	
21	V_5	[D TYPE]	–1641	
22	V_5	[D TYPE]	–1551	
23	V_4	[D TYPE]	–1461	
24	V_4	[D TYPE]	–1371	
25	V_3	[D TYPE]	–1282	
26	V_3	[D TYPE]	–1192	
27	V_2	[D TYPE]	–1102	
28	V_2	[D TYPE]	–1013	
29	V_1	[D TYPE]	–923	
30	V_1	[D TYPE]	–833	
31	V_0	[D TYPE]	–744	
32	V_0	[D TYPE]	–654	
33	V_R	[D TYPE]	–564	
34	V_R	[D TYPE]	–474	
35	V_{OUT}	[D TYPE]	–385	
36	V_{OUT}	[D TYPE]	–295	
37	CAP2–	[D TYPE]	–205	
38	CAP2–	[D TYPE]	–116	
39	CAP2+	[D TYPE]	–26	
40	CAP2+	[D TYPE]	64	
41	CAP1–	[D TYPE]	153	
42	CAP1–	[D TYPE]	243	
43	CAP1+	[D TYPE]	333	
44	CAP1+	[D TYPE]	423	
45	V_{SS}	[D TYPE]	512	
46	V_{SS}	[D TYPE]	602	
47	V_{SS2}	[D TYPE]	692	
48	V_{SS2}	[D TYPE]	781	
49	V_{DD}	[D TYPE]	871	
50	V_{DD}	[D TYPE]	961	
51	V_{DD}	[D TYPE]	1050	
52	$\overline{CK}$	[C TYPE]	1183	
53	V_{S1}	[C TYPE]	1303	
54	V_{SS}	[C TYPE]	1423	↓
55	P/S	[C TYPE]	1543	–1237
56	V_{DD}	[C TYPE]	1664	↓
57	IF	[C TYPE]	1784	
58	V_{SS}	[C TYPE]	1904	
59	C86	[C TYPE]	2024	
60	V_{DD}	[C TYPE]	2145	
61	$\overline{RES}$	[C TYPE]	2265	
62	V_{DD}	[C TYPE]	2385	
63	(FSA)	[C TYPE]	2505	
64	(FSB)	[C TYPE]	2636	
65	(FSC)	[C TYPE]	2767	
66	(FS0)	[C TYPE]	2897	
67	(FS1)	[C TYPE]	3028	
68	(FS2)	[C TYPE]	3159	
69	(FS3)	[C TYPE]	3289	
70	V_{DD}	[C TYPE]	3420	
71	V_{DD}	[C TYPE]	3550	
72	NC	[C TYPE]	3689	
73	NC	[C TYPE]	3794	
74	NC	[C TYPE]	3899	↓
75	NC	[B TYPE]	4191	–1250
76	COMSA	[B TYPE]	↓	–1098
77	SEGSF	[B TYPE]		–978
78	SEGSG	[B TYPE]		–858
79	SEGSH	[B TYPE]		–737
80	SEGSI	[B TYPE]		–617
81	SEGSJ	[B TYPE]		–497
82	COMS1	[B TYPE]		–394
83	COM1	[B TYPE]		–305
84	COM2	[B TYPE]		–215
85	COM3	[B TYPE]		–125
86	COM4	[B TYPE]		–36
87	COM5	[B TYPE]		54
88	COM6	[B TYPE]		144
89	COM7	[B TYPE]		234
90	COM8	[B TYPE]		323
91	COM9	[B TYPE]		413
92	COM10	[B TYPE]		503
93	COM11	[B TYPE]		592
94	COM12	[B TYPE]		682
95	COM13	[B TYPE]		772
96	COM14	[B TYPE]		861
97	COM15	[B TYPE]		951
98	COM16	[B TYPE]		1041
99	COMS1	[B TYPE]		1131
100	NC	[B TYPE]	↓	1251
101	NC	[A TYPE]	3915	1240
102	NC	[A TYPE]	3810	↓
103	SEG1	[A TYPE]	3547	
104	SEG2	[A TYPE]	3458	
105	SEG3	[A TYPE]	3368	
106	SEG4	[A TYPE]	3278	
107	SEG5	[A TYPE]	3188	
108	SEG6	[A TYPE]	3099	↓

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
109	SEG7 [A TYPE]	3009	1240
110	SEG8 [A TYPE]	2919	
111	SEG9 [A TYPE]	2830	
112	SEG10 [A TYPE]	2740	
113	SEG11 [A TYPE]	2650	
114	SEG12 [A TYPE]	2561	
115	SEG13 [A TYPE]	2471	
116	SEG14 [A TYPE]	2381	
117	SEG15 [A TYPE]	2291	
118	SEG16 [A TYPE]	2202	
119	SEG17 [A TYPE]	2112	
120	SEG18 [A TYPE]	2022	
121	SEG19 [A TYPE]	1933	
122	SEG20 [A TYPE]	1843	
123	SEG21 [A TYPE]	1753	
124	SEG22 [A TYPE]	1664	
125	SEG23 [A TYPE]	1574	
126	SEG24 [A TYPE]	1484	
127	SEG25 [A TYPE]	1394	
128	SEG26 [A TYPE]	1305	
129	SEG27 [A TYPE]	1215	
130	SEG28 [A TYPE]	1125	
131	SEG29 [A TYPE]	1036	
132	SEG30 [A TYPE]	946	
133	SEG31 [A TYPE]	856	
134	SEG32 [A TYPE]	767	
135	SEG33 [A TYPE]	677	
136	SEG34 [A TYPE]	587	
137	SEG35 [A TYPE]	497	
138	SEG36 [A TYPE]	408	
139	SEG37 [A TYPE]	318	
140	SEG38 [A TYPE]	228	
141	SEG39 [A TYPE]	139	
142	SEG40 [A TYPE]	49	
143	SEG41 [A TYPE]	–41	
144	SEG42 [A TYPE]	–130	
145	SEG43 [A TYPE]	–220	
146	SEG44 [A TYPE]	–310	
147	SEG45 [A TYPE]	–400	
148	SEG46 [A TYPE]	–489	
149	SEG47 [A TYPE]	–579	
150	SEG48 [A TYPE]	–669	
151	SEG49 [A TYPE]	–758	
152	SEG50 [A TYPE]	–848	
153	SEG51 [A TYPE]	–938	
154	SEG52 [A TYPE]	–1027	
155	SEG53 [A TYPE]	–1117	
156	SEG54 [A TYPE]	–1207	
157	SEG55 [A TYPE]	–1297	
158	SEG56 [A TYPE]	–1386	
159	SEG57 [A TYPE]	–1476	

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
160	SEG58 [A TYPE]	–1566	1240
161	SEG59 [A TYPE]	–1655	
162	SEG60 [A TYPE]	–1745	
163	SEG61 [A TYPE]	–1835	
164	SEG62 [A TYPE]	–1924	
165	SEG63 [A TYPE]	–2014	
166	SEG64 [A TYPE]	–2104	
167	SEG65 [A TYPE]	–2194	
168	SEG66 [A TYPE]	–2283	
169	SEG67 [A TYPE]	–2373	
170	SEG68 [A TYPE]	–2463	
171	SEG69 [A TYPE]	–2552	
172	SEG70 [A TYPE]	–2642	
173	SEG71 [A TYPE]	–2732	
174	SEG72 [A TYPE]	–2821	
175	SEG73 [A TYPE]	–2911	
176	SEG74 [A TYPE]	–3001	
177	SEG75 [A TYPE]	–3091	
178	SEG76 [A TYPE]	–3180	
179	SEG77 [A TYPE]	–3270	
180	SEG78 [A TYPE]	–3360	
181	SEG79 [A TYPE]	–3449	
182	SEG80 [A TYPE]	–3539	
183	NC [A TYPE]	–3704	
184	NC [A TYPE]	–3810	
185	NC [A TYPE]	–3915	
186	NC [B TYPE]	–4191	1251
187	COMS2 [B TYPE]		1131
188	*COM32 [B TYPE]		1041
189	*COM31 [B TYPE]		951
190	*COM30 [B TYPE]		861
191	*COM29 [B TYPE]		772
192	*COM28 [B TYPE]		682
193	*COM27 [B TYPE]		592
194	*COM26 [B TYPE]		503
195	*COM25 [B TYPE]		413
196	*COM24 [B TYPE]		323
197	*COM23 [B TYPE]		234
198	*COM22 [B TYPE]		144
199	*COM21 [B TYPE]		54
200	*COM20 [B TYPE]		–36
201	*COM19 [B TYPE]		–125
202	*COM18 [B TYPE]		–215
203	*COM17 [B TYPE]		–305
204	COMS2 [B TYPE]		–394
205	SEGSA [B TYPE]		–497
206	SEGSB [B TYPE]		–617
207	SEGSC [B TYPE]		–737
208	SEGSD [B TYPE]		–858
209	SEGSE [B TYPE]		–978
210	COMSA [B TYPE]		–1098

(FS*) : This is a FUSE adjusting pin. Set it in the floating state.
CK pin : Fix it to VDD when it is not used.
*: Don't connect COM17 to COM32.

<Pad coordinates> SED1242***

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
1	NC [B TYPE]	–4191	–1250
2	NC [C TYPE]	–3941	–1237
3	NC [C TYPE]	–3836	↓
4	NC [C TYPE]	–3555	
5	A0 [C TYPE]	–3403	
6	$\overline{WR}$ [C TYPE]	–3283	
7	$\overline{CS}$ [C TYPE]	–3163	
8	D7 [C TYPE]	–3043	
9	D6 [C TYPE]	–2922	
10	D5 [C TYPE]	–2802	
11	D4 [C TYPE]	–2682	
12	D3 [C TYPE]	–2562	
13	D2 [C TYPE]	–2441	
14	D1 [C TYPE]	–2321	
15	D0 [C TYPE]	–2201	
16	V_{DD} [D TYPE]	–2089	
17	V_{DD} [D TYPE]	–1999	
18	V_{DD} [D TYPE]	–1909	
19	V_{SS} [D TYPE]	–1820	
20	V_{SS} [D TYPE]	–1730	
21	V_5 [D TYPE]	–1641	
22	V_5 [D TYPE]	–1551	
23	V_4 [D TYPE]	–1461	
24	V_4 [D TYPE]	–1371	
25	V_3 [D TYPE]	–1282	
26	V_3 [D TYPE]	–1192	
27	V_2 [D TYPE]	–1102	
28	V_2 [D TYPE]	–1013	
29	V_1 [D TYPE]	–923	
30	V_1 [D TYPE]	–833	
31	V_0 [D TYPE]	–744	
32	V_0 [D TYPE]	–654	
33	V_R [D TYPE]	–564	
34	V_R [D TYPE]	–474	
35	V_{OUT} [D TYPE]	–385	
36	V_{OUT} [D TYPE]	–295	
37	CAP2– [D TYPE]	–205	
38	CAP2– [D TYPE]	–116	
39	CAP2+ [D TYPE]	–26	
40	CAP2+ [D TYPE]	64	
41	CAP1– [D TYPE]	153	
42	CAP1– [D TYPE]	243	
43	CAP1+ [D TYPE]	333	
44	CAP1+ [D TYPE]	423	
45	V_{SS} [D TYPE]	512	
46	V_{SS} [D TYPE]	602	
47	V_{SS2} [D TYPE]	692	
48	V_{SS2} [D TYPE]	781	
49	V_{DD} [D TYPE]	871	
50	V_{DD} [D TYPE]	961	
51	V_{DD} [D TYPE]	1050	
52	$\overline{CK}$ [C TYPE]	1183	
53	V_{S1} [C TYPE]	1303	
54	V_{SS} [C TYPE]	1423	
55	P/S [C TYPE]	1543	–1237
56	V_{DD} [C TYPE]	1664	↓
57	IF [C TYPE]	1784	
58	V_{SS} [C TYPE]	1904	
59	C86 [C TYPE]	2024	
60	V_{DD} [C TYPE]	2145	
61	$\overline{RES}$ [C TYPE]	2265	
62	V_{DD} [C TYPE]	2385	
63	(FSA) [C TYPE]	2505	
64	(FSB) [C TYPE]	2636	
65	(FSC) [C TYPE]	2767	
66	(FS0) [C TYPE]	2897	
67	(FS1) [C TYPE]	3028	
68	(FS2) [C TYPE]	3159	
69	(FS3) [C TYPE]	3289	
70	V_{DD} [C TYPE]	3420	
71	V_{DD} [C TYPE]	3550	
72	NC [C TYPE]	3689	
73	NC [C TYPE]	3794	
74	NC [C TYPE]	3899	
75	NC [B TYPE]	4191	–1250
76	COMSA [B TYPE]	↓	–1098
77	SEGSF [B TYPE]		–978
78	SEGSG [B TYPE]		–858
79	SEGSH [B TYPE]		–737
80	SEGSI [B TYPE]		–617
81	SEGSJ [B TYPE]		–497
82	COMS1 [B TYPE]		–394
83	COM1 [B TYPE]		–305
84	COM2 [B TYPE]		–215
85	COM3 [B TYPE]		–125
86	COM4 [B TYPE]		–36
87	COM5 [B TYPE]		54
88	COM6 [B TYPE]		144
89	COM7 [B TYPE]		234
90	COM8 [B TYPE]		323
91	COM9 [B TYPE]		413
92	COM10 [B TYPE]		503
93	COM11 [B TYPE]		592
94	COM12 [B TYPE]		682
95	COM13 [B TYPE]		772
96	COM14 [B TYPE]		861
97	COM15 [B TYPE]		951
98	COM16 [B TYPE]		1041
99	COMS1 [B TYPE]		1131
100	NC [B TYPE]		1251
101	NC [A TYPE]	3915	1240
102	NC [A TYPE]	3810	↓
103	SEG1 [A TYPE]	3547	
104	SEG2 [A TYPE]	3458	
105	SEG3 [A TYPE]	3368	
106	SEG4 [A TYPE]	3278	
107	SEG5 [A TYPE]	3188	
108	SEG6 [A TYPE]	3099	

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
109	SEG7 [A TYPE]	3009	1240
110	SEG8 [A TYPE]	2919	
111	SEG9 [A TYPE]	2830	
112	SEG10 [A TYPE]	2740	
113	SEG11 [A TYPE]	2650	
114	SEG12 [A TYPE]	2561	
115	SEG13 [A TYPE]	2471	
116	SEG14 [A TYPE]	2381	
117	SEG15 [A TYPE]	2291	
118	SEG16 [A TYPE]	2202	
119	SEG17 [A TYPE]	2112	
120	SEG18 [A TYPE]	2022	
121	SEG19 [A TYPE]	1933	
122	SEG20 [A TYPE]	1843	
123	SEG21 [A TYPE]	1753	
124	SEG22 [A TYPE]	1664	
125	SEG23 [A TYPE]	1574	
126	SEG24 [A TYPE]	1484	
127	SEG25 [A TYPE]	1394	
128	SEG26 [A TYPE]	1305	
129	SEG27 [A TYPE]	1215	
130	SEG28 [A TYPE]	1125	
131	SEG29 [A TYPE]	1036	
132	SEG30 [A TYPE]	946	
133	SEG31 [A TYPE]	856	
134	SEG32 [A TYPE]	767	
135	SEG33 [A TYPE]	677	
136	SEG34 [A TYPE]	587	
137	SEG35 [A TYPE]	497	
138	SEG36 [A TYPE]	408	
139	SEG37 [A TYPE]	318	
140	SEG38 [A TYPE]	228	
141	SEG39 [A TYPE]	139	
142	SEG40 [A TYPE]	49	
143	SEG41 [A TYPE]	–41	
144	SEG42 [A TYPE]	–130	
145	SEG43 [A TYPE]	–220	
146	SEG44 [A TYPE]	–310	
147	SEG45 [A TYPE]	–400	
148	SEG46 [A TYPE]	–489	
149	SEG47 [A TYPE]	–579	
150	SEG48 [A TYPE]	–669	
151	SEG49 [A TYPE]	–758	
152	SEG50 [A TYPE]	–848	
153	SEG51 [A TYPE]	–938	
154	SEG52 [A TYPE]	–1027	
155	SEG53 [A TYPE]	–1117	
156	SEG54 [A TYPE]	–1207	
157	SEG55 [A TYPE]	–1297	
158	SEG56 [A TYPE]	–1386	
159	SEG57 [A TYPE]	–1476	

PAD		COORDINATES	
No.	Name [BUMP TYPE]	X	Y
160	SEG58 [A TYPE]	–1566	1240
161	SEG59 [A TYPE]	–1655	
162	SEG60 [A TYPE]	–1745	
163	SEG61 [A TYPE]	–1835	
164	SEG62 [A TYPE]	–1924	
165	SEG63 [A TYPE]	–2014	
166	SEG64 [A TYPE]	–2104	
167	SEG65 [A TYPE]	–2194	
168	SEG66 [A TYPE]	–2283	
169	SEG67 [A TYPE]	–2373	
170	SEG68 [A TYPE]	–2463	
171	SEG69 [A TYPE]	–2552	
172	SEG70 [A TYPE]	–2642	
173	SEG71 [A TYPE]	–2732	
174	SEG72 [A TYPE]	–2821	
175	SEG73 [A TYPE]	–2911	
176	SEG74 [A TYPE]	–3001	
177	SEG75 [A TYPE]	–3091	
178	SEG76 [A TYPE]	–3180	
179	SEG77 [A TYPE]	–3270	
180	SEG78 [A TYPE]	–3360	
181	SEG79 [A TYPE]	–3449	
182	SEG80 [A TYPE]	–3539	
183	NC [A TYPE]	–3704	
184	NC [A TYPE]	–3810	
185	NC [A TYPE]	–3915	
186	NC [B TYPE]	–4191	1251
187	COMS2 [B TYPE]		1131
188	*COM32 [B TYPE]		1041
189	*COM31 [B TYPE]		951
190	*COM30 [B TYPE]		861
191	*COM29 [B TYPE]		772
192	*COM28 [B TYPE]		682
193	*COM27 [B TYPE]		592
194	*COM26 [B TYPE]		503
195	*COM25 [B TYPE]		413
196	*COM24 [B TYPE]		323
197	*COM23 [B TYPE]		234
198	*COM22 [B TYPE]		144
199	*COM21 [B TYPE]		54
200	*COM20 [B TYPE]		–36
201	*COM19 [B TYPE]		–125
202	*COM18 [B TYPE]		–215
203	*COM17 [B TYPE]		–305
204	COMS2 [B TYPE]		–394
205	SEGSA [B TYPE]		–497
206	SEGSB [B TYPE]		–617
207	SEGSC [B TYPE]		–737
208	SEGSD [B TYPE]		–858
209	SEGSE [B TYPE]		–978
210	COMSA [B TYPE]		–1098

(FS*) : This is a FUSE adjusting pin. Set it in the floating state.
CK pin : Fix it to VDD when it is not used.
*: Don't connect COM17 to COM32.

DESCRIPTION OF PINS

Power Pins

Pin name	I/O	Description	Q'ty
Board potential		IC board is based on V_{DD} potential. To lock the board potential with V_{DD}.	
V_{DD}	Power supply	Connected to the logic power supply. This is used in common with the MPU power pin V_{CC}.	6
V_{SS}	Power supply	0 V power pin that is connected to system GND.	4
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined for the liquid crystal cell is applied by resistance-division or impedance conversion by operational amplifier. The potential is determined on V_{DD} and the following relations must be observed. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{DD} \geq V_5 \geq V_{OUT}$ $V_{DD} \geq V_{SS} \geq V_{SS2} \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to V1 to V4 by command selection. $V_1 = 1/5\ V_5$ (1/4 V_5) $V_2 = 2/5\ V_5$ (2/4 V_5) $V_3 = 3/5\ V_5$ (2/4 V_5) $V_4 = 4/5\ V_5$ (3/4 V_5)	6
V_{S1}	O	Supply voltage output pin for oscillating circuit. Don't connect a load to the outside.	1

LCD Power Circuit Pins

Pin name	I/O	Description	Q'ty
CAP1+	O	Boosting condenser positive side connecting pin. Condenser is connected with the CAP1– pin.	1
CAP1–	O	Boosting condenser negative side connecting pin. Condenser is connected with the CAP1+ pin.	1
CAP2+	O	Boosting condenser positive side connecting pin. Condenser is connected with the CAP2– pin.	1
CAP2–	O	A boosting condenser negative side connecting pin. Condenser is connected with the CAP2+ pin.	1
V_{OUT}	O	Output pin for boosting. Smoothing condenser is connected with V_{DD}.	1
V_R	I	Voltage adjusting pin. Voltage between V_{DD} and V_5 is given by resistance-division.	1
V_{SS2}	I	Boosting power pin. The voltage between V_{DD} and V_{SS2} is boosted by a specified multiple.	1

System Bus Connecting Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Q'ty</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 to D0</td><td>I</td><td>8-bit input data bus which is connected to the 16-bit standard MPU data bus.
Pin D7 and pin D6 function as a serial data input and a serial clock input at P/S = "L", respectively.
<table>
<tr><th>Pin / Mode</th><th>P/S</th><th>C86</th><th>I/F</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3-D0</th><th>$\overline{\text{CS}}$</th><th>A0</th><th>$\overline{\text{WR}}$</th></tr>
<tr><td>Serial I/F</td><td>"L"</td><td>H or L</td><td>—</td><td>SI</td><td>SCL</td><td>OPEN</td><td>OPEN</td><td>OPEN</td><td>$\overline{\text{CS}}$</td><td>A0</td><td>—</td></tr>
<tr><td>68I/F 8bit</td><td>"H"</td><td>"H"</td><td>"H"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{\text{CS}}$</td><td>A0</td><td>E</td></tr>
<tr><td>68I/F 4bit</td><td>"H"</td><td>"H"</td><td>"L"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{\text{CS}}$</td><td>A0</td><td>E</td></tr>
<tr><td>80I/F 8bit</td><td>"H"</td><td>"L"</td><td>"H"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{\text{CS}}$</td><td>A0</td><td>$\overline{\text{WR}}$</td></tr>
<tr><td>80I/F 4bit</td><td>"H"</td><td>"L"</td><td>"L"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{\text{CS}}$</td><td>A0</td><td>$\overline{\text{WR}}$</td></tr>
</table>
C86: An MPU selecting pin
OPEN: OPEN is allowable, but it is recommend to fix it to one of potentials as a matter of noise-resistance characteristic.
—: Either "H" or "L" is allowable, but the potential should be fixed.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually used to distinguish data from a command to which the LSB of the MPU address bus is connected.
"L" : Indicates that D0 to D7 are of a command.
"H" : Indicates that D0 to D7 are of data.</td><td>1</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I</td><td>Reset pin for initializing the whole IC. Be sure to input it once when the power supply is turned on. A reset operation is performed at the "L" level of the $\overline{\text{RES}}$ signal.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU selecting pin. Fix it to "H" or "L" depending on the MPU to be used.
"L" : 80 series MPU interface
"H" : 68 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{\text{CS}}$</td><td>I</td><td>Chip selecting pin. Usually, it inputs a signal that is obtained by decoding an address signal. Chip selection is enabled at the "L" level.</td><td>1</td></tr>
<tr><td>$\overline{\text{WR}}$
(E)</td><td>I</td><td><When the 80 series MPU is selected> Active "L"
A pin for connecting the WR signal of the 80 series MPU.
The signal on the data bus is latched at the rise of the $\overline{\text{WR}}$ signal.
<When the 68 series MPU is connected> Active "H"
Becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>A pin for selecting either serial interface or parallel interface.
"L" : Serial interface
"H" : Parallel interface</td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>A data bit length selecting pin at parallel interface.
"H" : 8-bit parallel interface
"L" : 4-bit parallel interface
At P/S = "L", set pins D3 to D0 to V_{DD} or V_{SS}, or OPEN.</td><td>1</td></tr>
<tr><td>$\overline{\text{CK}}$</td><td>I</td><td>An external clock input pin.
When using the internal oscillating circuit, fix it to "H".
When using an external clock input, the internal oscillating circuit must be turned off by command.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

Dynamic Drive Pins [SED1240]

Pin name	I/O	Description	Q'ty
COM1 to COM32	O	Common signal output pins (for characters)	32
COMS1, COMS2	O	Common signal output pins (for others than characters) COMS1, COMS2: Symbol output command output	4
SEG1 to SEG80	O	Segment signal output pins (for characters)	80

Dynamic Drive Pins [SED1241]

Pin name	I/O	Description	Q'ty
COM1 to COM24	O	Common signal output pins (for characters)	16
COMS1, COMS2	O	Common signal output pins (for others than characters) CMOS1, CMOS2: Symbol display common output	4
SEG1 to SEG80	O	Segment signal output pins (for characters)	80

Dynamic Drive Pins [SED1242]

Pin name	I/O	Description	Q'ty
COM1 to COM16	O	Common signal output pins (for characters) (Keep COM17 to COM32 unconnected.)	16
COMS1, COMS2	O	Common signal output pins (for others than characters) CMOS1, CMOS2: Symbol display common output	4
SEG1 to SEG80	O	Segment signal output pins (for characters)	80

Static Drive Pins

Pin name	I/O	Description	Q'ty
COMSA	O	Common signal output pin (for static icons)	2
SEGS A to J	O	Segment signal output pins (for static icons)	10

Note: For the electrode of the liquid crystal display panel connected to the static drive terminal, it is recommended use the pattern separated from the electrode connected to the dynamic drive terminal. If this pattern is too close, the liquid crystal and electrode may be deteriorated.

DESCRIPTION OF FUNCTIONS

MPU Interfaces

In the SED1240 series, an MPU type, interface bit length and interface method can be selected depending on pins IF, P/S and C86.

Selection of MPU

In the SED1240 series, when parallel input is selected (P/S = “H”), pin C86 has an MPU selecting function.
When either “H” or “L” is selected as the polarity of pin C86, the 80 series MPU or 68 series MPU can be selected as shown in Table 1.
Selection of an interface bit length (8 bits, 4 bits) is performed by pin IF.

Table 1

MPU type	Pin C86 state	Polarity of $\overline{RES}$ function input	MPU connection			
			A0	$\overline{WR}$	$\overline{CS}$	D0 to D7
68 series	High level	Low level active	A0	E	$\overline{CS}$	D0 to D7
80 series	Low level		A0	$\overline{WR}$	$\overline{CS}$	D0 to D7

Selection of interface type

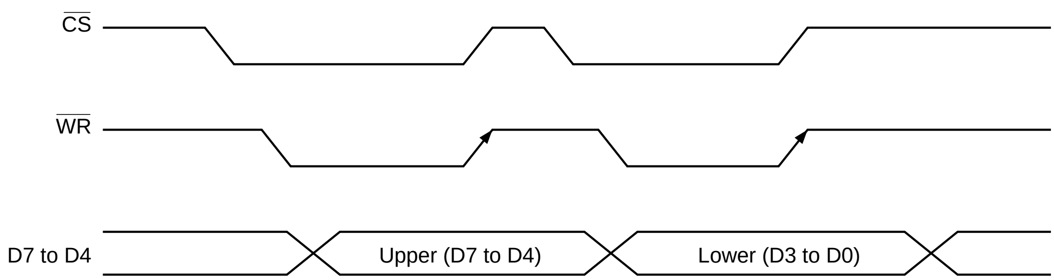
In the SED1240 series, it is possible to select an 8-bit or 4-bit parallel interface or a serial interface that permits a data transfer through a serial input (SI). As the selecting method, set the polarity of pins of P/S and IF to “H” or “L”.

Table 2

Interface type	Interface bit length	Selecting pin state		Pin state										
		P/S	IF	$\overline{CS}$	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Parallel	8 bits	H	H	$\overline{CS}$	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Parallel	4 bits	H	L	$\overline{CS}$	A0	$\overline{WR}$	D7	D6	D5	D4	OPEN or H or L			
Serial	1 bit	L	H or L	$\overline{CS}$	A0	H or L	SI	SCL	OPEN or H or L					

Interface with 4-bit MPU

When data is transferred by a 4-bit interface (IF = 0), 8-bit commands, data and addresses are divided into 2 parts for transfer. A timing example of the 80 series MPU is shown below.



Note: For continuous writing, perform it after securing a time exceeding the system cycle time (t_{cyc}).

Serial interface (P/S = “L”)

The serial interface consists of an 8-bit shift register and a 3-bit counter, and becomes ready to accept an SI input or SCL input in the chip selected state ($\overline{CS}$ = “L”).
Unless any chip is selected, the shift register and the counter are reset to the initial state. (Refresh state)
Data is input in the order of D7, D6, ... D0 from the serial data input pin (SI) at the rise of the serial clock (SCL). At the rising edge of the 8th serial clock, the data is converted into parallel data.
Whether the serial data input (SI) is display data or a command is identified and judged by A0 input. When A0 = “H”, the data becomes display data. When A0 = “L”, the data becomes a command. The A0 input is read and identified at the rise of the 8 × nth serial clock (SCL) after chip selection.

Fig. 1 shows a timing chart of the serial interface. In case of the SCL signal, extreme care should be taken about terminal reflection and external noise due to a wiring length. Accordingly, it is recommended to make an operation check.
It is also recommended to periodically refresh the each command write state to prevent a malfunction from being caused by noise.

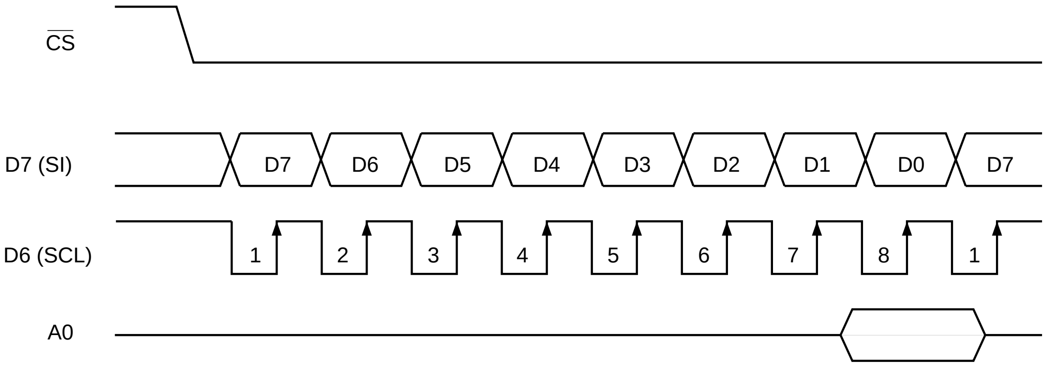


Fig. 1 Serial Interface Input Timing

Identification of data bus signals

The SED1240 series identifies each data bus signal by a combination of A0 and $\overline{WR}$ (E) as shown in Table 3.

Table 3

Common	68 series	80 series	Function
A0	(E)	$\overline{WR}$	
1	1	0	Writes into the RAM and symbol register.
0	1	0	Writes into the internal register (commands)

Chip select

The SED1240 series has chip select pin $\overline{CS}$. Only when $\overline{CS}$ = "L", the MPU interface is enabled. In the other states than the chip select state, D0 to D7 and A0, $\overline{WR}$, SI, and SCL inputs are invalidated. When an serial input interface is selected, the shift register and the counter are reset. However, the $\overline{RES}$ input can be performed regardless of the $\overline{CS}$ state.

Power Circuit

The power circuit built in the SED1240 series is a low power consumption power circuit that generates a voltage required for liquid crystal drive, and consists of a boosting circuit, voltage regulating circuit, and voltage follower.
The power circuit capacity is set for a small-scale liquid crystal panel.
In the case of a liquid crystal panel with a large display capacity, the display quality may be remarkably degraded. In this case, an external power supply is required.
Functional selection is performed by power control commands.
Some parts of the external power supply and the internal power supply can be used together.

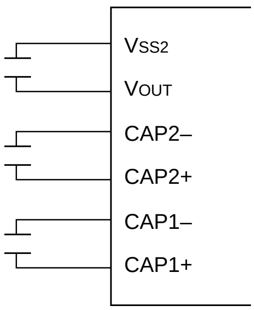
Table 4

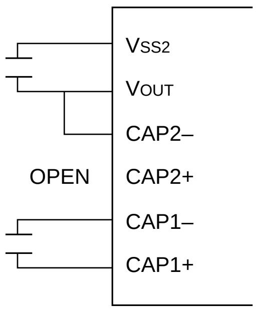
	Boosting circuit	Voltage regulat-ing circuit	Voltage follower	External voltage input	Boosting system pin
	○	○	○	V_{SS2}	USE
Note 1	×	○	○	V_{OUT}, V_{SS2}	OPEN
Note 2	×	×	○	V_5, V_{SS2}	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

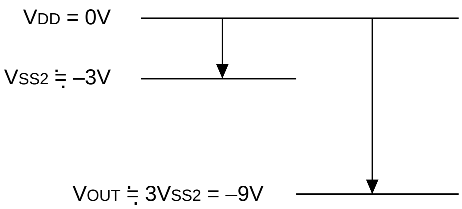
Note 1: When the boosting circuit is turned off, set the boosting system pins (CAP1+, CAP1–, CAP2+, CAP2–) to OPEN so that liquid crystal drive voltages may be applied to the V_{OUT} pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, set the V_{OUT} pin and the boosting system pins to OPEN and connect the V_5 pin to give liquid crystal drive voltages from the outside.
Note 3: When all the built-in power supplies are turned off, liquid crystal drive voltages V_1, V_2, V_3, V_4, and V_5 are supplied from the outside and set the CAP1+, CAP1–, V_{SS2} and V_{OUT} pins to OPEN.

Boosting circuit

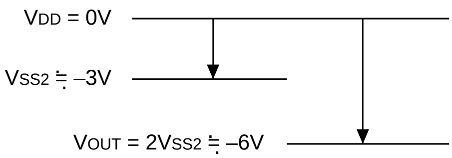
The SED1240 series is provided with a boosting circuit for triple boosting and double boosting for the potential between V_{DD} and V_{SS2}.
For triple boosting, connect a capacitor between CAP1+ and CAP1–, between CAP2+ and CAP2–, and between V_{DD} and V_{OUT}, and the V_{DD} - V_{SS2} potential is triple-boosted to the negative side and output to the V_{OUT} pin.
For double boosting, connect a capacitor between CAP1+ and CAP1– and between V_{DD} and V_{OUT}, set CAP2+ to OPEN, and connect CAP2– to V_{OUT}, and the V_{DD} - V_{SS2} potential is double-boosted to the negative side and output to the V_{OUT} pin.
Because the boosting circuit uses signals from the oscillator output, the internal oscillating circuit or the external clock must be in operation.
The relation of boosting voltages is shown below.
Set the potential between the V_{DD} and V_{SS2} to ensure that the V_{OUT} does not exceed the permissible operating voltage range of V_{SS} - V_{OUT} (V_5) when double or triple boosted.







Potential relation of triple boosting voltages



Potential relation of double boosting voltages

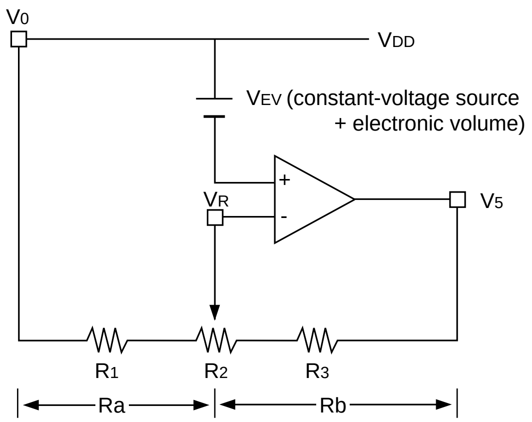
* Set the V_{SS2} voltage range to ensure that V_{OUT} terminal voltage does not exceed the permissible operating voltage range of V_{SS} - V_{OUT} and absolute maximum rating.

SED1240 Series

Voltage regulating circuit

The boosting voltage generated at V_{OUT} is output as a liquid crystal drive voltage of V_5 through the voltage regulating circuit.
The SED1240 series is provided with a high-precision constant-voltage source, a 32-step electronic volume function, and a V_5 voltage regulating resistor. This permits constructing a high-precision voltage regulating circuit with a small quantity of parts. The voltage regulating circuit outputs V_{EV} and has a temperature gradient of about –0.04%.
As the V_5 voltage regulating resistor, a built-in resistor or an external resistor can be selected by command as a matter of configuration.

[When using an external resistor (No use of V_5 voltage regulating built-in resistor is set by command.)]
The V_5 voltage can be obtained from the following expression ① by adjusting resistors Ra and Rb within the range of $| V_5 | < | V_{OUT} |$.



$$V_5 = \left(1 + \frac{R_b}{R_a}\right) \cdot V_{EV} \quad \cdots\cdots ①$$

In this case, V_{EV} is determined by the constant-voltage source in the IC and by setting the electronic volume. When the electronic volume value is (00000), $V_{REG} \fallingdotseq 2.0$ V, being constant.
For voltage adjustment of V_5 output, connect a variable resistor among V_R, V_{DD}, and V_5. For fine voltage adjustment of V_5 output, it is recommended to combine fixed resistors R1 and R3 with variable resistor R2.

[R1, R2 and R3 setup example]
- R1 + R2 + R3 = 1.2 MΩ (Determined by the current value I_{05} flowing between V_{DD} and V_5. Supposing $I_{05} \leq 5$ μA)
- Minimum voltage of V_5: –6 V (Determined by liquid crystal characteristic)
- Variable voltage range by R2: –4 to –6 V (Determined by the liquid crystal characteristic)
- When the electronic volume register is set to (0, 0, 0, 0, 0), V_{EV} = 2.0 V (TYP). Accordingly, each resistor value can be calculated by the above conditions and expression ① as follows.

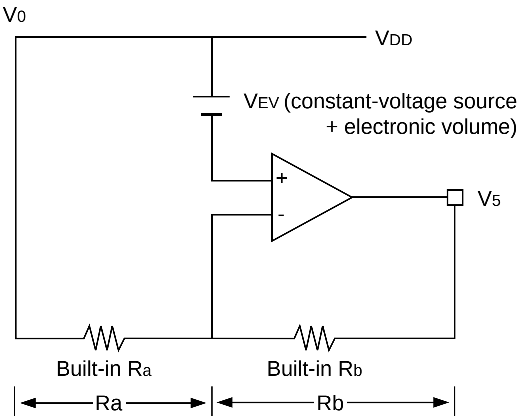
R1 = 400 KΩ
R2 = 200 KΩ
R3 = 600 KΩ

Note 1: The input impedance of the V_R pin is high, so it is necessary to take a proper measure against noise for short wiring and shielding wiring.

[When using the V_5 voltage regulating built-in resistor (Use of V_5 voltage regulating built-in resistor is set by command.)]
When the V_5 voltage regulating built-in resistor and the electronic volume function are used, the liquid crystal supply voltage V_5 can be controlled and the density of liquid crystal display can be controlled by commands only without adding any external resistor.
The V_5 voltage can be obtained by the following expression ② by adjusting resistors Ra and Rb within the range of $| V_5 | < | V_{OUT} |$.

$$V_5 = \left(1 + \frac{R_b}{R_a}\right) \cdot V_{EV} \quad \cdots\cdots ②$$

In this case, V_{EV} is determined by the constant-voltage source within the IC and by setting the electronic volume. When the electronic volume value is (00000), $V_{REG} \fallingdotseq 2.0$ V, being constant.



The voltage range of the V_5 output can be adjusted by changing the built-in resistor ratio (1 + Rb/Ra) by command. Reference values are shown in Table 5 and Fig. 2.

Table 5 V_5 voltage regulating built-in resistor ratio set values (reference values)

Command		(1 + Rb/Ra)
IR1	IR0	
0	0	2.81
0	1	3.27
1	0	3.72
1	1	4.21

V5 voltage by V5 voltage regulating built-in resistor ratio set value and electronic volume resistor value (reference value)
[Fig. 2]

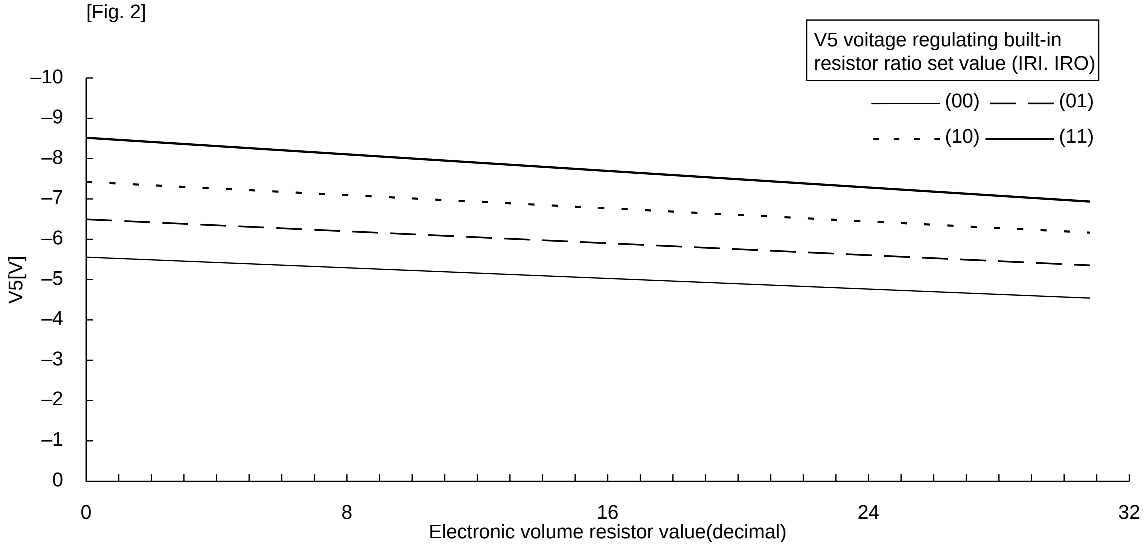
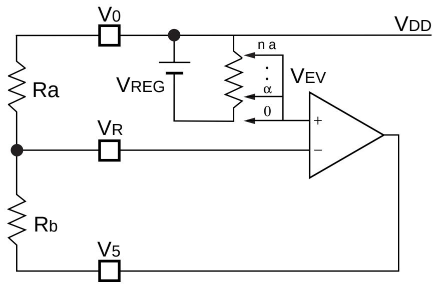


Fig. 2

• Voltage regulating circuit using the electronic volume function
When the electronic volume function is used, the liquid crystal drive voltage V_5 can be controlled by the command to adjust the density of liquid crystal display. Regarding this method, set 5-bit data in the electronic volume register, and the liquid crystal drive voltage V_5 can take one of 32 states of voltage value.
When the electronic volume function is used, the voltage regulating circuit must be turned on by the power control command.

[Constant setup example when using the electronic volume function]



$$V_5 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV}$$

However: $V_{EV} = V_{REG} - \alpha$

$\alpha = V_{REG} / 150$

Table 6

No.	Electronic volume register	α	V_5
0	(0, 0, 0, 0, 0)	0	Large
1	(0, 0, 0, 0, 1)	1α	•
2	(0, 0, 0, 1, 0)	2α	•
3	(0, 0, 0, 1, 1)	3α	•
•	•	•	•
•	•	•	•
30	(1, 1, 1, 1, 0)	n-1α	•
31	(1, 1, 1, 1, 1)	nα	Small

When the electronic volume function is not used, set the electronic volume register to (0,0,0,0,0).

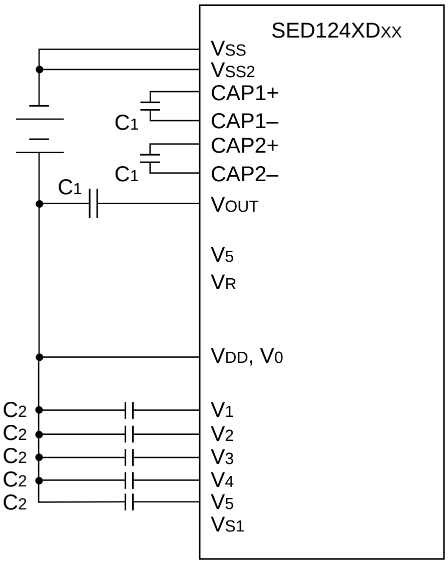
Liquid crystal voltage generating circuit

The V_5 potential is resistance-divided by the built-in resistor of the IC or external resistors Ra and Rb, generating potentials V_1, V_2, V_3, and V_4 required for liquid crystal drive. Furthermore, potentials V_1, V_2, V_3, and V_4 are impedance-converted by the voltage follower and supplied to the liquid crystal drive circuit.

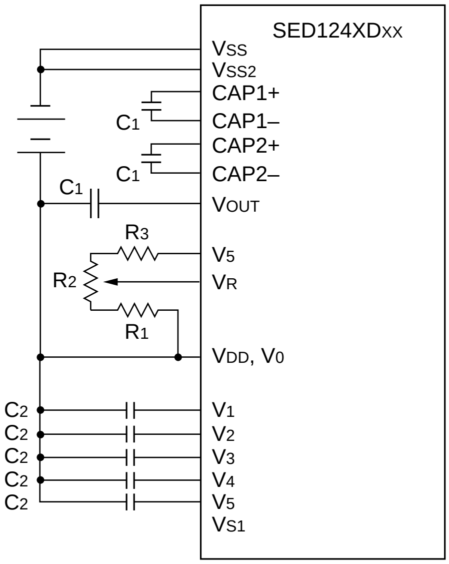
Regarding the liquid crystal drive voltage, the 1/5 bias or 1/4 bias can be selected by command. For liquid crystal power pins, capacitors C2 for voltage stabilization must be connected to pins V_1 to V_5 externally.
A reference circuit example of each case is shown below.

① Using all of the boosting circuit, power regulating circuit, and voltage follower

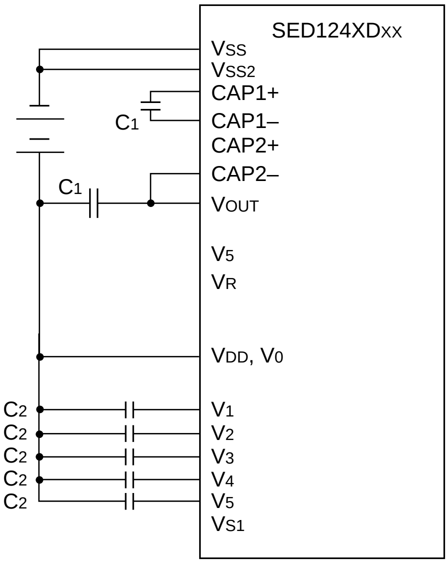
[When using a V_5 voltage regulating built-in resistor]
(Example of V_{SS2} = V_{SS}, triple boosting)



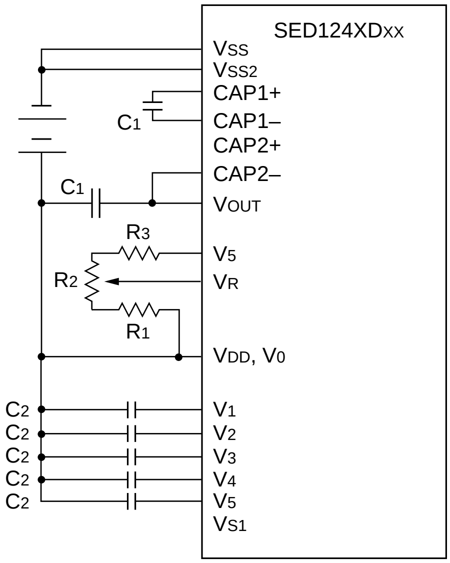
[When using no V_5 voltage regulating built-in resistor]
(Example of V_{SS2} = V_{SS}, triple boosting)



(Example of V_{SS2} = V_{SS}, double boosting)



(Example of V_{SS2} = V_{SS}, double boosting)

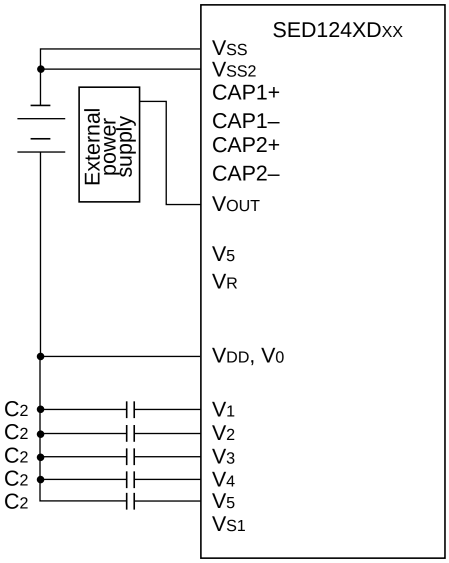


Reference set values: C_1: 0.47 to 4.7 μF
C_2: 0.1 to 4.7 μF

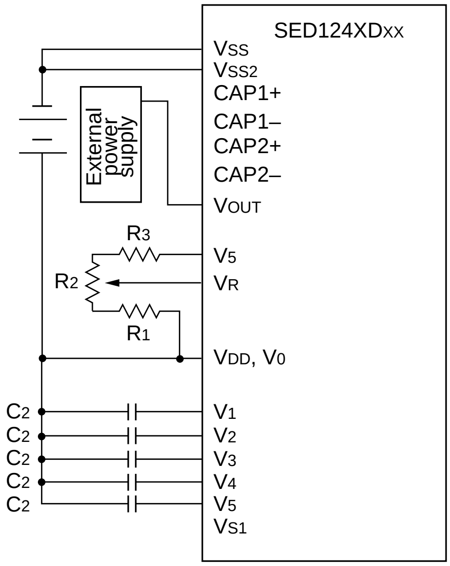
It is recommended to set optimum values suitable for the panel size in capacitors C_1 and C_2 while watching the liquid crystal display and drive waveforms.

② Using only the voltage regulating circuit and the voltage follower.

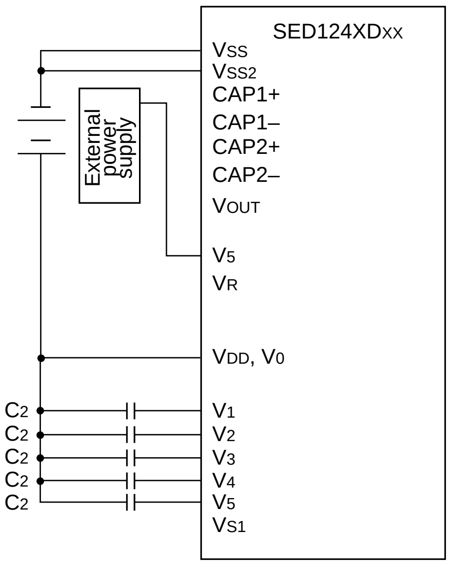
[When using a V_5 voltage regulating built-in resistor]
(Example of V_{SS2} = V_{SS})



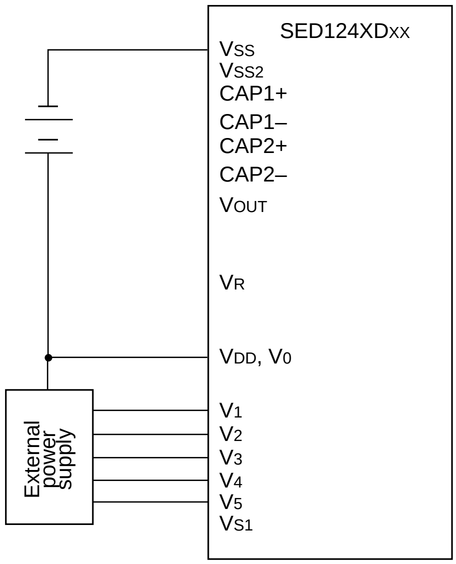
[When using no V_5 voltage regulating built-in resistor]
(Example of V_{SS2} = V_{SS})



(Example of V_{SS2} = V_{SS})



(Example of V_{SS2} = V_{SS})



Reference set values: C_1: 0.47 to 4.7 μF
C_2: 0.1 to 4.7 μF
It is recommended to set optimum values suitable for the panel size in capacitors C_1 and C_2 while watching the liquid crystal display and drive waveforms.

*1 Because the input impedance of the V_R pin is high, use a short wire and a shielding wire.

*2 Determine C_1 and C_2 values depending on the size of the LCD panel to be driven. Set proper values that permit stabilizing the liquid crystal drive voltages.

[Setting example]
- Turn on the voltage regulating circuit and the voltage follower and give a voltage to V_{OUT} from the outside.
- Display a LCD heavy load pattern like horizontal stripes and determine a C_2 value so that the liquid crystal drive voltages (V_1 to V_5) may be stabilized. However, it is necessary to set the same capacity value in C_2 in every case.
- Next, turn on the built-in power supply and determine a C_1 value.

High power mode

The power circuit built-in the SED1240 series is a low power consumption type. (when the high power mode is OFF)
Accordingly, in the case of a large load liquid crystal or panel, the display quality may be degraded. In this case, the display quality can be improved by entering HPM = '1' by command. Before determining whether or not to use this mode, it is recommended to make a display check with a real machine.
In case the display quality cannot be improved satisfactorily though the high power mode is set, a liquid crystal drive power must be supplied from the outside.

Low Power Consumption Mode

The SED1240 series is provided with the standby mode/ sleep mode to attain low power consumption in the standby status of the unit.

● Standby mode
The standby mode is turned on and off by the power save command and display off/booster circuit off command. Only static icons can be displayed.

1. Liquid crystal display output
   COM1 to COM32, COMS1, COMS2: VDD level
   SEG1 to SEG80: VDD level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Can be caused to come on by static drive.
   Control the static icon display by SEGSA, B, C, D, E, F, G, H, I, J, COMSA by the static icon RAM.
2. Contents of DDRAM, CGRAM, and symbol register
   The written contents are kept in memory regardless of the ON/OFF status of the standby mode.
3. The operation mode remains in the status provided before execution of the standby mode. The internal circuit for dynamic display output is stopped.
4. Oscillating circuit
   For static display, the oscillating circuit must be ON.

● Sleep mode
Turn off the power circuit and the oscillating circuit, set '0' in all the data of the static icon register, and execute the power save command.
Then, the sleep mode is set and the current consumption can be reduced to a value close to the static current.

1. Liquid crystal display output
   COM1 to COM32, COMS1, COMS2: VDD level
   SEG1 to SEG80, SEGS1, 2, 4, 5: VDD level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Set '0' in all the data of the static icon register and blink ON/OFF (for static icons).
2. Contents of SSRAM, CGRAM and symbol register
   The written contents can be kept in memory regardless of the ON/OFF status of the sleep mode.
3. The operation mode remains in the status provided before execution of the sleep mode. All the internal circuits are stopped.
4. Power circuit and oscillating circuit
   Turn off the built-in power supply and oscillating circuit by the power save command and the power control command.

* Caution: If the oscillating circuit is stopped with the static icon register data and blinking kept off, previous display will remain on the icon. To avoid this, be sure to turn off the data and blinking before stopping the oscillating circuit.

Reset Circuit

When the $\overline{RES}$ input becomes active, this LSI will be put into the initial setup status. Resetting is performed at the 'L' level of the $\overline{RES}$ input signal.

● Initial setup status

1. Line scroll register
   LS1, 0 = 0 : Scroll amount 0 line
2. Line blink control
   LB4 = 0 : DDRAM line 4 blink OFF
   LB3 = 0 : DDRAM line 3 blink OFF
   LB2 = 0 : DDRAM line 2 blink OFF
   LB1 = 0 : DDRAM line 1 blink OFF
3. Vertical double-size display register
   DD4 = 0 : Line 4 is displayed in standard form.
   DD3 = 0 : Line 3 is displayed in standard form.
   DD2 = 0 : Line 2 is displayed in standard form.
   DD1 = 0 : Line 1 is displayed in standard form.
4. Display ON/OFF register
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
   D = 0 : Display OFF
   RE = 0 : Extended register OFF
5. Power save register
   O = 0 : Oscillating circuit OFF
   PS = 0 : Power save OFF
6. Power control register
   HPM = 0 : High power mode OFF
   VC = 0 : Voltage regulating circuit OFF
   VF = 0 : Voltage follower OFF
   P = 0 : Boosting circuit OFF
   IRS = 1 : For built-in resistor
   BAS = 0 : 1/5 bias
   IR1,0 = 00 : Rb/Ra = small
7. System set register
   CG = 0 : CGRAM not used
   CS = 0 : Left shift
   SS = 0 : Normal display
   R1, 0 = 0 : Standard ROM + OPTION ROM1
8. Electronic volume
   (0,0,0,0,0)
9. Static icon ON/OFF control
   (SEGSA, B, C, D, E, F, G, H, I, J) =
   (0,0,0,0,0,0,0,0,0,0): Display OFF
10. Static icon blink control
    (SEGSA, B, C, D, E, F, G, H, I, J) =
    (0,0,0,0,0,0,0,0,0,0): Blink OFF

As seen in MPU Interface, the RES pin inputs data at the same timing as MPU resetting and performs initialization concurrently with the MPU. However, if this pin is put into the high impedance for a certain period after the MPU bus and ports are reset, perform a reset input after the input to the SED1240 series is definitively set.
For the reset signal, it is necessary to input '0' level

pulses at least for 10 μs as described in DC Characteristics. The ordinary operation will be started in 1 μs or more after the rising edge of the RES signal. When the RES pin becomes active, each register will be cleared and set to the above setup status.
If initialization is not executed by the RES pin when the supply voltage is applied, a clear disable status may appear.
In case the built-in liquid crystal power circuit is not used, the $\overline{RES}$ input must be active when the external liquid crystal power supply is turned on.

DESCRIPTION OF COMMANDS

Table 7 shows a command table. The SED1240 series identifies each data/command by a combination of A0 and $\overline{WR}$ (E).
An extended command can be selected by the RE bit in the command.
Interpreting and executing commands are performed only at the internal timing. This permits high-speed processing.

Overview of Commands

Table 7

Command type	Command name	RE	A0	$\overline{WR}$
Display control instructions	Cursor Home	0	0	0
	Display ON/OFF Control	0/1	0	0
	Line Blink Control	0	0	0
	Line Scroll Control	1	0	0
	Static Icon Display Control	0	1	0
	Static Icon Display Blink Control	0	1	0
	Vertical Double-size Display Control	1	0	0
Power control	Power Save	0/1	0	0
	Power Control (1)	0	0	0
	Power Control (2)	1	0	0
	Electronic Volume Control	0	1	0
System set	System Set (1)	0	0	0
	System Set (2)	1	0	0
Address control instructions	DDRAM, Symbol Register	0	0	0
	CGRAM	1	0	0
Data input instruction	Data Write	0/1	1	0

The execution time of each instruction is determined by the internal processing time of the SED1240 series. Accordingly, for executing an instruction, secure a time exceeding the cycle time (tcyc) and then execute the instruction.

Table 8 SED1240 Series Command Table

<table>
<tr><th rowspan="2">Command</th><th colspan="11">Code</th><th rowspan="2">Function</th></tr>
<tr><th>RE</th><th>A0</th><th>WR</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="2">(1) Cursor Home/ Line Scroll Control</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>*</td><td>*</td><td>*</td><td>*</td><td>Moves the cursor to the home position.
(Set the address to 30H.)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>*</td><td>*</td><td>LS1</td><td>LS0</td><td>Specifies the number of display scrolls in units of line.
<table><tr><th>LS1</th><th>LS0</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>Scroll amount 0 line</td></tr><tr><td>0</td><td>1</td><td>One-line upward scroll</td></tr><tr><td>1</td><td>0</td><td>Two-line upward scroll</td></tr><tr><td>1</td><td>1</td><td>Three-line upward scroll</td></tr></table></td></tr>
<tr><td rowspan="2">(2) Line Blink/ Vertical Double-size Display Control</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>LB4</td><td>LB3</td><td>LB2</td><td>LB1</td><td>Exerts blink control for each specified line.
LB4 = 1 (Blinks the display for line 4 of DDRAM in black-and-white reverse form.)
LB4 = 0 (Does not blink the display for line 4 of DDRAM.)
LB3 = 1 (Blinks the display for line 3 of DDRAM in black-and-white reverse form.)
LB3 = 0 (Does not blink the display for line 3 of DDRAM.)
LB2 = 1 (Blinks the display for line 2 of DDRAM in black-and-white-reverse form.)
LB2 = 0 (Does not blink the display for line 2 of DDRAM.)
LB1 = 1 (Blinks the display for line 1 of DDRAM in black-and-white reverse form.)
LB1 = 0 (Does not blink the display for line 1 of DDRAM.)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>DD4</td><td>DD3</td><td>DD2</td><td>DD1</td><td>Displays the specified DDRAM line in vertical double-size form.
DD4 = 1 (Displays the data for line 4 of DDRAM in vertical double-size form.)
DD4 = 0 (Displays the data for line 4 of DDRAM in standard form.)
DD3 = 1 (Displays the data for line 3 of DDRAM in vertical double-size form.)
DD3 = 0 (Displays the data for line 3 of DDRAM in standard form.)
DD2 = 1 (Displays the data for line 2 of DDRAM in vertical double-size form.)
DD2 = 0 (Displays the data for line 2 of DDRAM in standard form.)
DD1 = 1 (Displays the data for line 1 of DDRAM in vertical double-size form.)
DD1 = 0 (Displays the data for line 1 of DDRAM in standard form.)</td></tr>
</table>

<table>
<tr><th rowspan="2">Command</th><th colspan="11">Code</th><th rowspan="2">Function</th></tr>
<tr><th>RE</th><th>A0</th><th>WR</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>(3) Display ON/OFF/ Extended Register ON/OFF Control</td><td>0/1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>C</td><td>B</td><td>RE</td><td>D</td><td>Sets cursor ON/OFF, cursor blink ON/OFF (B), display ON/OFF (D), use/no-use of extended register (RE), and electronic volume LBS (RE).
C= 1 (cursor ON) C = 0 (cursor OFF)
B = 1 (blink ON) B = 0 (blink OFF)
D = 1 (display ON) D = 0 (display OFF)
RE = 1 (extended register ON) RE = 0 (extended register OFF)</td></tr>
<tr><td>(4) Power Save Control</td><td>0/1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>*</td><td>*</td><td>0</td><td>PS</td><td>Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (O).
PS = 1 (power save ON) PS = 0 (power save OFF)
O = 1 (oscillation ON) O = 0 (oscillation OFF)</td></tr>
<tr><td rowspan="2">(5) Power Control</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>HPM</td><td>VC</td><td>VF</td><td>P</td><td>Sets high power mode ON/OFF (HPM), voltage regulating circuit ON/OFF (VC), voltage follower ON/OFF (VF), and boosting circuit ON/OFF (P).
HPM = 1 (high power mode ON) HPM = 0 (high power mode OFF)
VC = 1 (voltage regulating circuit ON) VC = 0 (voltage regulating circuit OFF)
VF = 1 (voltage follower ON) VF = 0 (voltage follower OFF)
P = 1 (boosting circuit ON) P = 0 (boosting circuit OFF)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>IRS</td><td>BAS</td><td>IR1</td><td>IR0</td><td>Sets V_5 voltage regulating resistor selection (IRS), LCD bias set (BAS), and V_5 voltage regulating built-in resistor ratio set (IR1, IR0).
IRS = 1 (use of built-in resistor) IRS = 0 (no use of built-in resistor)
BAS = 1 (1/4 bias) BAS = 0 (1/5 bias)
(IR1, IR0) = (11, 10, 01, 00) ... (Rb/Ra ratio large to small)</td></tr>
<tr><td rowspan="2">(6) System Set</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>R1</td><td>R0</td><td>CS</td><td>CG</td><td>Sets ROM option (R1, R0), use/no use of CGRAM (CG), and COM shift direction (CS)
CG = 1 (use of CGRAM) CG = 0 (no use of CGRAM)
CS = 1 (right shift) CS = 0 (left shift)
<table><tr><th>R1</th><th>R0</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>Standard ROM + OPTION ROM1</td></tr><tr><td>0</td><td>1</td><td>Standard ROM + OPTION ROM2</td></tr><tr><td>1</td><td>0</td><td>Standard ROM + OPTION ROM3</td></tr><tr><td>1</td><td>1</td><td>Standard ROM + OPTION ROM4</td></tr></table></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>*</td><td>*</td><td>SS</td><td>*</td><td>Sets the normal/reverse display (SS) of each segment character.
SS = 1 (reverse) SS = 0 (normal)</td></tr>
<tr><td rowspan="2">(7) RAM Address Set</td><td>0</td><td>0</td><td>0</td><td>1</td><td colspan="7">ADDRESS</td><td>Sets the address of DDRAM, static icon RAM or electronic volume RAM.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td colspan="7">ADDRESS</td><td>Sets the address of CGRAM or symbol register RAM.</td></tr>
</table>

Command	Code											Function
	RE	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(8) RAM Data Write	0/1	1	0	DATA								Writes data into the DDRAM, CGRAM, symbol register RAM, static icon RAM or electronic volume RAM. This is determined by the address set instruction executed immediately before writing data.
(9) NOP	0/1	0	0	0	0	0	0	0	0	0	0	A command for NON-OPERATION. This also serves as a test mode clear command, so it is recommended to input it periodically.
(10) Test Mode	0/1	0	0	0	0	0	0	*	*	*	*	A command for IC chip test. Don’t use this command.

Description of Command Functions

Cursor home

Function: Presets the address counter to 30H. Only when the previous RAM access is made to the area of RE = 0 of the RAM map, the cursor is moved to digit 1 on line 1 if the cursor is displayed.
If line scroll is set, it is cleared to the scroll amount = 0 line.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	*	*	*	*

* : Don't Care

Line scroll control

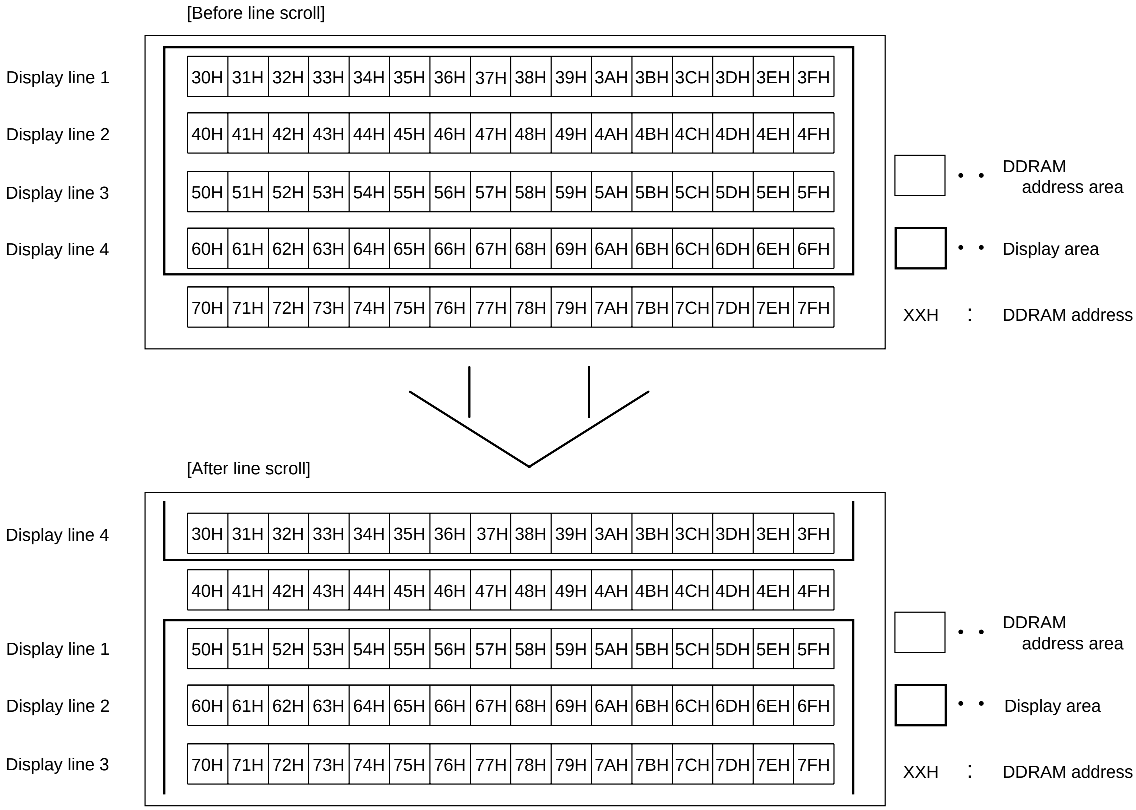
Function: Controls the display scroll amount for each line.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	*	*	LS1	LS0

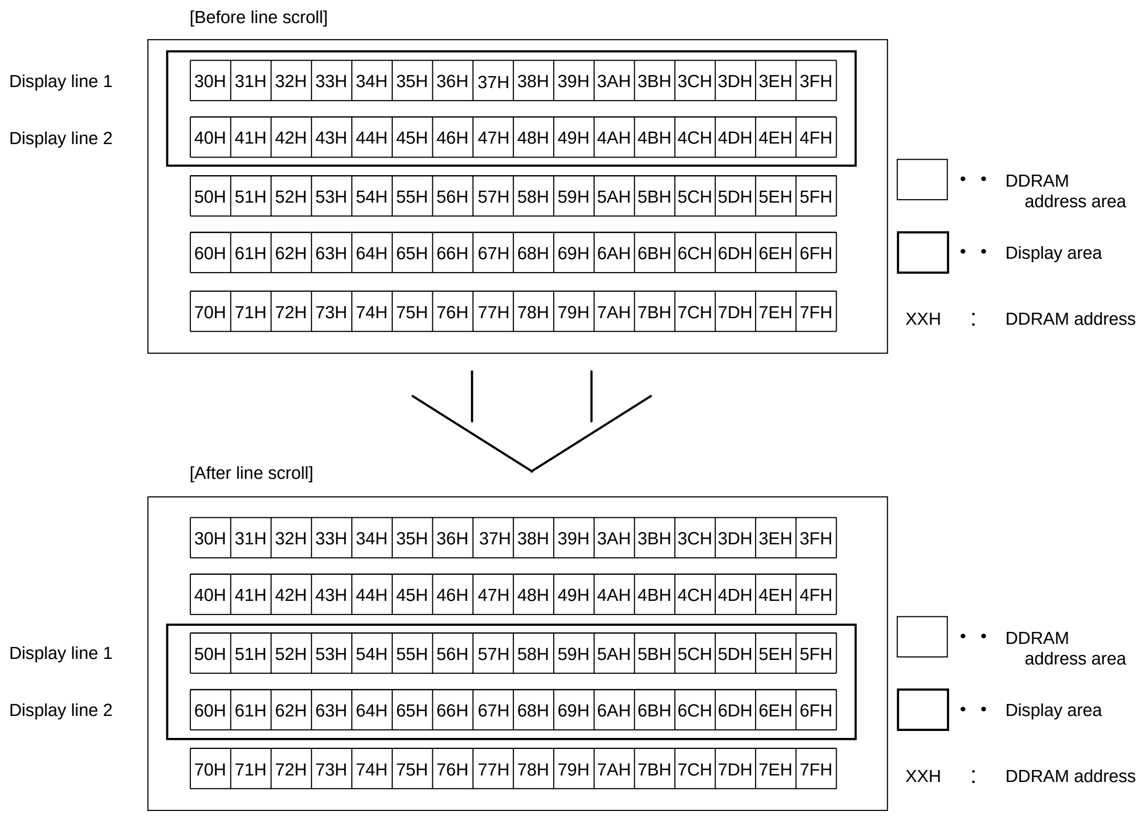
* : Don't Care

LS1	LS0	Function
0	0	Scroll amount 0 line
0	1	Scrolls 1 line upward. (display line 1 from DDRAM line 2)
1	0	Scrolls 2 lines upward. (display line 1 from DDRAM line 3)
1	1	Scrolls 3 lines upward. (display line 1 from DDRAM line 4)

• When 2-line scroll has been performed upward at the 4-line display



- When 2-line scroll has been performed upward at the 2-line display [(LS1, LS2) = (1, 0)]



Line blink display control

Function: Displays the specified line in back-and-while reverse form.
The specified line corresponds to the address line of the DDRAM.
(Not the display line)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	LB4	LB3	LB2	LB1

- Displays the specified line of the DDRAM in black-and-white form by setting LB4 to LB1.
  - LB4 = 0 : Displays the data for line 4 of the DDRAM in standard form. (no blink) [DDRAM 60H to 6FH]
  - LB4 = 1 : Displays the data for line 4 of DDRAM in black-and-white reverse blink form. [DDRAM 60H to 6FH]
  - LB3 = 0 : Displays the data for line 3 of the DDRAM in standard form. (no blink) [DDRAM 50H to 5FH]
  - LB3 = 1 : Displays the data for line 3 of the DDRAM in black-and-white reverse blink form. [DDRAM 50H to 5FH]
  - LB2 = 0 : Displays the data for line 2 of the DDRAM in standard form. (no blink) [DDRAM 40H to 4FH]
  - LB2 = 1 : Displays the data for line 2 of the DDRAM in black-and-white reverse blink form. [DDRAM 40H to 4FH]
  - LB1 = 0 : Displays the data for line 1 of the DDRAM in standard form. (no blink) [DDRAM 30H to 3FH]
  - LB1 = 1 : Displays the data for line 1 of the DDRAM in black-and-white reverse blink form. [DDRAM 30H to 3FH]
- f_{BLINK} = 1 to 2Hz.
- Blinking is performed at the same frequency as cursor blink.
  If blinking is caused to occur at the same time, the cursor position will be hard to know.

SED1240 Series

Vertical double-size display control

Function: Displays the specified line in vertical double-size form.
The specified line corresponds to the address of the DDRAM.
(Not the display line)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	DD4	DD3	DD2	DD1

- Displays the specified line of the DDRAM in vertical double-size form by setting DD4 to DD1.

DD4 = 0 : Displays the data for line 4 of the DDRAM in standard form. [DDRAM 60H to 6FH]

DD4 = 1 : Displays the data for line 4 of the DDRAM in vertical double-size form. [DDRAM 60H to 6FH]

DD3 = 0 : Displays the data for line 3 of the DDRAM in standard form. [DDRAM 50H to 5FH]

DD3 = 1 : Displays the data for line 3 of the DDRAM in vertical double-size form. [DDRAM 50H to 5FH]

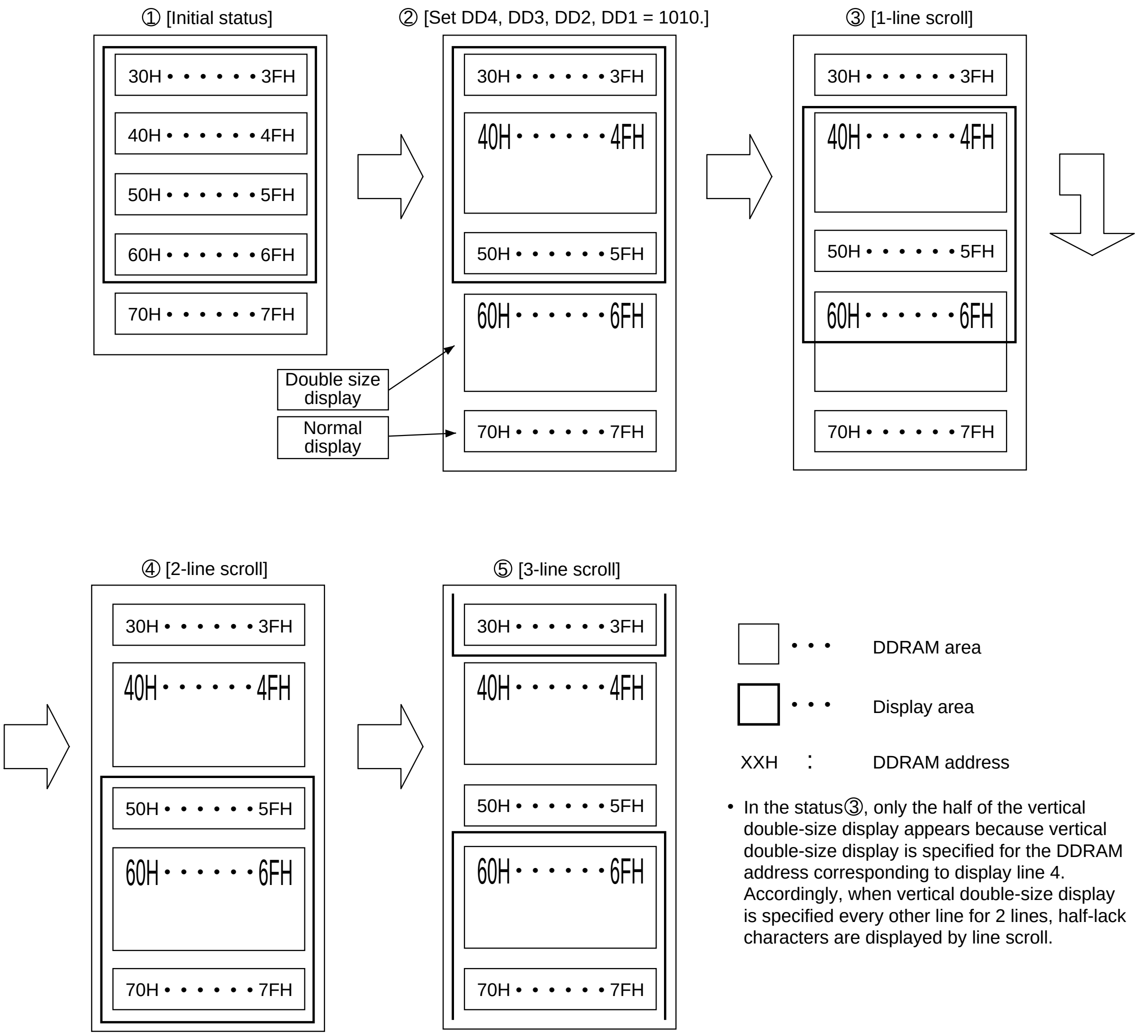
DD2 = 0 : Displays the data for line 2 of the DDRAM in standard form. [DDRAM 40H to 4FH]

DD2 = 1 : Displays the data for line 2 of the DDRAM in vertical double-size form. [DDRAM 40H to 3FH]

DD1 = 0 : Displays the data for line 1 of the DDRAM in standard form. [DDRAM 30H to 3FH]

DD1 = 1 : Displays the data for line 1 of the DDRAM in vertical double-size form. [DDRAM 30H to 3FH]

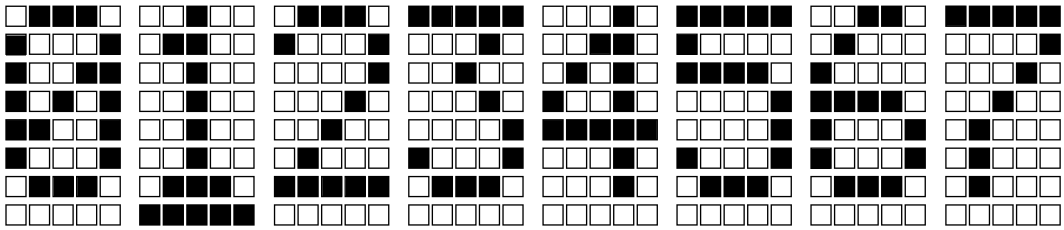
• Example of vertical double-size display
An example of 4-line display will be cited for explanation.

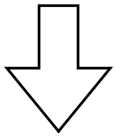


• In the status③, only the half of the vertical double-size display appears because vertical double-size display is specified for the DDRAM address corresponding to display line 4. Accordingly, when vertical double-size display is specified every other line for 2 lines, half-lack characters are displayed by line scroll.

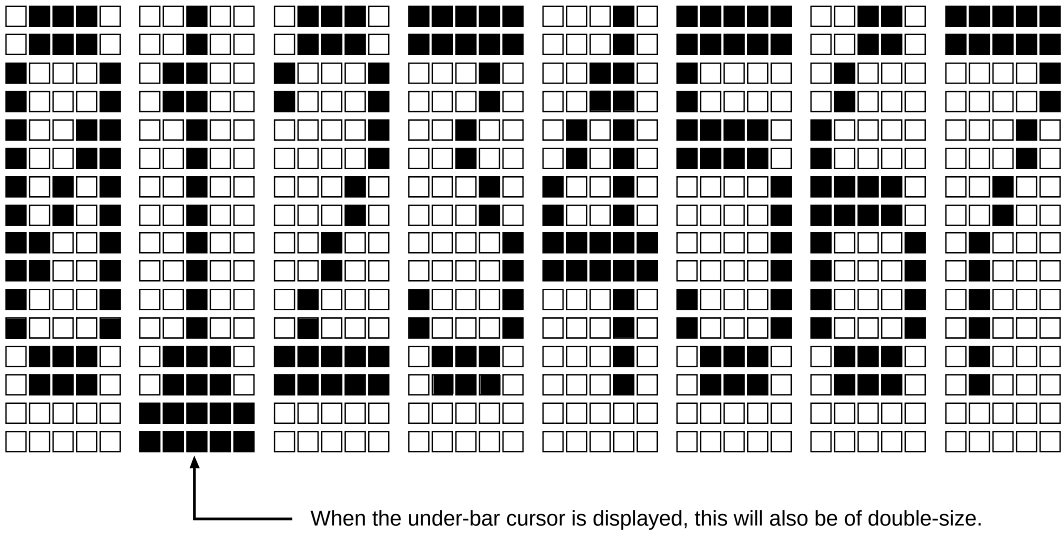
• Example of vertical double-size display (characters)

[Standard display]





[Vertical double-size display]



When the under-bar cursor is displayed, this will also be of double-size.

Display ON/OFF control

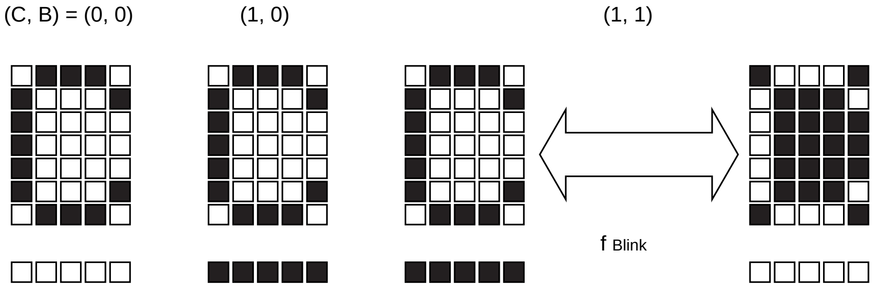
Function: Sets both display and cursor ON/OFF, and extended register access.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	1	1	C	B	RE	D

- Display ON/OFF is specified by setting D.
  - D = 0 : Display ON
  - D = 1 : Display ON
- Character blink ON/OFF at the cursor position is specified by setting B. However, when the cursor is OFF, this bit is invalidated.
  - B = 0 : Cursor blink OFF
  - B = 1 : Cursor blink ON
- Cursor ON/OFF is specified by setting C.
  - C = 0 : No display of cursor
  - C = 1 : Display of cursor
- Extended register access is specified by setting RE.
  - RE = 0 : Extended register OFF
  - RE = 1 : Extended register ON
- The relation between C/B register and cursor display is shown in the following table.

C	B	Cursor display
0	0	No display (fixed)
0	1	No display (fixed)
1	0	Display of under-bar cursor
1	1	Alternate display of display characters and black-and-white reversed display characters

- Example of cursor display



The cursor display position is indicated by the address counter. Accordingly, when moving the cursor, change the address counter value by the RAM address set command or the auto increment by the RAM data write command.
To display the under-bar cursor when character data (CGRAM) at the cursor position, the position corresponding to the cursor position will be displayed in black-and-white reverse form.
If the address counter is set to the symbol register position at (C, B) = (1, 1), symbols can be caused to blink selectively (every 5 dots because symbols correspond to characters).

Power save

Function: Controls the oscillating circuit and sets and resets the power save mode and the sleep mode.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	1	0	0	*	*	O	PS

∗ : Don't Care

- Power save mode ON/OFF is specified by setting PS.
  - PS = 0 : Power save OFF (reset)
  - PS = 1 : Power save ON (set)
- Oscillating circuit ON/OFF is specified by setting O.
  - O = 0 : Oscillating circuit OFF (stop of oscillation)
  - O = 1 : Oscillating circuit ON (start of oscillation)

Power control (1)

Function: Controls the operation of the built-in power circuit.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	HPM	VC	VF	P

∗ : Don't Care

- Boosting circuit ON/OFF is specified by setting P. For operating the boosting circuit, the oscillating circuit must be in operation.
  P = 0 : Boosting circuit OFF
  P = 1 : Boosting circuit ON
- Voltage follower ON/OFF is specified by setting VF.
  VF = 0 : Voltage follower OFF
  VF = 1 : Voltage follower ON
- Voltage regulating circuit ON/OFF is specified by setting VC.
  VC = 0 : Voltage regulating circuit OFF
  VC = 1 : Voltage regulating circuit ON.
- High power mode ON/OFF is specified by setting HPM.
  HPM = 0 : High power mode OFF
  HPM = 1 : High power mode ON

Power control (2)

Function: Controls the operation of the built-in power circuit.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	IRS	BAS	IR1	IR0

∗ : Don't Care

- The relation of IR0 and option combinations is shown in the following table.

IR1	IR0	(1 + Rb/Ra)
0	0	Small
0	1	↓
1	0	
1	1	Large

- Bias selection is performed by setting BAS.
  BAS = 0 : 1/5 bias
  BAS = 1 : 1/4 bias
- Either built-in V5 voltage regulating resistor or external resistor (no use of built-in resistor) is selected by setting IRS.
  IRS = 0 : No use of built-in resistor
  IRS = 1 : Use of built-in resistor

System set (1)

Function: Selects an option ROM and sets the common shift direction and the use/no use of CGRAM.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	R1	R0	CS	CG

- The relation of R1 and R0 combinations is shown in the following figure.

R1	R0	ROM combination
0	0	Standard ROM (160 characters or 154 characters) + option ROM1 (96 characters)
0	1	Standard ROM (160 characters or 154 characters) + option ROM2 (96 characters)
1	0	Standard ROM (160 characters or 154 characters) + option ROM3 (96 characters)
1	1	Standard ROM (160 characters or 154 characters) + option ROM4 (96 characters)

- The COM shift direction is specified by setting CS.
  CS = 0 : COM left shift (COM1 → COM32 → COMS1 → COMS2)
  CS = 1 : COM right shift (COM32 → COM1 → COMS1 → COMS2)
- The use/no use of CGRAM is specified by setting CG.
  CG = 0 : No use of CGRAM
  CG = 1 : Use of CGRAM

System set (1)

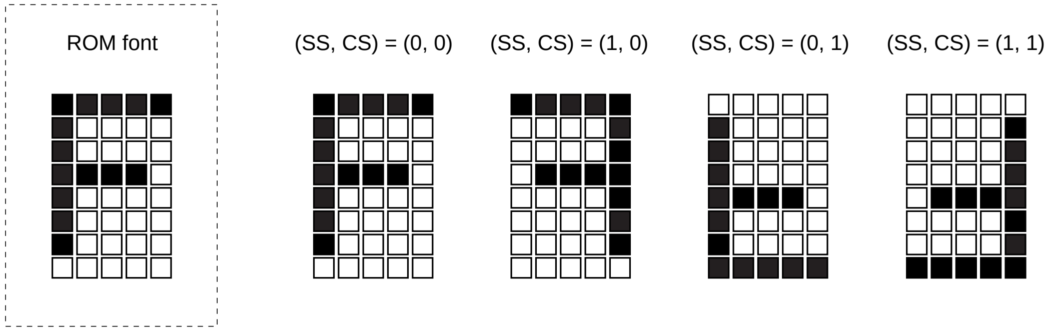
Function: sets the normal/reverse display of SEG characters.
This function operates for each character.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	0	*	*	SS	*

∗ : Don't Care

- The normal/reverse display of SEG is specified by setting SS.
  SS = 0 : Normal display of SEG
  SS = 1 : Reverse display of SEG
- For the symbol register RAM output, only the normal display is available.

- Example of display (compared by the same mounting method)



RAM address set (1) [DDRAM, static icon RAM, electronic volume RAM]

Function: Sets the address for writing data into the DDRAM, static icon RAM (including blink control), and electronic volume RAM in the address counter. When the cursor appears, it is displayed at the display position corresponding to the DDRAM address set by this command. (When the static icon RAM or electronic volume RAM is specified, the cursor disappears on the display.)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	ADDRESS						

① The settable address is the address 00H to 7FH in D6 to D0.
② When writing data in the RAM, set the address for writing data by this command. Next, when data is written in succession, the address will be automatically incremented. (00H to 7FH → 00H)
③ RE = 0, 09H is for testing. Be sure not to use it!

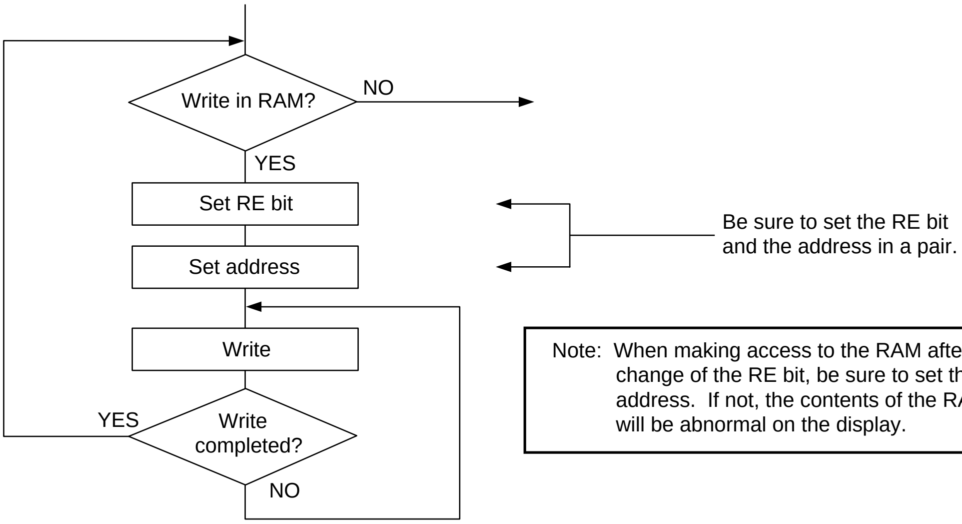
RAM address set (2) [CGRAM, symbol register RAM]

Function: Sets the address for writing data into the CGRAM or symbol register RAM in the address counter.
When the CGRAM address is set, the cursor will disappear on the display. When the symbol register RAM is set, the cursor moves to the corresponding symbol position, causing this symbol to blink selectively.
When the cursor home command is executed immediately after execution of this instruction (before execution of RAM Address Set (1)), the cursor will not be displayed. (Because the address is set at address 30H of RE-1 of the RAM map.)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	ADDRESS						

① The settable address of the address of 00H to 7FH in D6 to D0.
② When writing data in the RAM, set the address for writing data by this command. Next, if data is written in succession, the address will be automatically incremented. (00H to 7FH → 00H)
③ RE = 1, 30H - 5FH i8s set to No Use. It is not available.

<Example of Address Set>



Note: When making access to the RAM after a change of the RE bit, be sure to set the address. If not, the contents of the RAM will be abnormal on the display.

[SED1240 RAM map] (4-line 16-digit display)

RE	Low order / High order	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0XH	SI		SIB		Unused				EV	TEST	Unused					
	1XH	Unused															
	2XH	Unused															
	3XH	DDRAM line 1															
	4XH	DDRAM line 2															
	5XH	DDRAM line 3															
	6XH	DDRAM line 4															
	7XH	DDRAM line 5															
1	0XH	CGROM(00H)								CGROM(01H)							
	1XH	CGROM(02H)								CGROM(03H)							
	2XH	CGROM(04H)								CGROM(05H)							
	3XH	Unused															
	4XH	Unused															
	5XH	Unused															
	6XH	Symbol register															
	7XH	Symbol register															

Symbol register:
COMS1, 2

For static icon:
COMSA, SEGSA - J

SI : Static icon RAM
SIB : Static icon blink control RAM
EV : Electronic volume RAM
TEST : Testing register. Don't use it.

[SED1240 Series RAM map] (2-line 16-digit display)

RE	High order \ Low order	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0XH	SI		SIB		Unused				EV	TEST	Unused					
	1XH	Unused															
	2XH	Unused															
	3XH	DDRAM line 1															
	4XH	DDRAM line 2															
	5XH	DDRAM line 3															
	6XH	DDRAM line 4															
	7XH	DDRAM line 5															
1	0XH	CGROM(00H)								CGROM(01H)							
	1XH	CGROM(02H)								CGROM(03H)							
	2XH	CGROM(04H)								CGROM(05H)							
	3XH	Unused															
	4XH	Unused															
	5XH	Unused															
	6XH	Symbol register															
	7XH	Symbol register															

Symbol register:
COMS1, 2

For static icon:
COMSA, SEGSA - J

SI : Static icon RAM
SIB : Static icon blink control RAM
EV : Electronic volume RAM
TEST : Testing register. Don't use it.

[Display range of each master]

The following shows the display range for the DDRAM area when the vertical double size is unspecified and scroll amount is 0 line:

SED1240 (4 lines by 16 columns)	1st line on display	RE = 0	30H to 3FH
	2nd line on display	RE = 0	40H to 4FH
	3rd line on display	RE = 0	50H to 5FH
	4th line on display	RE = 0	60H to 6FH
SED1241 (3 lines by 16 columns)	1st line on display	RE = 0	30H to 3FH
	2nd line on display	RE = 0	40H to 4FH
	3rd line on display	RE = 0	50H to 5FH
SED1242 (2 lines by 16 columns)	1st line on display	RE = 0	30H to 3FH
	2nd line on display	RE = 0	40H to 4FH

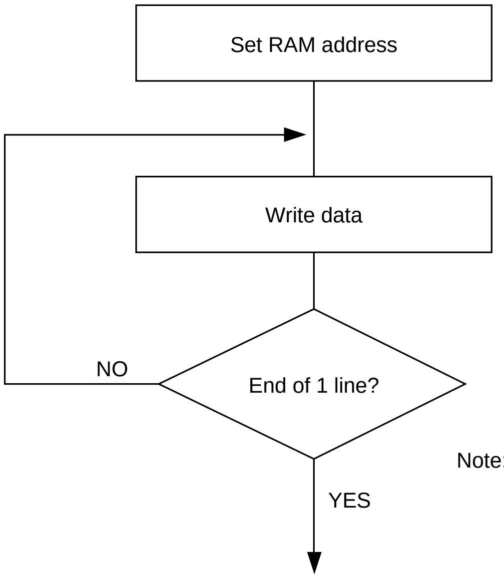
RAM data write

Function: Writes data in the RAM areas of the DDRAM, CGRAM, symbol register RAM, static icon RAM, and electronic volume RAM.
Before this command, be sure to execute the address set command.
After that, each time data is written, the address will be automatically incremented. (Regarding the RE bit, the contents set by the command will be kept in memory.)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	1	0	DATA							

① Data is written into the DDRAM, CGRAM, symbol register RAM, static icon RAM, or electronic volume RAM.
② The address counter is automatically incremented by 1, so data can be written in succession. However, the address counter advances from 00H to 7FH to 00H. Accordingly, when writing data into the CGRAM, take care not to write it at the addresses subsequent to 30H.

<Data write example>
An example of writing one line of data into the DDRAM continuously is shown below.



Note: Before executing instructions in succession, secure a time exceeding t_{CYC} and then execute them.

NOP

Function: A no-operation command. No operation is performed functionally. However, because a test mode reset function exists inside, the test mode can be reset if the IC is put into this mode by an effect of noise.
It is recommended to add this command at each breakpoint of the program.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	0	0	0	0	0	0

Test mode

Function: An IC test mode set command. Don't use it in any case.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	0	0	*	*	*	*

CHARACTER GENERATOR

Character Generator ROM (CGROM)

The SED1240 series is provided with a character generator ROM consisting of up to 544 types of characters. Each character size is of a structure of 5×8 dots.
A character code table of the SED1240 series is shown in CGROM Table X to X. In this case, which of CGROM and CGRAM should be used for the 6 characters of 00H to 05H of the character code is specified by the system set command.

The CGROM of the SED1240 series is a mask ROM and is compatible with the user's own CGROM. Please ask our sales department for further information.
Regarding a changed product of CGROM, the product name is defined as follows:

Example: SED1240D<u>AB</u>
↑
Digits corresponding to CGROM pattern change

The following shows the standard font specified for SED1240 series:

SED1240DAB, SED1240T0A: JISS1 (Font A)
SED1240DBB, SED1240T0B : ASCII (Font B)
SED1240DGB, SED1240T0G: JISS2 (Font G)

SED1241DAB, SED1241T0A: JISS1 (Font A)
SED1241DBB, SED1241T0B : ASCII (Font B)
SED1241DGB, SED1241T0G: JISS2 (Font G)

SED1242DAB, SED1242T0A: JISS1 (Font A)
SED1242DBB, SED1242T0B : ASCII (Font B)
SED1242DGB, SED1242T0G: JISS2 (Font G)

[SED1240D0A CGROM Font]

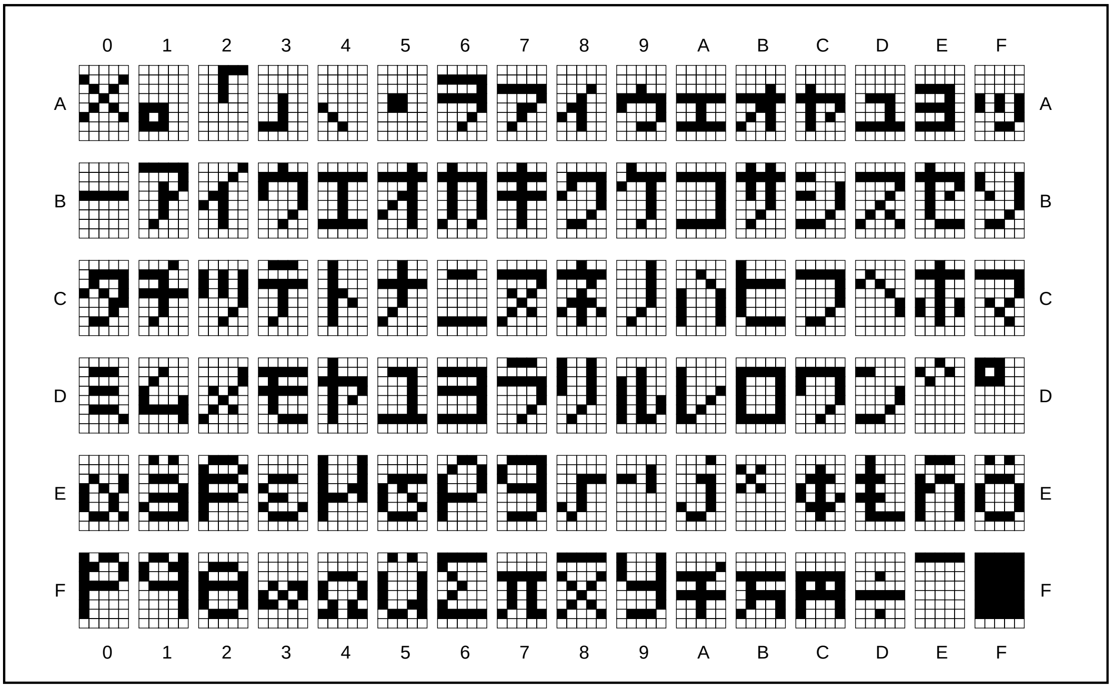
Standard ROM Font



OPTION ROM1 (when R1, R0 = 0, 0 is selected)

Lower 4 Bit of Code

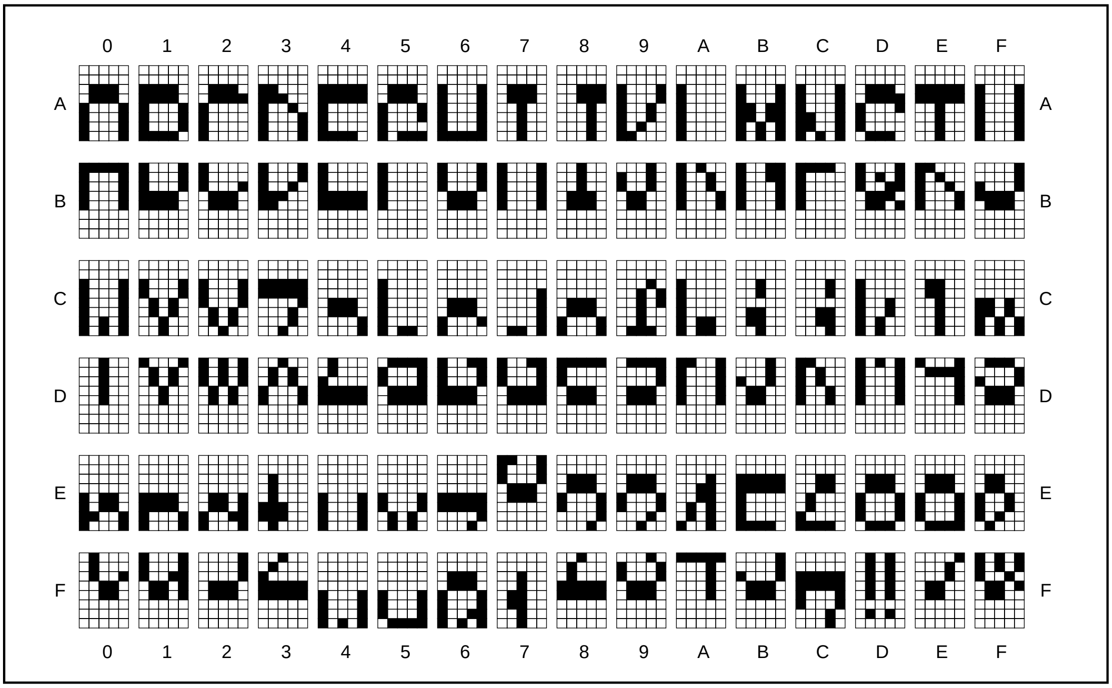
Higher 4 Bit of Code



OPTION ROM2 (when R1, R0 = 0, 1 is selected)

Lower 4 Bit of Code

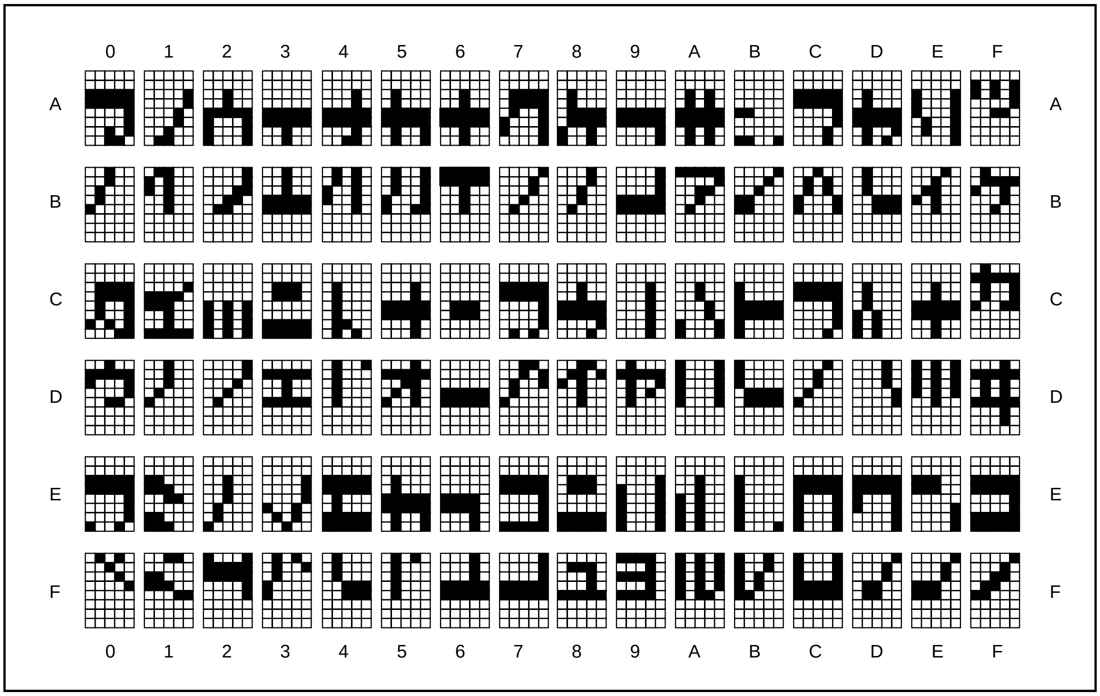
Higher 4 Bit of Code



OPTION ROM3 (when R1, R0 = 1, 0 is selected)

Lower 4 Bit of Code

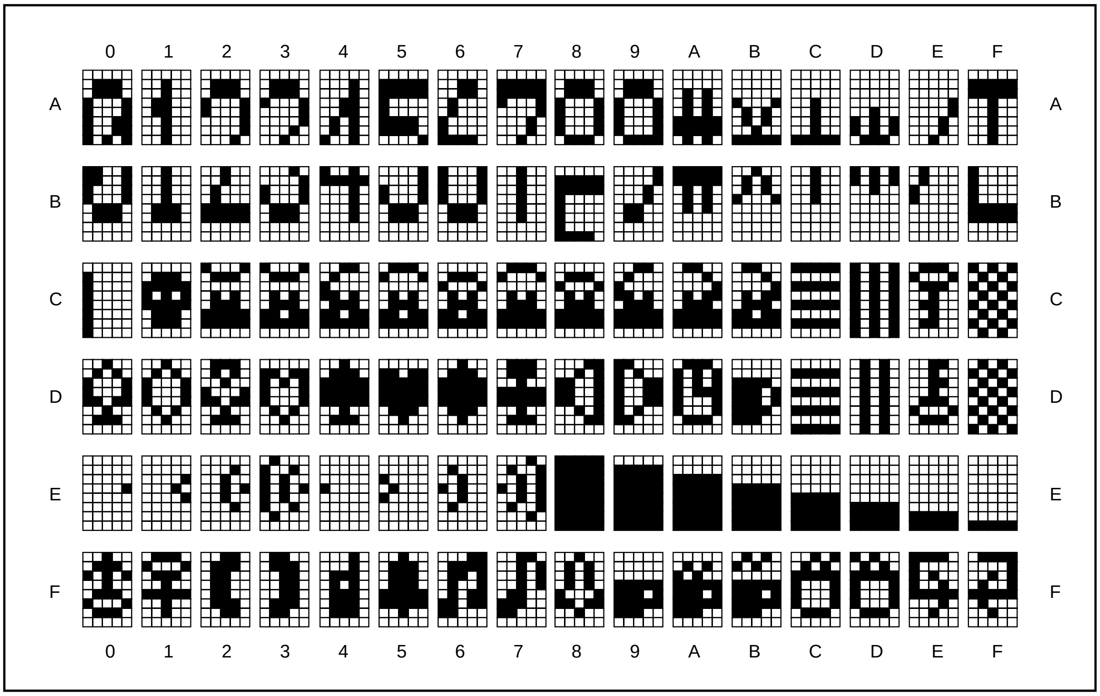
Higher 4 Bit of Code



OPTION ROM4 (R1, R0 = 1,1 is selected)

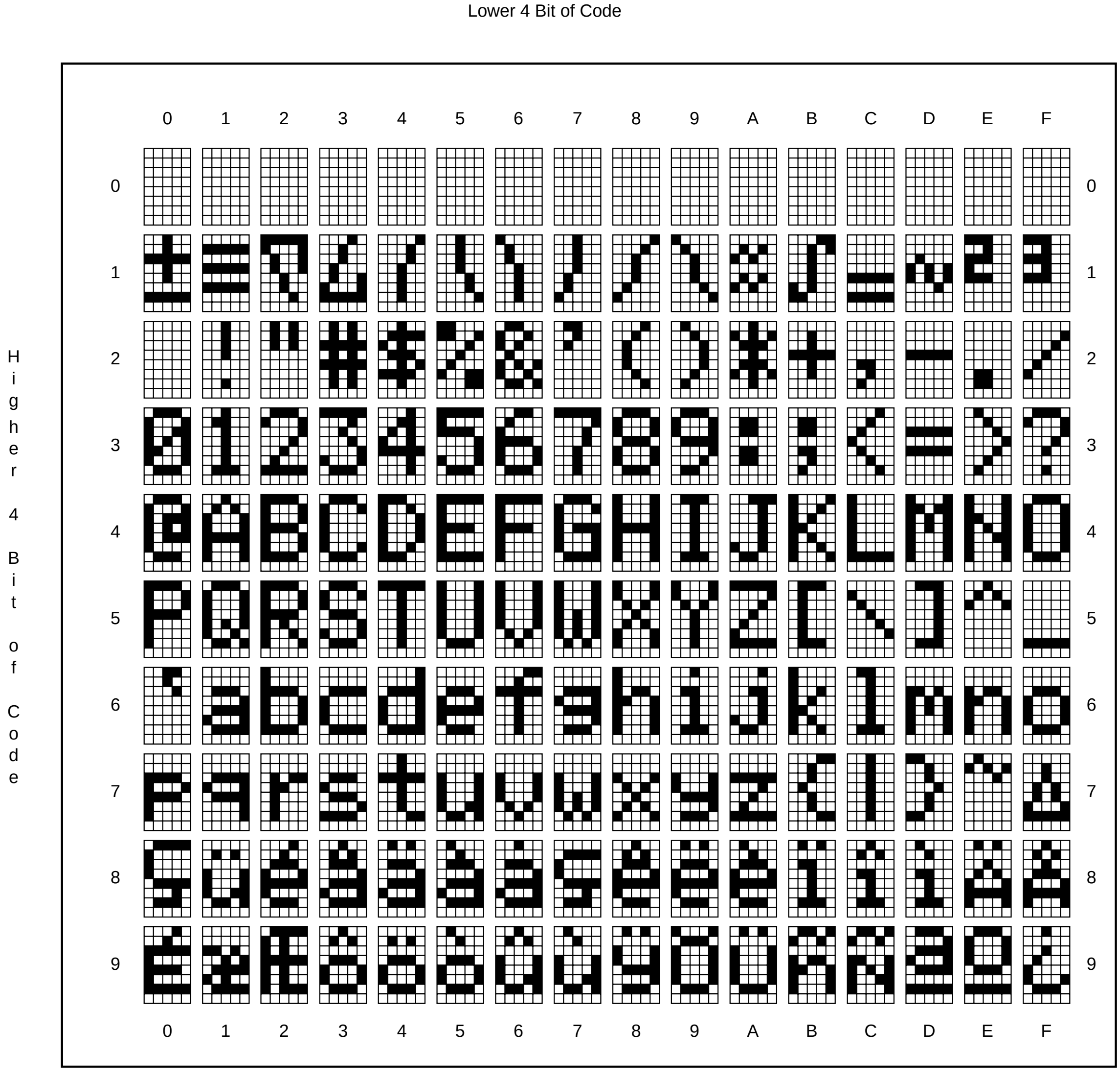
Lower 4 Bit of Code

Higher 4 Bit of Code



[CGROM Font (ASCII: Font B)]

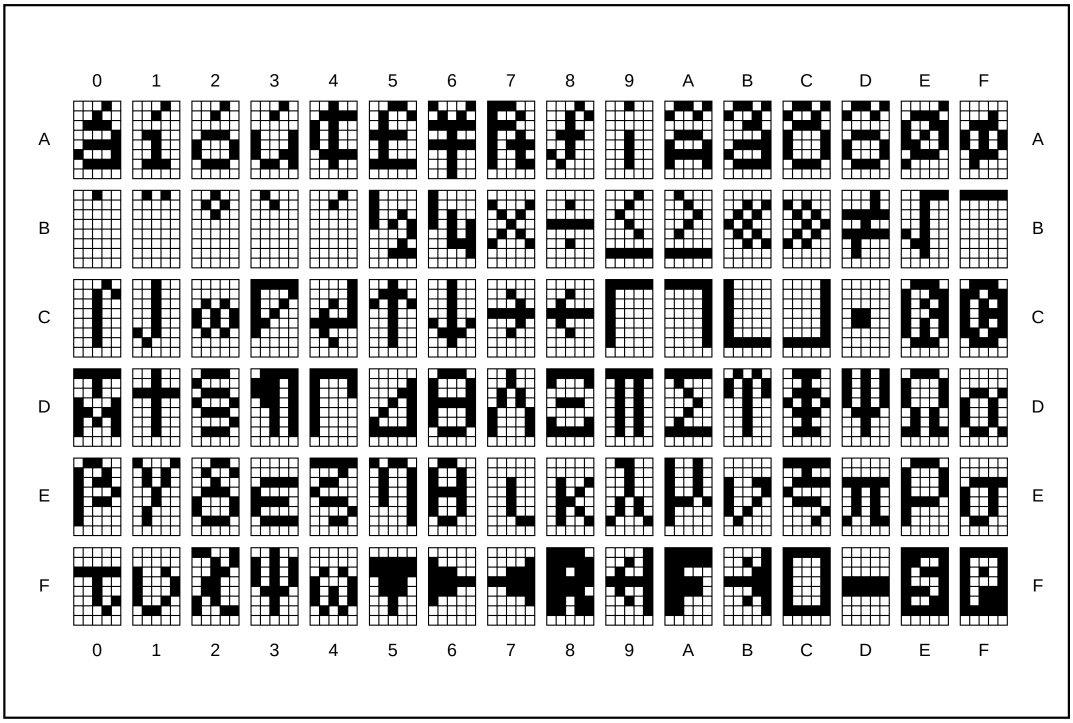
Standard ROM Font



OPTION ROM1 (when R1, R0 = 0, 0 is selected)

Lower 4 Bit of Code

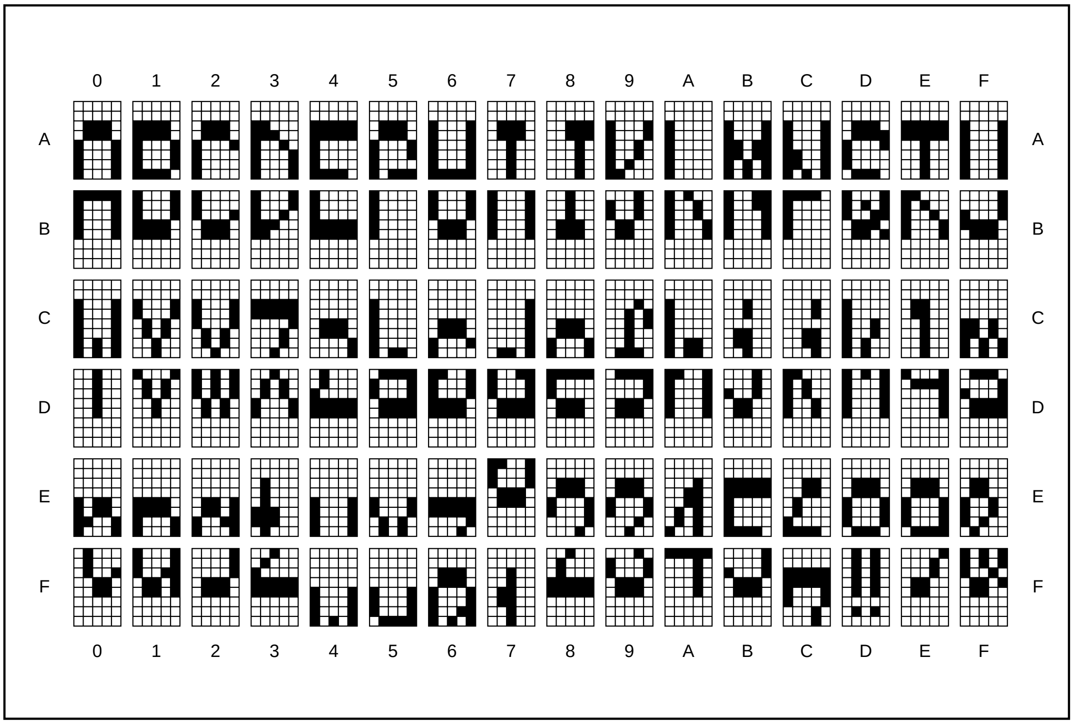
Higher 4 Bit of Code



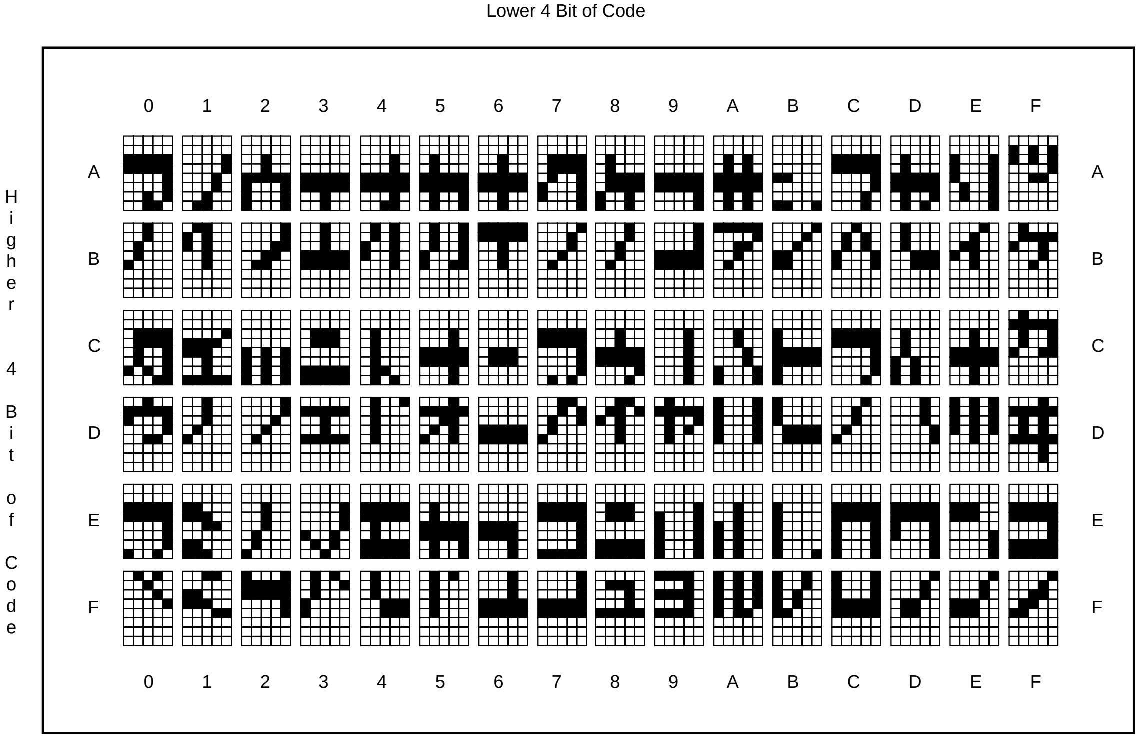
OPTION ROM2 (when R1, R0 = 0, 1 is selected)

Lower 4 Bit of Code

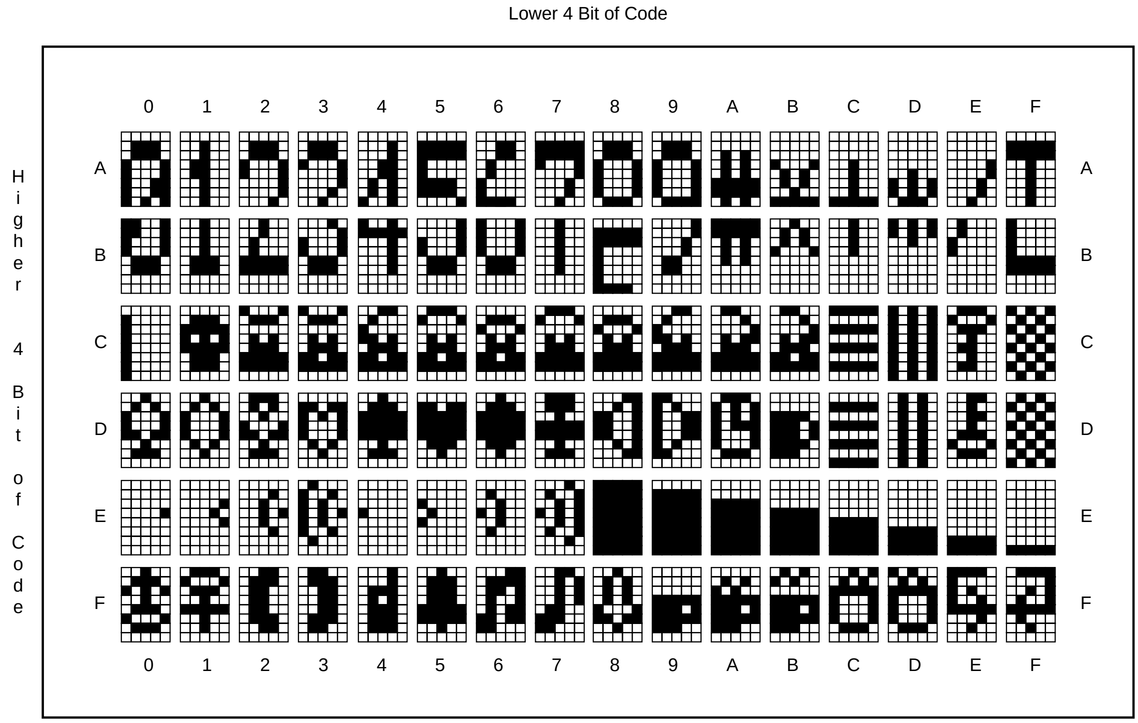
Higher 4 Bit of Code



OPTION ROM3 (when R1, R0 = 1, 0 is selected)

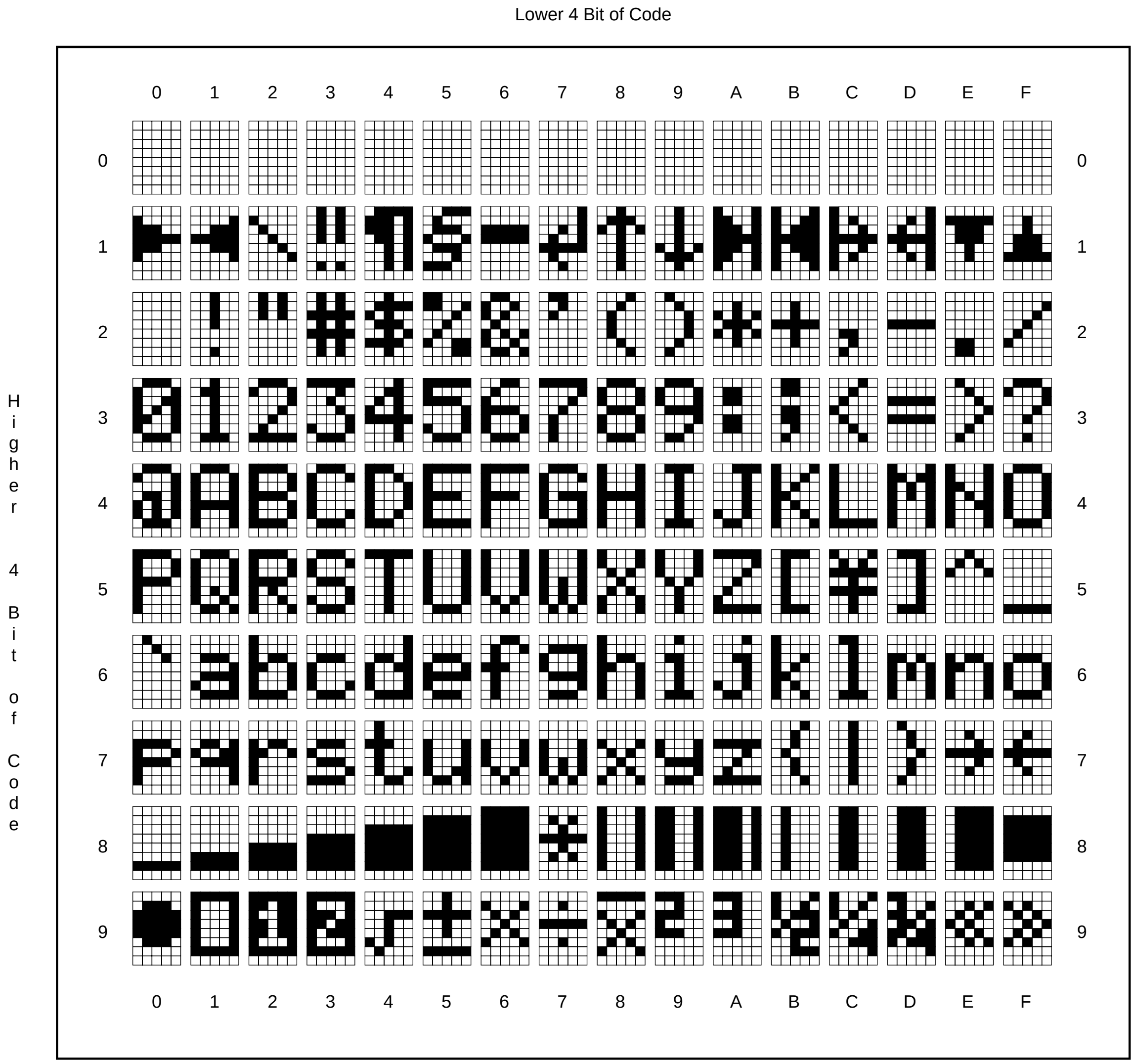


OPTION ROM4 (R1, R0 = 1,1 is selected)



[CGROM Font (JISS2: Font G)]

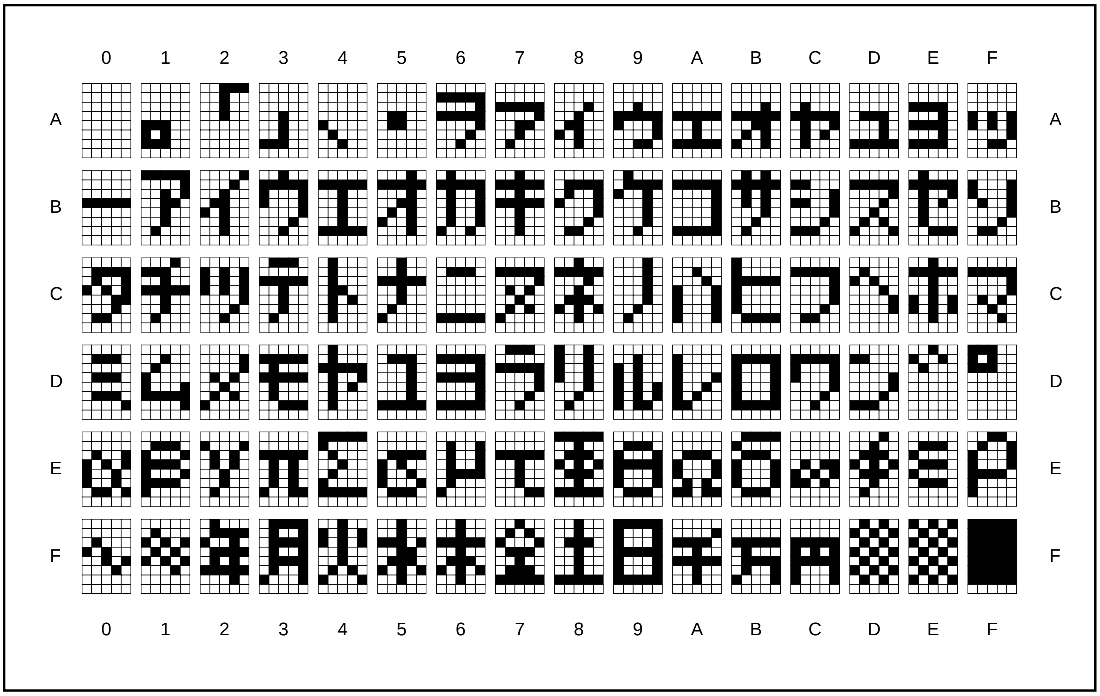
Standard ROM Font



OPTION ROM1 (when R1, R0 = 0, 0 is selected)

Lower 4 Bit of Code

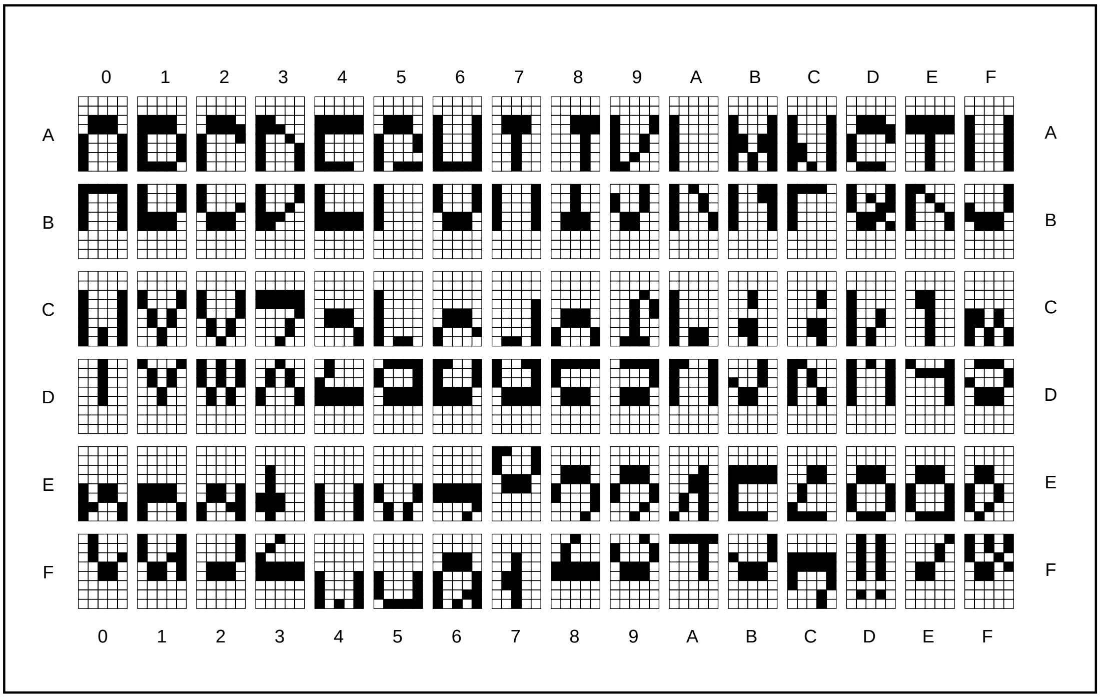
Higher 4 Bit of Code



OPTION ROM2 (when R1, R0 = 0, 1 is selected)

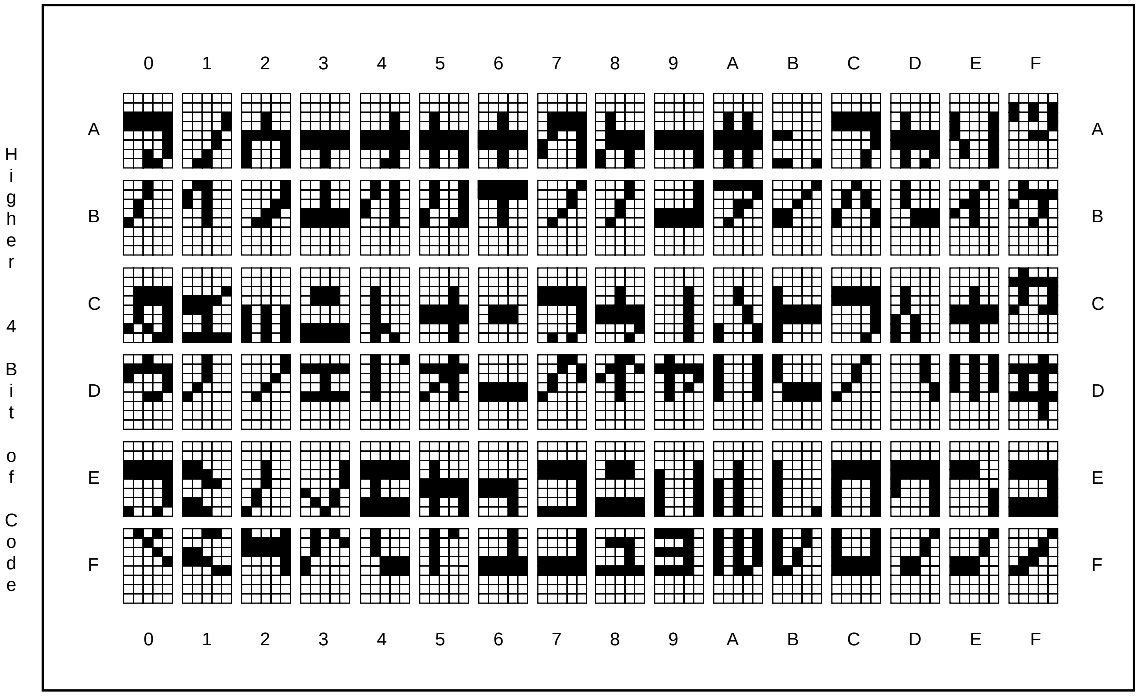
Lower 4 Bit of Code

Higher 4 Bit of Code



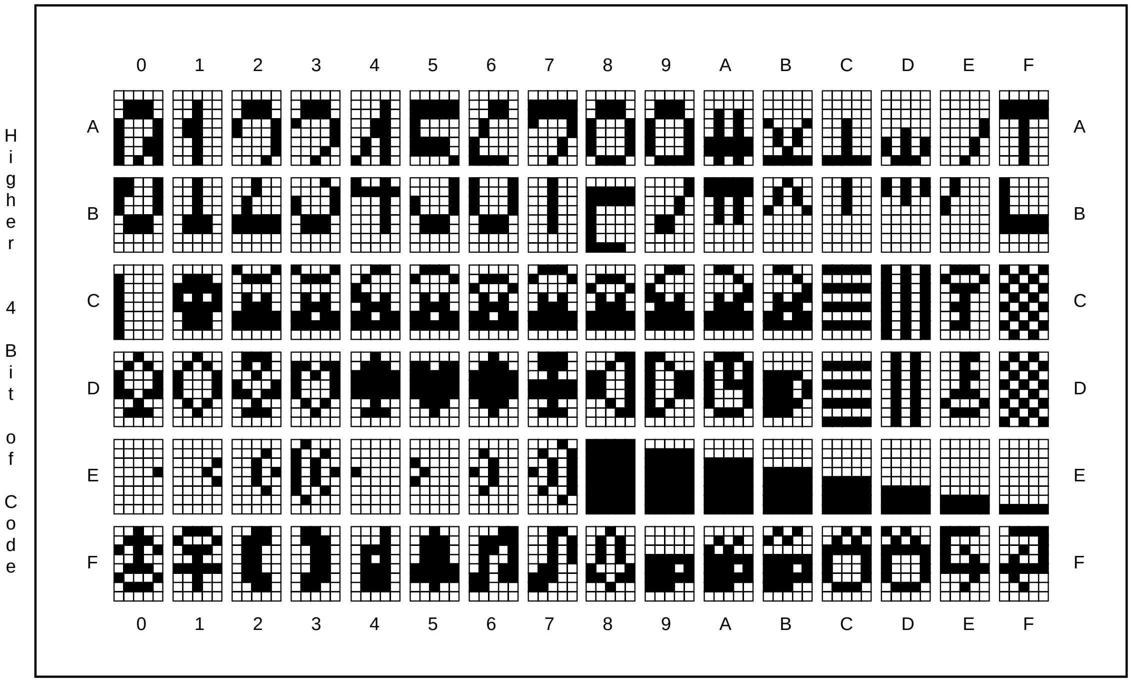
OPTION ROM3 (when R1, R0 = 1, 0 is selected)

Lower 4 Bit of Code



OPTION ROM4 (R1, R0 = 1,1 is selected)

Lower 4 Bit of Code



Character Generator RAM (CGRAM)

The SED1240 series is provided with a CGROM that permits the user to program character patterns so as to attain a character display with a high degree of freedom. When using the CGRAM, select Use of CGRAM by the system set command. The CGRAM capacity is 240 bits having a structure of 5×8 dots and optional 6 types of patterns can be registered.

The relation among CGRAM character patterns, CGRAM addresses, and character codes is shown below.

Character code	RAM Address (CGRAM selection: RE = 1)		CGRAM data (character pattern) D7							D0	Character display SEG
00H 02H 04H	(00H to 07H) (10H to 17H) (20H to 27H)	0	*	*	*	0	1	1	1	1	□■■■■
		1	*	*	*	1	0	0	0	0	■□□□□
		2	*	*	*	1	0	0	0	0	■□□□□
		3	*	*	*	0	1	1	1	1	□■■■■
		4	*	*	*	0	0	0	0	1	□□□□■
		5	*	*	*	0	0	0	0	1	□□□□■
		6	*	*	*	1	1	1	1	0	■■■■□
		7	*	*	*	0	0	0	0	0	□□□□□
01H 03H 05H	(08H to 0FH) (18H to 1FH) (28H to 2FH)	8	*	*	*	0	0	1	0	0	□□■□□
		9	*	*	*	0	0	1	0	0	□□■□□
		A	*	*	*	0	1	1	1	0	□■■■□
		B	*	*	*	0	1	1	1	0	□■■■□
		C	*	*	*	0	1	1	1	0	□■■■□
		D	*	*	*	1	1	1	1	1	■■■■■
		E	*	*	*	1	1	1	1	1	■■■■■
		F	*	*	*	0	0	0	0	0	□□□□□

Unused (D7–D5) Character data (D4–D0)

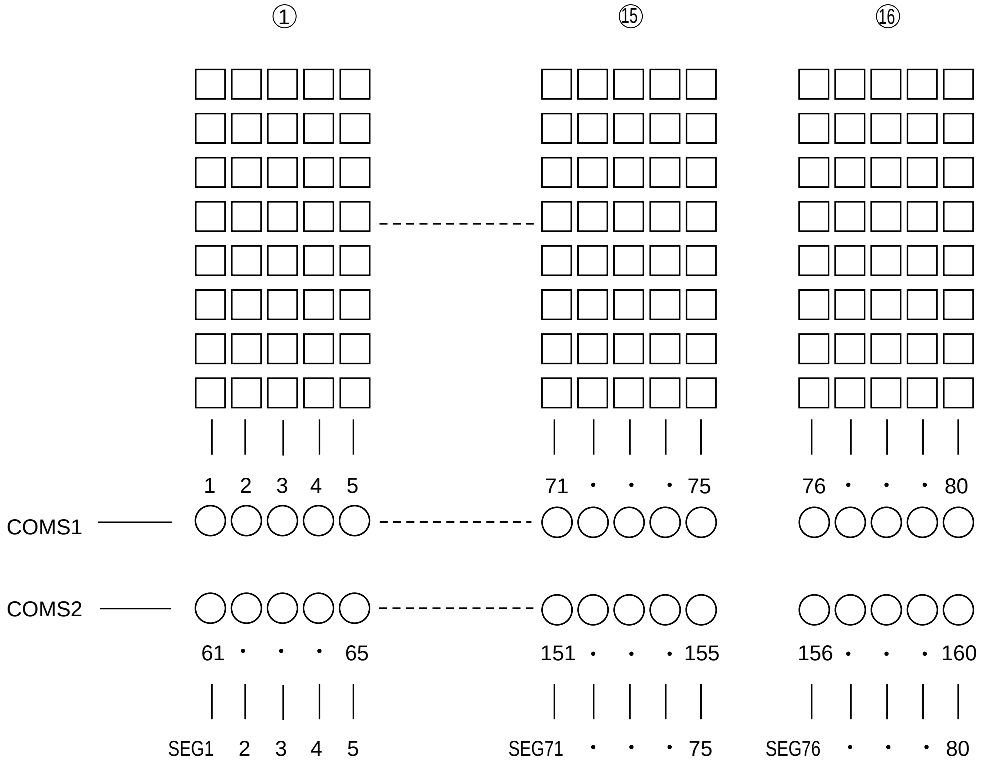
1: Display
0: No display

The character size of 5×8 can also be set. In this case, use the RAM of *7H, *FH of the CGRAM address. However, when the under-bar cursor is used, the data of *7H, *FH is displayed in reverse form.

Symbol Register RAM

The SED1240 series is provided with a symbol register RAM that permits setting each symbol so that symbols may be displayed individually on the screen.
The symbol register capacity is 160 bits in both SED1240, SED1241 and SED1242 series and up to 160 symbols can be displayed.
Each symbol can be blink-controlled in units of bit by using D7 and D6.
The relation among symbol register display patterns, RAM address and write data is shown by citing an example.

[SED1240 (4-line 16-digit display), SED1241 (2-line 16-digit display)]



RAM address [RE = 1]		Bits for symbol							
		D7							D0
60H to 6FH	0	BONF	IORH	*	1	2	3	4	5
	1	BONF	IORH	*	6	7	8	9	10
	:	:							
	F	BONF	IORH	*	76	77	78	79	80
70H to 7FH	0	BONF	IORH	*	81	82	83	84	85
	1	BONF	IORH	*	86	87	88	89	90
	:	:							
	F	BONF	IORH	*	156	157	158	159	160

Note 1: When a symbol is 1.5 times as large as other bits, it is recommended to divide it into COMS1 and COMS2 for driving.

D7 (BONF)	D6 (IORH)	Function
0	*	No blink
1	0	D4 to D0 blink in black-and-white reverse form.
1	1	The bits of "1" out of D4 to D0 blink.

f_{BLINK} : 1 to 2Hz

Static Icon RAM

The SED1240 series can display static icons in the standby mode.
Each of 10 icons can be set in respect of ON/OFF and blink by using the pins of COMSA to SEGSA to J. The relation between static icon functions and static icon RAM write data is shown below.

RAM address [RE = 0]	SI data								Display [□ · · · OFF ■ · · · ON]
	D7	D6	D5	D4	D3	D2	D1	D0	
00H									SEGSA B C D E
	*	*	*	0	0	0	0	0	□ □ □ □ □
	*	*	*	0	0	0	0	1	□ □ □ □ ■
	*	*	*	0	0	0	1	0	□ □ □ ■ □
				⋮					⋮
	*	*	*	1	1	1	1	1	■ ■ ■ ■ ■
01H									SEGSF G H I J
	*	*	*	0	0	0	0	0	□ □ □ □ □
	*	*	*	0	0	0	0	1	□ □ □ □ ■
	*	*	*	0	0	0	1	0	□ □ □ ■ □
				⋮					⋮
	*	*	*	1	1	1	1	1	■ ■ ■ ■ ■

For static icons, blink ON/OFF control can be exerted independently for each pin.

RAM address [RE = 0]	ISB data VS pin								Function
	D7	D6	D5	D4	D3	D2	D1	D0	
02H	*	*	*	SEGSA	SEGSB	SEGSC	SEGSD	SEGSE	Blink 1 = ON 0 = OFF
03H	*	*	*	SEGSF	SEGSG	SEGSH	SEGSI	SEGSJ	

The following table shows a static icon ON/OFF function and static icon blink control.

RAM address [RE = 0]	SI data								Display [□ · · · OFF ■ · · · ON]
	D7	D6	D5	D4	D3	D2	D1	D0	
00H	*	*	*	1	0	1	1	0	SEGSA B C D E
02H	*	*	*	0	1	0	1	0	■ □ ■ ■ □ ⇕ f_{BLINK} ■ ■ ■ □ □

f_{BLINK}: 1 to 2Hz

<Cautions for static icon operation>

- Be sure to write static icon data when the oscillating circuit is on. If the data is written when the oscillating circuit is off (Sleep Mode), previous display may remain and instantaneous lighting may occur.
- To perform resetting on the $\overline{RES}$ terminal except at the time of turning on power, turn off the static icon and blinking in advance, then turn off the oscillating circuit. If resetting is performed when the static icon or blinking is on, instantaneous lighting may be caused by stopping of the oscillating circuit.

Electronic Volume RAM

The SED1240 series is provided with an electronic volume function that permits controlling the liquid crystal drive voltage V_5 and adjusting the density of liquid crystal display. The electronic volume function can select one of 32 states of the liquid crystal drive voltage by writing 5-bit data into the electronic volume RAM.

When a V_5 voltage regulating built-in resistor is used, this function can attain a wider adjustment if the resistor ratio set command is used together.
The relation between electronic volume set RAM addresses and write data is shown below.

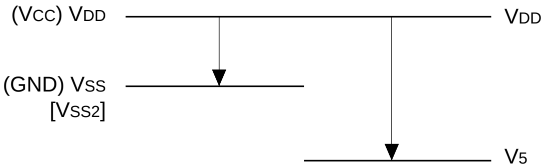
Function	RAMaddress [RE=0]	Electronic volume data								State	V_{EV}
		D7	D6	D5	D4	D3	D2	D1	D0		
Electronic volume	08H	⁎	⁎	⁎	0	0	0	0	0	0	V_{REG-0}
		⁎	⁎	⁎	0	0	0	0	1	1	$V_{REG-\alpha}$
		⁎	⁎	⁎	0	0	0	1	0	2	$V_{REG-2\alpha}$
						· · ·				· · ·	
		⁎	⁎	⁎	1	1	1	0	1	29	$V_{REG-29\alpha}$
		⁎	⁎	⁎	1	1	1	1	0	30	$V_{REG-30\alpha}$
		⁎	⁎	⁎	1	1	1	1	1	31	$V_{REG-31\alpha}$
	09H	⁎	⁎	⁎	⁎	T4	T2	T1	T0	–	For test

⁎ :Unused
α :$\alpha = V_{REG}/150$
Note :Address"09H"(RE=0)isusedfortest.Don'tuseit.

SED1240 Series

ABSOLUTE MAXIMUM RATINGS

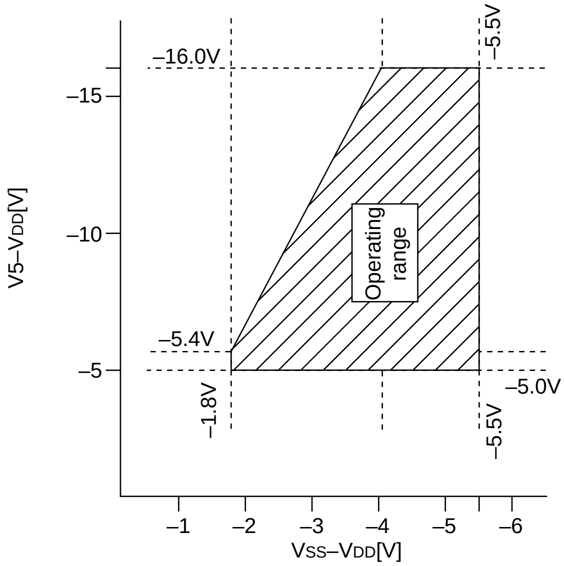
Item		Symbol	Standard value	Unit
Supply voltage (1)		V_{SS}	–7.0 to +0.3	V
Supply voltage (2)		V_{SS2}	–7.0 to +0.3	V
	Double boosting		–7.0 to +0.3	
	Triple boosting		–6.0 to +0.3	
Supply voltage (2)		V_5, V_{OUT}	–18.0 to +0.3	V
Supply voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		T_{opr}	–30 to +85	°C
Storage temperature	TCP	T_{str}	–55 to +100	°C
	Bare chip		–65 to +125	



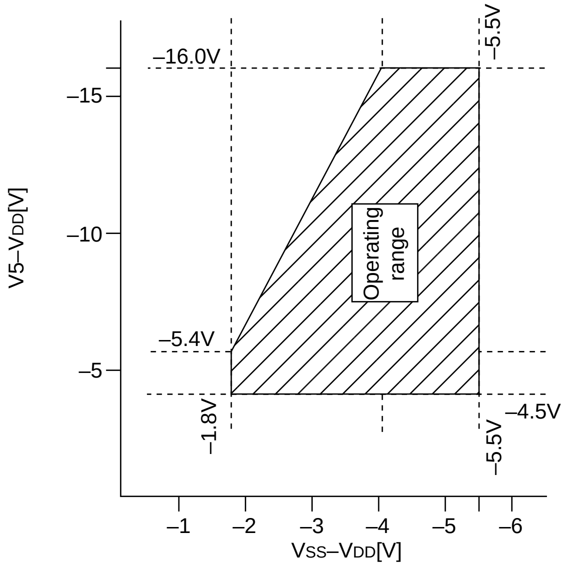
Notes: 1. All the voltage values are based on V_{DD} = 0 V.
2. The voltages of V_1, V_2, V_3, and V_4 must always meet the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and the condition of $V_{DD} \geq V_5 \geq V_{OUT}$, $V_{DD} \geq (V_{SS}, V_{SS2}) \geq V_{OUT}$.
3. If the LSI is used exceeding the absolute maximum ratings, it may result in permanent destruction. It is desirable to use the LSI in the condition of electric characteristics at ordinary operation. If this condition is exceeded, a malfunction may be caused to the LSI, having a bad effect on its reliability.

● Operating voltage range for V_{SS} system (V_{SS} and V_{SS2}) and V_5 system (V_5)
Set the V_{SS2} to ensure that the V_{OUT} does not exceed the following operating voltage range:
It applies when an external power supply is used. When using an internal power supply, make sure to set V_{SS} in such that V_{OUT} may not exceed the operating voltage range of V_5 system given below.

When 1/4 bias is used



When 1/5 bias is used



DC CHARACTERISTICS

[V_{SS} = –5.5 V to –1.8 V, Ta = –30 to 85°C unless otherwise specified]

Item		Symbol	Condition		min	typ	max	Unit	Applicable pin
Supply voltage (1)	Recommended operation	V_{SS}	—		–3.6 –5.5	—	–2.4 –1.8	V	V_{SS} *1
Supply voltage (2)	Recommended operation	V_{SS2}	—		–3.6 –5.5	—	–2.4 –1.8	V	V_{SS2} *2 *9
Supply voltage (3)	Recommended operation	V_5	When 1/4 bias used		–16.0	—	–5.0	V	V_5 *2
			When 1/5 bias used		–16.0	—	–4.5	V	
		V_1, V_2	—		0.6×V_5	—	V_{DD}	V	V_1, V_2
		V_3, V_4	—		V_5	—	0.4×V_5	V	V_3, V_4
High-level input voltage (1)		V_{IHC}	V_{SS} = –2.4V to –1.8V		0.1×V_{SS}	—	V_{DD}	V	*3
Low-level input voltage (1)		V_{ILC}			V_{SS}	—	0.9×V_{SS}	V	
High-level input voltage (2)		V_{IHC}	V_{SS} = –5.5V to –2.4V		0.2×V_{SS}	—	V_{DD}	V	
Low-level input voltage (2)		V_{ILC}			V_{SS}	—	0.8×V_{SS}	V	
Input leak current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	—	1.0	µA	*3
Liquid crystal driver ON resistance		R_{ON}	Ta=25°C ΔV=0.1V	V_5=–7.0V	—	20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}	—		—	0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	During display	V_5=–6V no load		—	—	80	µA	V_{DD} *5
		At standby	Oscillation ON, power OFF		—	—	20	µA	V_{DD} *6
		At sleep	Oscillation OFF, power OFF		—	—	5	µA	V_{DD}
		During access	fcyc=200KHZ		—	—	500	µA	V_{DD} *7
Input pin capacity		C_{IN}	Ta=25°C	f=1MHZ	—	5.0	8.0	pF	*3

Item	Symbol	Condition	min	typ	max	Unit	Applicable pin
Frame frequency	f_{FR}	Ta=25°C V_{SS}=–3.0V	70	100	130	Hz	*10
External clock frequency	f_{CK}	2-line display (SED1242)	—	28.8	—	KHz	*10 *11
	f_{CK}	3-line display (SED1241)	—	41.6	—	KHz	*10 *11
	f_{CK}	4-line display (SED1240)	—	54.4	—	KHz	*10 *11

Item	Symbol	Condition	min	typ	max	Unit	Applicable pin
Minimum reset pulse width	t_{RW}	—	10	—	—	µs	*8
Reset start time	t_{RES}	—	—	—	50	ns	*8

Dynamic system

Item		Symbol	Condition	min	typ	max	Unit	Applicable pin
Built-in power supply	Input voltage	V_{SS2}	Double boosting	–5.5	—	–1.8	V	V_{SS2}
			Triple boosting	–5.5	—	–1.8		
	Boosting output voltage	V_{OUT}	Double boosting	–11.0	—	—	V	V_{OUT}
			Triple boosting	–16.5	—	—		
	Voltage regulating circuit operating voltage	V_{OUT}	—	–16.5	—	–5.4	V	V_{OUT}
	Voltage follower operating voltage	V_5	—	–16.0	—	–4.5	V	V_5 *12
	Reference voltage	V_{REG}	Ta = 25°C –0.05%/°C	–2.06	–2.0	–1.94	V	—

*1: The wide operating voltage range is guaranteed except the case where a sudden voltage change occurs during MPU access.
In the low-supply voltage data holding characteristic, it is applied in the sleep mode and MPU access cannot be guaranteed

*2: At triple boosting, take care about supply voltage V_{SS2} so that it may not exceed the V_5 operating voltage range.

*3: D0 to D5, D6 (SCL), D7 (SI), A0, $\overline{RES}$, $\overline{CS}$, $\overline{WR}$ (E), P/S, IF. C86. $\overline{CK}$

*4: This is a resistance value when a voltage of 0.1 V is applied between output pins SEGn, SEGSn, COMn, and COMSn, and each power pin (V_1, V_2, V_3, V_4). This is specified within the range of operating voltage (2).
$R_{ON} = 0.1\ V / \Delta I$
(ΔI: A current flowing when 0.1 V is applied between the power supply and the output)

*5: Applies under the following conditions:
- No access from MPU during all characters 'H' display
- The built-in circuit and oscillating circuit are operating.
- CGRAM unused, HPM = 0 specified, V_{SS} = -3.0

*6: Applies under the following conditions:
- Standby mode
- ALl the built-in power circuit off
- Display off
- Oscillating circuit on

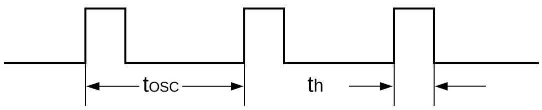
*7: Indicates that fcyc is used for writing at all times. The current consumption during access is approximately proportional to the access frequency (fcyc).

*8: Specifies the $\overline{RES}$ signal minimum pulse width. To perform resetting, it is necessary to input the pulse having a width of t_{RW} or more. Original, the method for reset case 1 is used, but the method for reset case 2 can also be used if the reset start time condition of t_{RES} or less is satisfied.

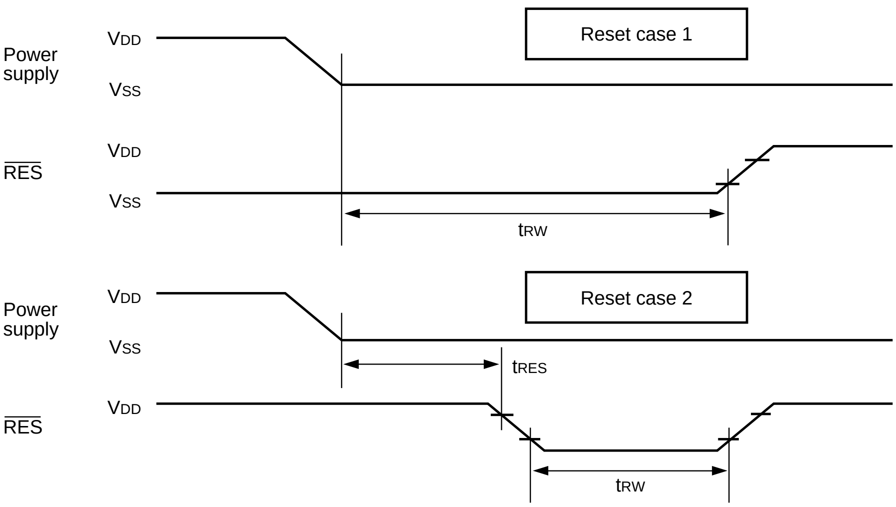
*9: The boosting circuit performs boosting, using voltage between the V_{DD} and V_{SS2} as source voltage. Check the V_{SS2} input voltage to ensure that it does not exceed V_{OUT} absolute maximum rating, or the operating voltage range of the V_{SS} system (V_{SS}) and V_5 system (V_5).

*10: Frequency f_{OSC} of the internal circuit drive oscillating circuit and boosting clock fBST vary according to the type. The following shows the relationship between the oscillating circuit f_{OSC} and boosting clock f BST:
- f_{OSC} = (number of digits) × (1/duty) × f_{FR}
- f_{BST} = (1/2) × (1/number of digits) × f_{OSC}

*11: Enter the following input when performing operations by the external clock, without using the built-in oscillating circuit:
- Duty = (t_h/t_{OSC}) × 100 = 20 to 30%
- $f_{OSC} = 1/t_{OSC}$



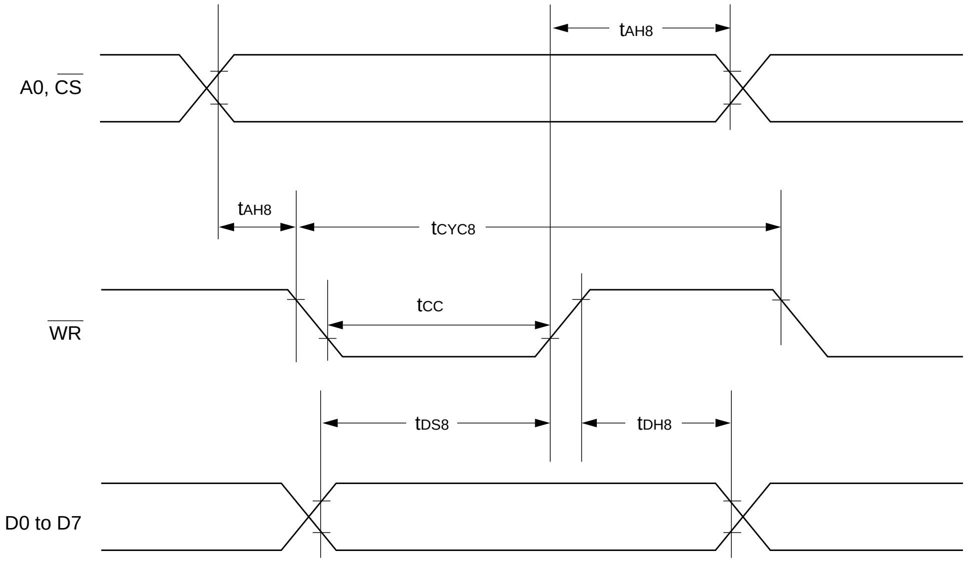
*12: Adjust the V_5 voltage regulating circuit within the voltage follower operating voltage range.



* All timing are specified on the basis of 20% and 80% of V_{SS}.

AC CHARACTERISTICS

System Bus Write Characteristics I (80 series MPU)



[V_{SS} = –5.5 V to –4.5 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}	–	30	–	ns
Address setup time		t_{AW8}	–	60	–	ns
System cycle time	WR	t_{CYC8}	–	300	–	ns
Control pulse width (WR)		t_{CC}	–	60	–	ns
Data setup time	D0 to D7	t_{DS8}	–	60	–	ns
Data hold time		t_{DH8}	–	50	–	ns

[V_{SS} = –4.5 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

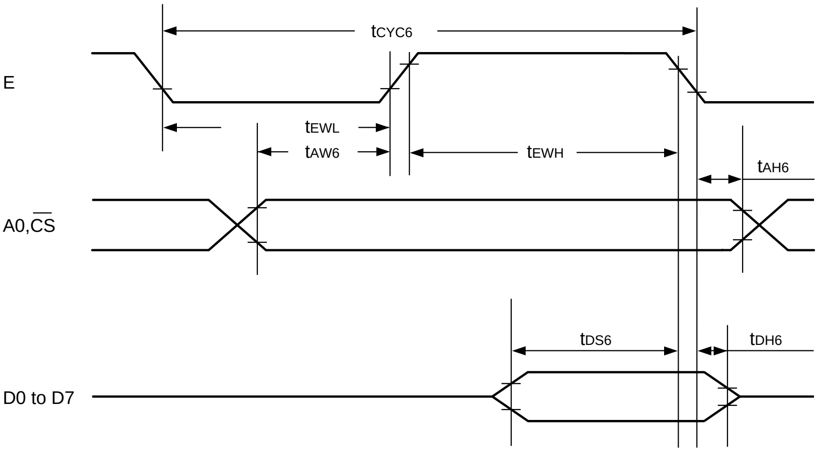
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}	–	30	–	ns
Address setup time		t_{AW8}	–	60	–	ns
System cycle time	WR	t_{CYC8}	–	500	–	ns
Control pulse width (WR)		t_{CC}	–	100	–	ns
Data setup time	D0 to D7	t_{DS8}	–	100	–	ns
Data hold time		t_{DH8}	–	50	–	ns

[V_{SS} = –2.4 V to –1.8 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}	–	30	–	ns
Address setup time		t_{AW8}	–	60	–	ns
System cycle time	WR	t_{CYC8}	–	1000	–	ns
Control pulse width (WR)		t_{CC}	–	200	–	ns
Data setup time	D0 to D7	t_{DS8}	–	200	–	ns
Data hold time		t_{DH8}	–	50	–	ns

*1: At the fall and rise time of input signals, set 15 ns or less.
*2: Every timing is specified on 20% and 80% of V_{SS}.
*3: The same timing is not required for A0 and $\overline{CS}$. Input signals so that A0 and $\overline{CS}$ may satisfy t_{AW8} and t_{AH8} respectively.

System Bus Write Characteristics II (68 series MPU)



[VSS = –5.5 V to –4.5 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	t_{CYC6}	–	300	–	ns
Address setup time		t_{AW6}		60	–	ns
Address hold time		t_{AH6}		30	–	ns
Data setup time	D0 to D7	t_{DS6}	–	60	–	ns
Data hold time		t_{DH6}	–	50	–	ns
Enable H pulse width	E	t_{EWH}	–	60	–	ns
Enable L pulse width	E	t_{EWL}	–	60	–	ns

[VSS = –4.5 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

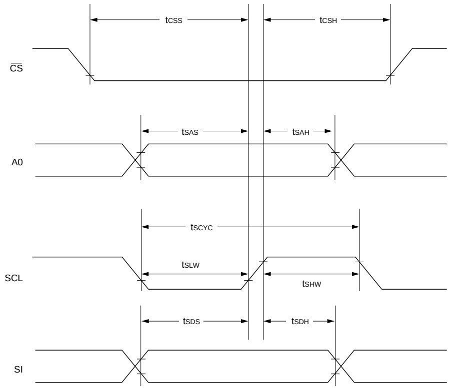
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	t_{CYC6}	–	500	–	ns
Address setup time		t_{AW6}		60	–	ns
Address hold time		t_{AH6}		30	–	ns
Data setup time	D0 to D7	t_{DS6}	–	100	–	ns
Data hold time		t_{DH6}	–	50	–	ns
Enable H pulse width	E	t_{EWH}	–	100	–	ns
Enable L pulse width	E	t_{EWL}	–	100	–	ns

[VSS = –2.4 V to –1.8 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	t_{CYC6}	–	1000	–	ns
Address setup time		t_{AW6}		60	–	ns
Address hold time		t_{AH6}		30	–	ns
Data setup time	D0 to D7	t_{DS6}	–	200	–	ns
Data hold time		t_{DH6}	–	50	–	ns
Enable H pulse width	E	t_{EWH}	–	200	–	ns
Enable L pulse width	E	t_{EWL}	–	200	–	ns

*1: t_{CYC6} indicates the cycle of the E signal in the $\overline{CS}$ active state.
It is necessary to secure t_{CYC6} after $\overline{CS}$ becomes active.
*2: For the rise and fall time of input signals, set 15 ns or less.
*3: Every timing is specified on 20% and 80% of V_{SS}.
*4: The same timing is not required for A0 and $\overline{CS}$. Input signals so that A0 and $\overline{CS}$ may satisfy t_{AW6} and t_{AH6} respectively.

Serial Interface



[VSS = –5.5 V to –4.5 V, Ta = –30 to 85°C]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	t_{SCYC}	–	700	–	ns
SCL "H" pulse width		t_{SHW}	–	250	–	ns
SCL "L" pulse width		t_{SLW}	–	250	–	ns
Address setup time	A0	t_{SAS}	–	50	–	ns
Address hold time		t_{SAH}	–	250	–	ns
Data setup time	SI	t_{SDS}	–	50	–	ns
Data hold time		t_{SDH}	–	50	–	ns
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}	–	150	–	ns
		t_{CSH}	–	500	–	ns

[VSS = –4.5 V to –2.4 V, Ta = –30 to 85°C]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	t_{SCYC}	–	1000	–	ns
SCL "H" pulse width		t_{SHW}	–	300	–	ns
SCL "L" pulse width		t_{SLW}	–	300	–	ns
Address setup time	A0	t_{SAS}	–	50	–	ns
Address hold time		t_{SAH}	–	300	–	ns
Data setup time	SI	t_{SDS}	–	50	–	ns
Data hold time		t_{SDH}	–	50	–	ns
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}	–	150	–	ns
		t_{CSH}	–	700	–	ns

[VSS = –2.4 V to –1.8 V, Ta = –30 to 85°C]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	t_{SCYC}	–	2000	–	ns
SCL "H" pulse width		t_{SHW}	–	300	–	ns
SCL "L" pulse width		t_{SLW}	–	300	–	ns
Address setup time	A0	t_{SAS}	–	50	–	ns
Address hold time		t_{SAH}	–	500	–	ns
Data setup time	SI	t_{SDS}	–	50	–	ns
Data hold time		t_{SDH}	–	50	–	ns
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}	–	150	–	ns
		t_{CSH}	–	900	–	ns

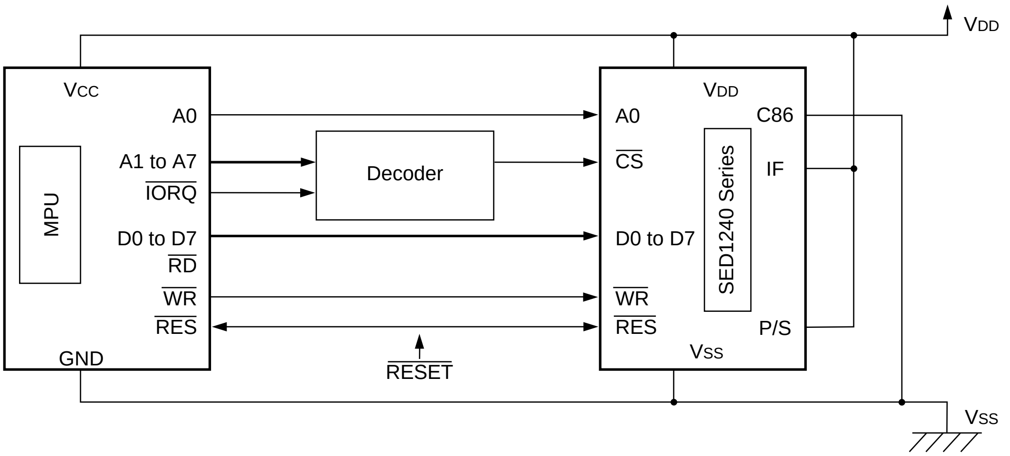
*1: For the rise and fall time of input signals, set 15 ns or less.
*2: Every timing is specified on 20% and 80% of VSS.
*3: To validate a command or data immediately before the rise of $\overline{CS}$, t_{CSH} must be satisfied at the latch timing of D0 data. If $\overline{CS}$ is started at another data latch timing, the previous command or data will not be input.

SED1240 Series

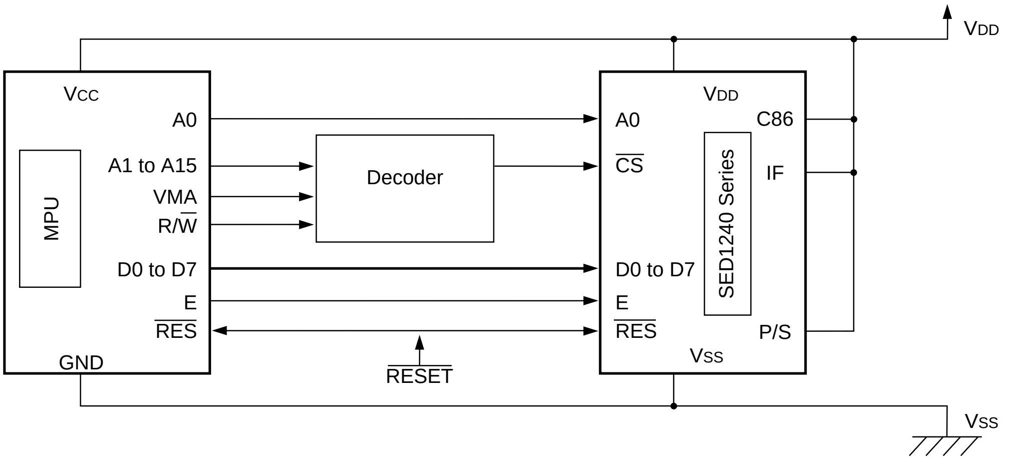
MPU INTERFACE CONNECTION EXAMPLES (FOR REFERENCE)

The SED1240 series can be connected to the 80 series MPU or 68 series MPU. Furthermore, it can be operated with less signal lines if the serial interface is used.
When an MPU bus, port, etc. are put into high-impedance for a certain period by RESET, input RESET into this machine after the input to the SED1240 series becomes definitive.

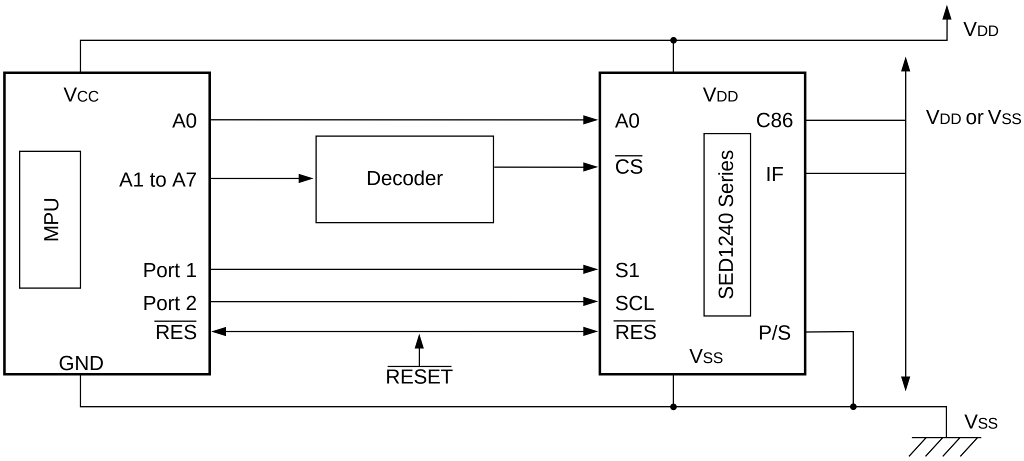
80 Series MPU



68 Series MPU

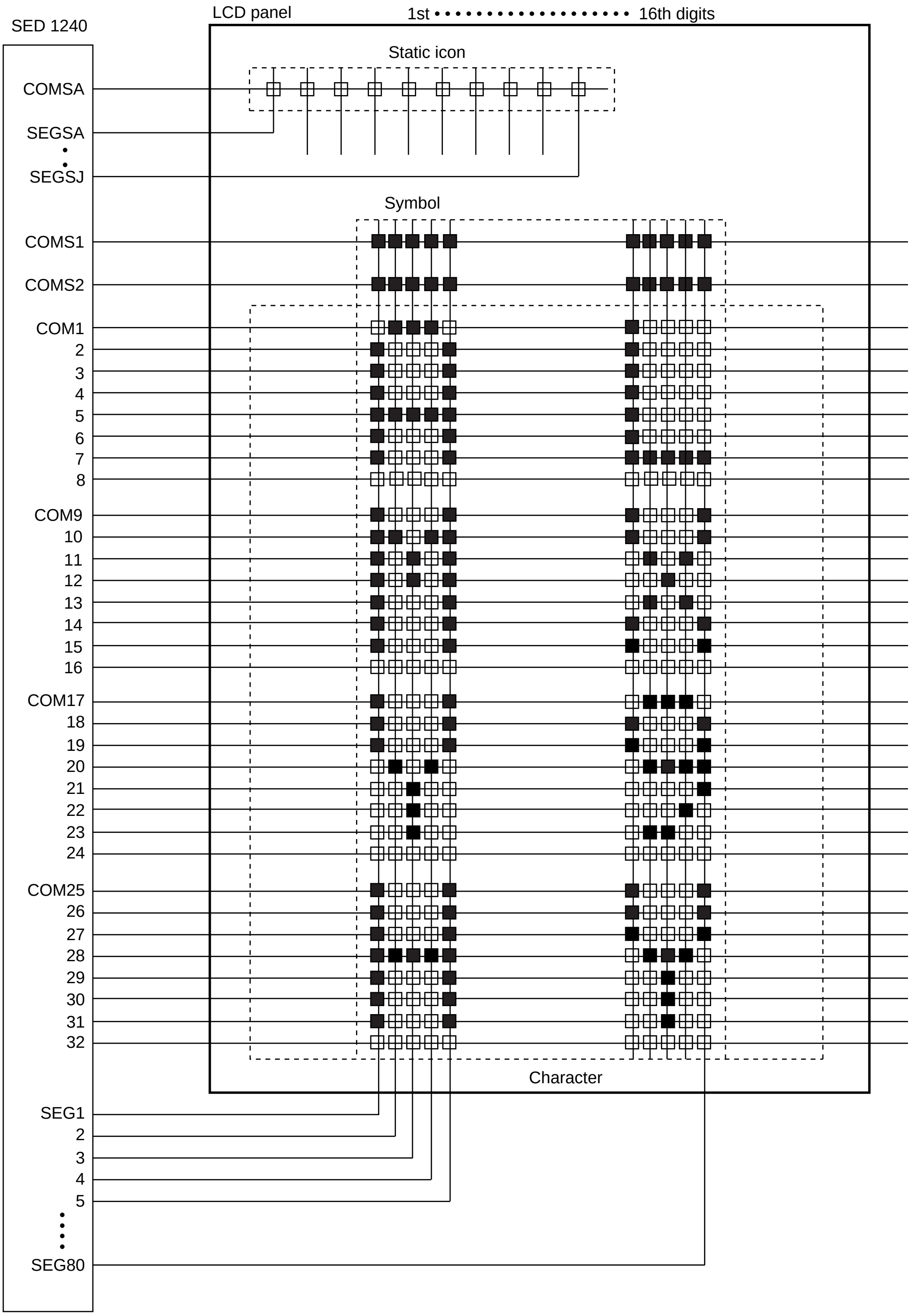


Serial Interface

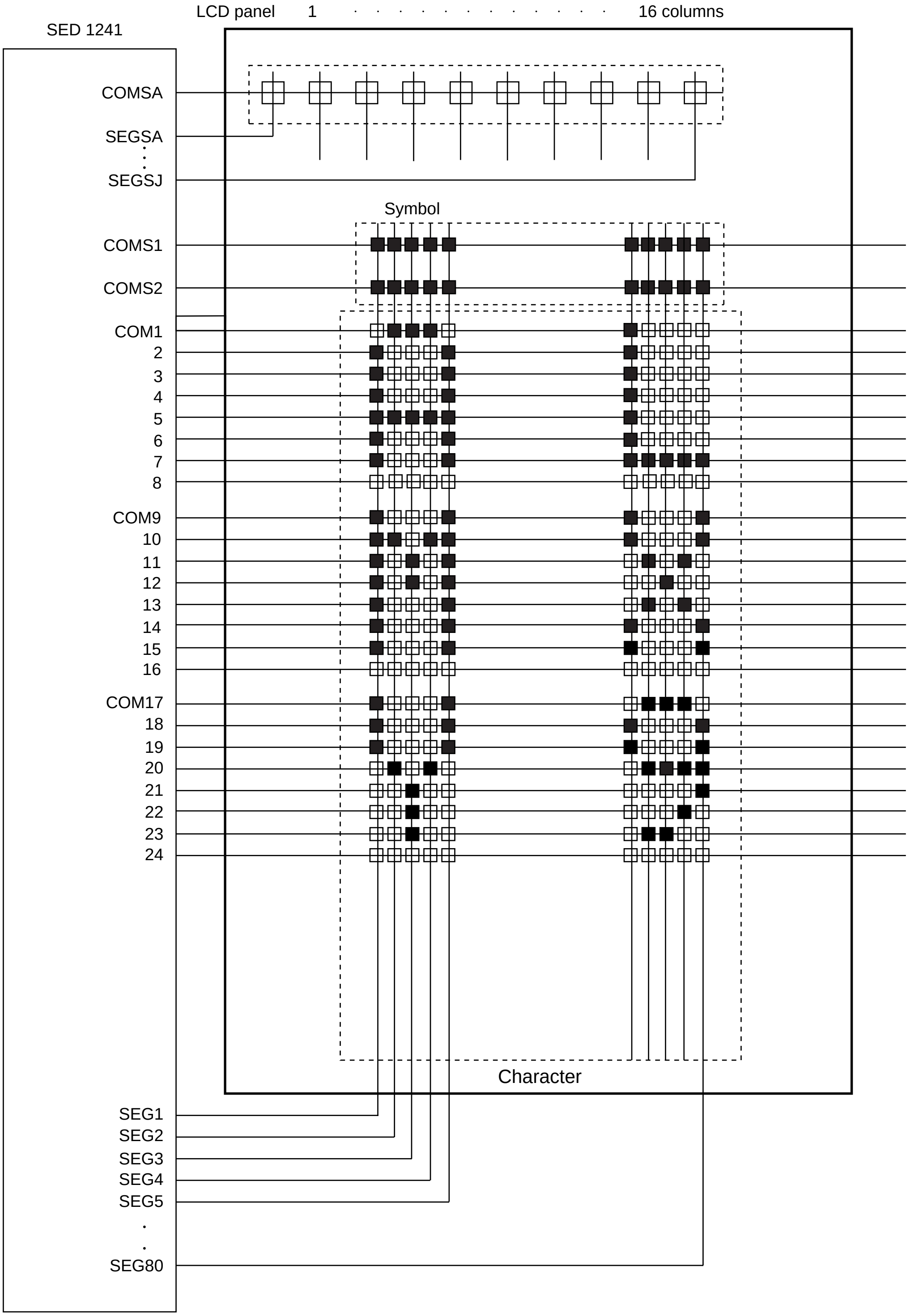


INTERFACE WITH LCD CELL (FOR REFERENCE)

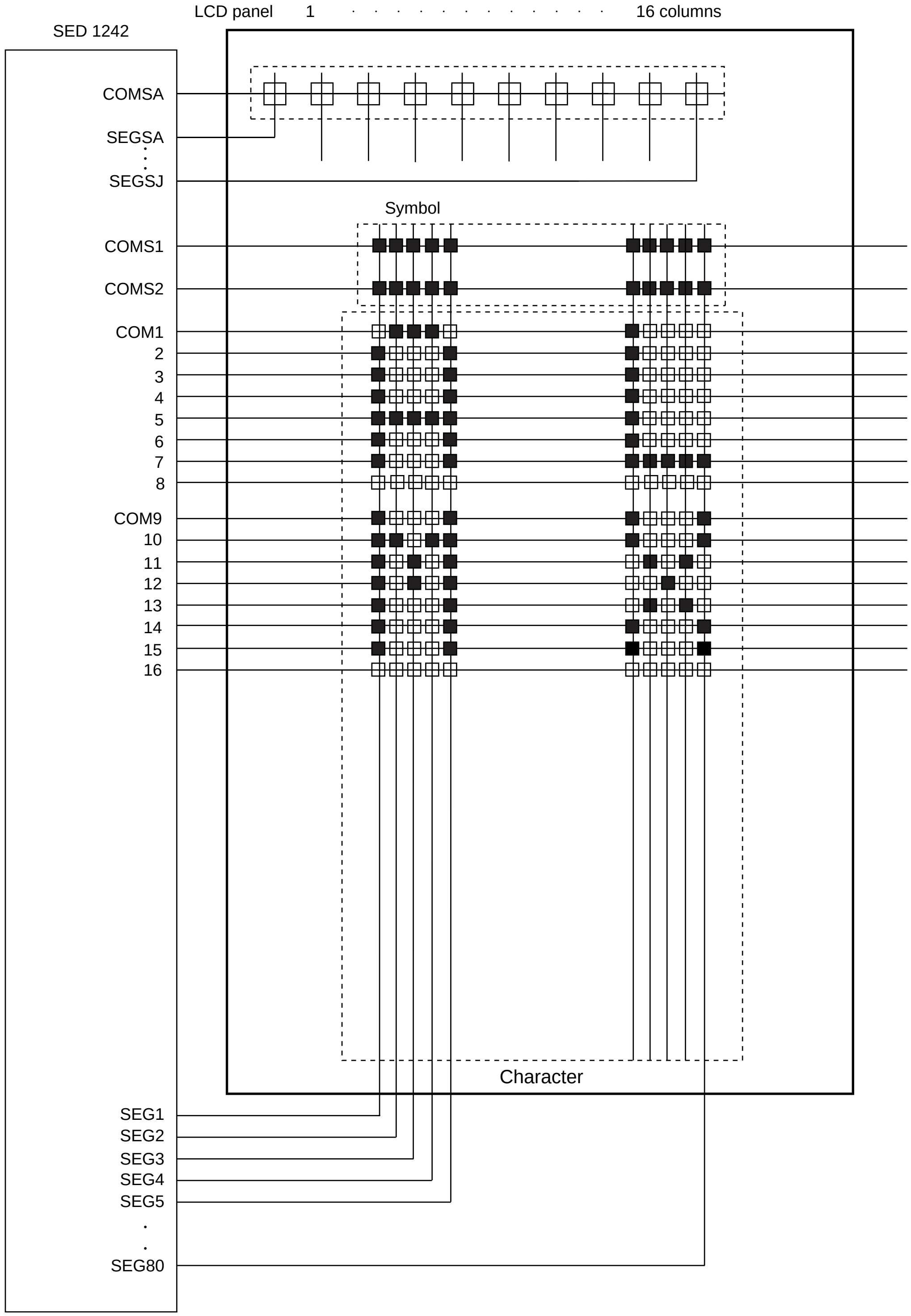
[16 digits × 4 line 5 × 8 dots + symbol]



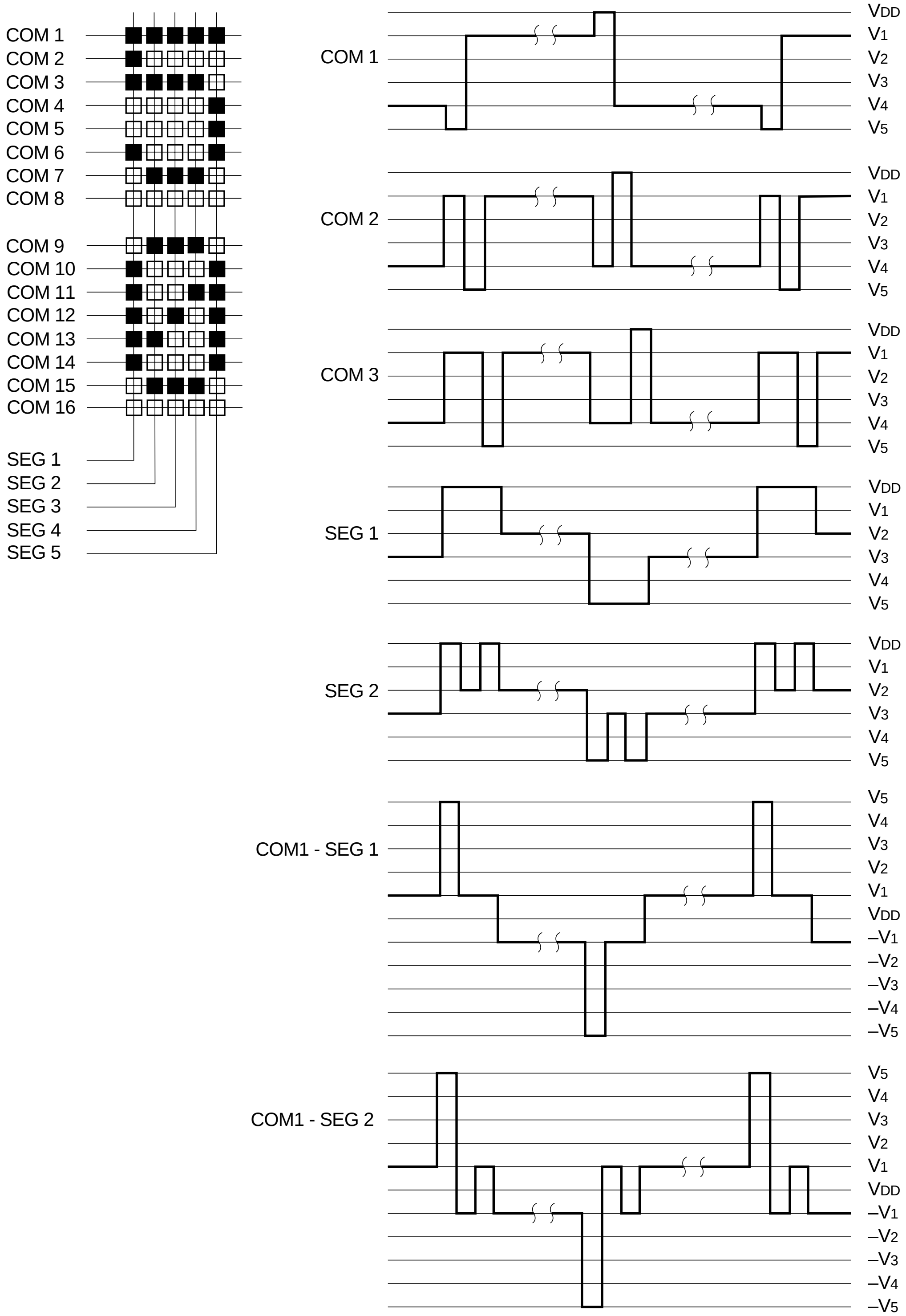
[16 digits × 3 line 5 × 8 dots]



[16 digits × 2 line 5 × 8 dots]



LIQUID CRYSTAL DRIVE WAVEFORM (B WAVEFORM)



Example of Setting the Instructions (Reference)

(1) Initialization

This IC has no power-on reset function when power is turned on. Accordingly, the IC internal status is indefinite when the power has been turned on. Be sure to initialize the system. If electric charge remains in the smoothing capacitor connected between the liquid crystal drive voltage output terminal (V_1 to V_5) and V_{DD} terminal, such a trouble as temporary blackening will occur when power is turned on. To avoid such a trouble, follow the steps given below:

Turn on V_{DD}-V_{SS} power when $\overline{RES}$ terminal="L".

↓

Power stabilizes.

↓

After power and input level to this IC have been stabilized, change $\overline{RES}$ "L" to $\overline{RES}$ "H" subsequent to t_{RW} holding. (Reset clear)

↓

Command state (initial state)
"See this specification No.21".

↓

Wait for 20 microseconds or more

↓

Command input:Asterisked items (*) are in no particular order.
- (0) NOP(Note 0)
- (1) System set
- (2) Power save control
  - -PS : off(power save)
  - -O : on(oscillating circuit)
- (*) Line scroll control set
- (*) Line blink vertical double size display control set
- (*) power control set
  - -IRS,BAS,IRI,IRO
- (*) Electronic volume resistor set
  - -Address :00H -Data (* ,* ,* ,* ,*)
- (7) RAM set (Note 1)
  - -RAM address set
  - -Data write

↓

(8) Power circuit ON

↓

Wait for 500 microseconds or more. (Note 2)

↓

Display ON)D=1) (Note 3)

↓

(10) Static icon control (Notes 3 and 4)
- -Address : 00H -Data (* ,* ,* ,* ,*)
- -Address : 01H -Data (* ,* ,* ,* ,*)
- -Address : 02H -Data (* ,* ,* ,* ,*)
- -Address : 03H -Data (* ,* ,* ,* ,*)

↓

End of initializarion

Note 0 : (0) is a NOP command. This command has a function to clear the test mode. After resetting, it is recommended to execute this command several times before starting input. It is also recommended to execute it on a periodic basis at a proper position of the insutruction.

Note 1: (7) denotes RAM initialization. Set the contents to be displayed in the beginning. For items not to be displayed (RAM clear), use the following steps:
- DDRAM - write 20H (character code).
- CGRAM - write 00H (data "0").
- Symbol register - write 00H (data "0").

The RAM data is unspecified at the time of $\overline{RES}$ input (after power is turned on). If the data "0" is not written at this stage, unexpected display may occur to the unset position.

Note 2: Defined by the rising characteristics of the boosting circuit, power regulating circuit and voltage and follower circuit, time setting varies according to the external capacity. So be sure to make confirmation by external capacity, and set this time.

Note 3: The dynamic drive system display lamp is lit up by the display on/off command when it is on. The static icon lamp is lit by the static icon control command. So to light up the lamp simultaneously with start of display, execute the display on/off control command and static icon control within one frame.

Note 4: Static icon control must be operated when the oscillating circuit is on. (This is mandatory.)

Note 5: (0) to (8) must be performed when display is off.

(2-1) Setting the Standby mode

End of initialization

↓

Normal operation
(Power save is cleared and oscillating circuit is on.)

↓

(1) Display on/off control command input
- D : off (display)

(2) Power conrtol command input
- P, VF, VC : off

(3) Power save command input
- PS : on (power save)
- O : on (oscillate)

↓

Enters Standby status.

↓

Displays only the static icon

(2-1) Resetting the Standby mode

Standby mode

↓

(1) Power save command input
-PS : off (power save)
-O : on (oscillate)

(2) Power control command input
-P, VF, VC : on

↓

Wait for 500 microseconds or more.

↓

(3) Display on/off control command input
- D : off (display)

↓

Returns to normal operation (original state).

(3-1) Setting the Sleep mode

End of initialization

↓

Normal operation
(Power save is cleared and oscillating circuit is on.)

↓

(1) Display on/off control command input
- D : off (display)

(2) Static icon control
- Address : 00H - Data (0, 0, 0, 0, 0)
- Address : 01H - Data (0, 0, 0, 0, 0)
- Address : 02H - Data (0, 0, 0, 0, 0)
- Address : 03H - Data (0, 0, 0, 0, 0)

(3) Power control command input
- P, VF, VC : off

(4) Power save command input
- PS : on (power save)
- O : on (oscillate)

↓

Enters Sleep status.

↓

All displays off

(3-1) Resetting the Sleep mode

Sleep mode

↓

(1) Power save command input
- PS : off (power save)
- O : on (oscillate)

(2) Power control command input
- P, VF, VC : on

↓

Wait for 500 microseconds or more.

↓

(3) Display on/off control command input
- D : on (display)

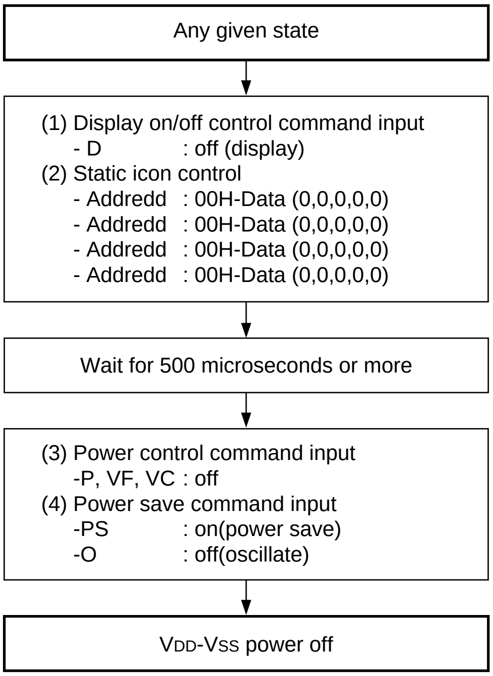
↓

(1) Static icon control
- Address : 00H - Data (*, *, *, *, *)
- Address : 01H - Data (*, *, *, *, *)
- Address : 02H - Data (*, *, *, *, *)
- Address : 03H - Data (*, *, *, *, *)

↓

Returns to normal operation (original state).

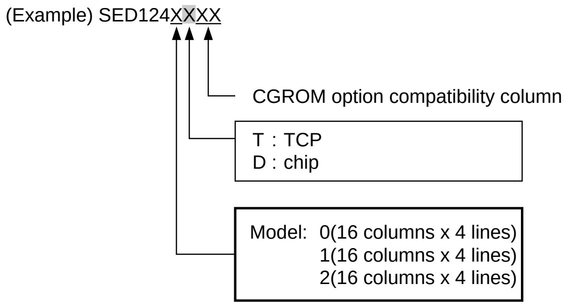
(4) Power off sequence
Similar to the case of power on sequence, if this IC power is turned off when the built-in power is on, power supply to the built-in liquid crystal drive circuit may continue for a very little time, adversely affecting the liquid crystal panel display quality. To prevent this, strictly follow the power off sequence.



OPTIONS LIST

The SED 1240 series has the following options. Options are available exclusively for users. Please contact our Sales Department.

○ The following shows how to define the name of the product compatible with options:



Character Generator ROM (CGROM) Specifications

The SED1240 series is provided with a character generator ROM for up to 544 types of characters. Each character size is of a structure of 5×7 (8) dots.

This CGROM is designed as a masked ROM, and is compatible with the CGROM for exclusive use of the user. For the standard CGROM, see the Character Font Table.

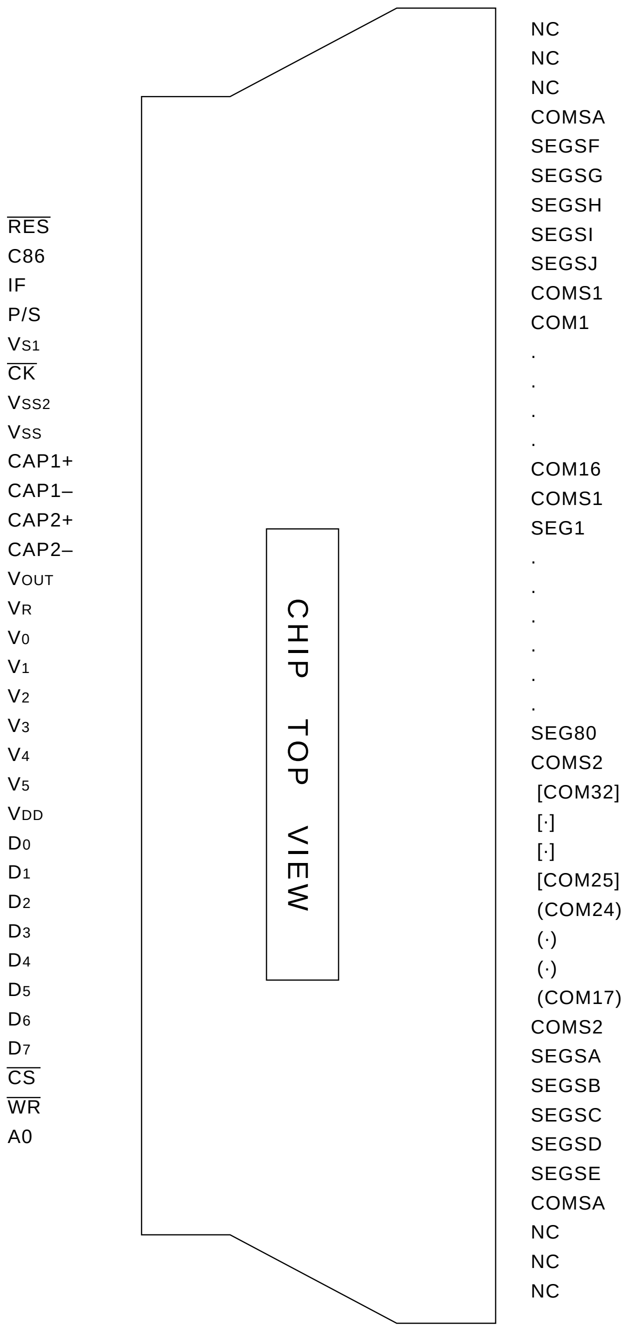
TCP Specifications

The SED1240 series is compatible with the TCP specifications exclusive to the user, in addition to our standard TCP. Please contact our Sales Department for information.

Example of TCP Arrangement

Note: The following does not specify the TCP external view.

REFERENCE

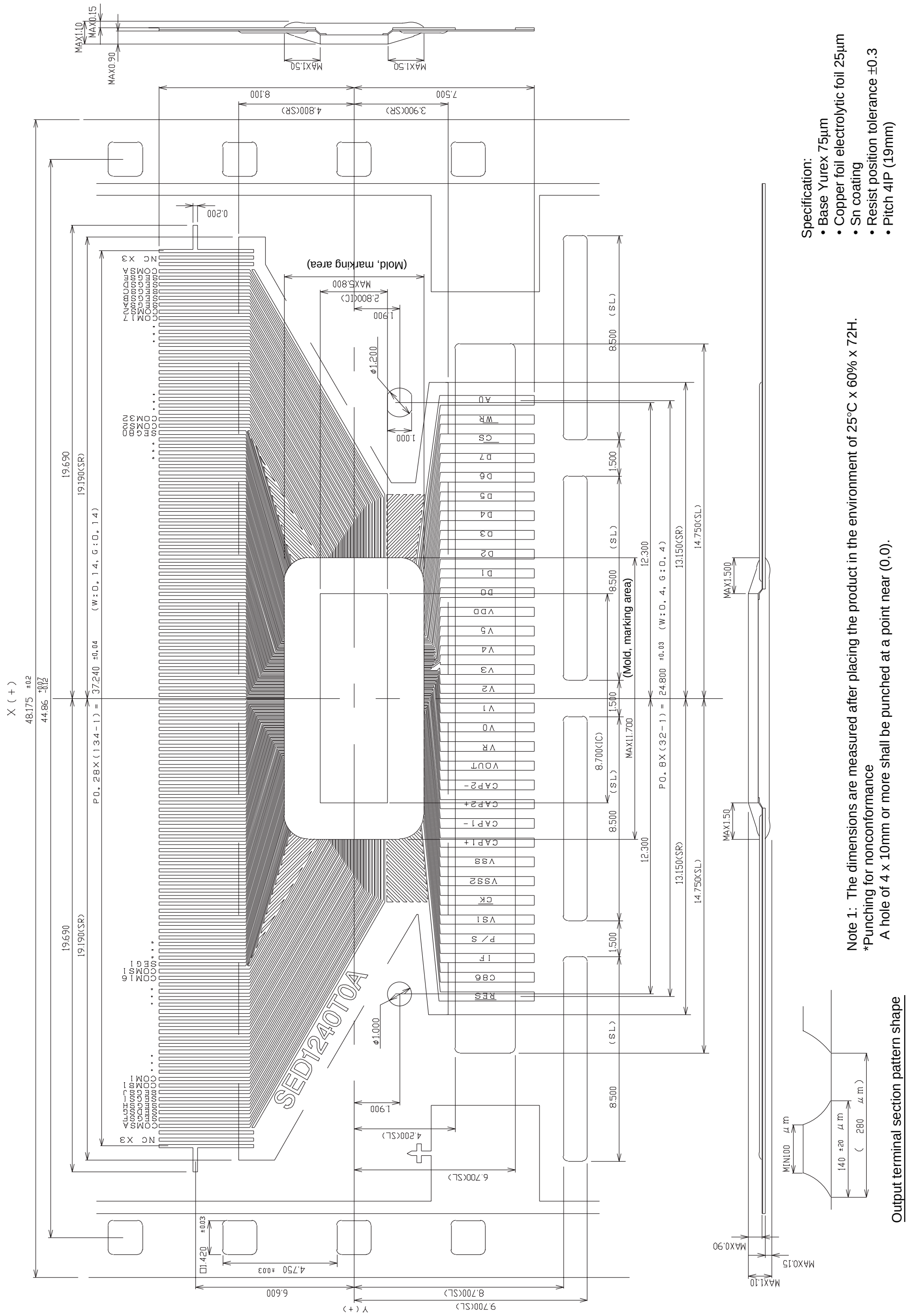


SED1240TXX: COM1 to 16, (COM17 to 24) and [COM25 to 32] are used.
SED1241TXX: COM1 to 16 and (COM17 to 24) are used. [COM25 to 32] is for NC.
SED1242TXX: COM1 to 16 is used. (COM17 to 24) and [COM25 to 32] are for NC.

EXAMPLE OF TCP

TCP External View

REFERENCE



SED1278
LCD Controller/Drivers

Technical Manual

Contents

OVERVIEW

The SED1278 is a dedicated character display controller/driver which, when used with the SED1181F or the SED1681 segment drivres, is able to display up to 80 characters under 4- or 8-bit MPU control.

The internal character generator (CG) ROM has an extended 240, 5×10 pixel, character set, plus CGRAM space for an additional eight user definable 5×8 pixel characters. These memory features combined with the rich set of control instructions offer the potential for a highly flexible character display system.

The SED1278 features a guaranteed minimum LCD drive voltage of 3 V making it suitable for use with low voltage LCD panels.

FEATURES

- Interface for 4- and 8-bit MPUs
- Display RAM – 80 bytes (80 characters)
- Character generator ROM – 240 characters
  - 5×8 pixel font
- Character genrator RAM – 64 bytes
  - 5×8 pixel font, 8 characters.
  - 5×10 pixel font, 4 characters.
- Number of characters used

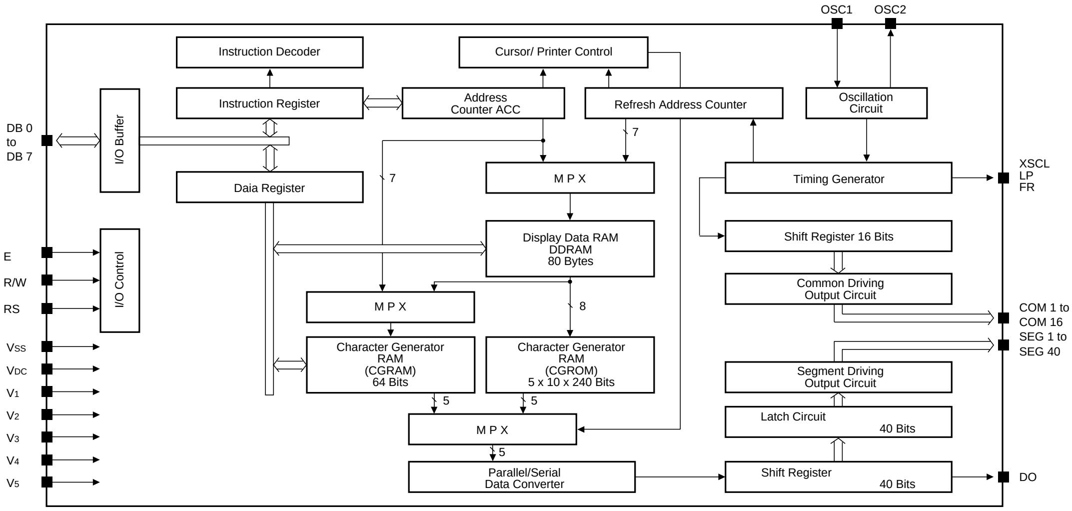
	Duty	SED1278F	SED1181FLA	No. of characters used
One-line display	1/8, 1/11	1	0	8 columns × 1 line
			6	80 columns × 1 line
Two-line display	1/16	1	0	8 columns × 2 lines
			3	40 columns × 2 lines

- Powerful display control instructions
- LCD driver outputs
  - 40 segment driver outputs
  - 16 common driver outputs
- Low LCD drive voltage – 3 V minimum (V_{DD}–V_5)
- Dual-frame AC drive
- On-chip power-on reset
- On-chip RC oscillator
- Single 5 V operation
- Chip (SED1278D) and 80-pin QFP (SED1278F) packages

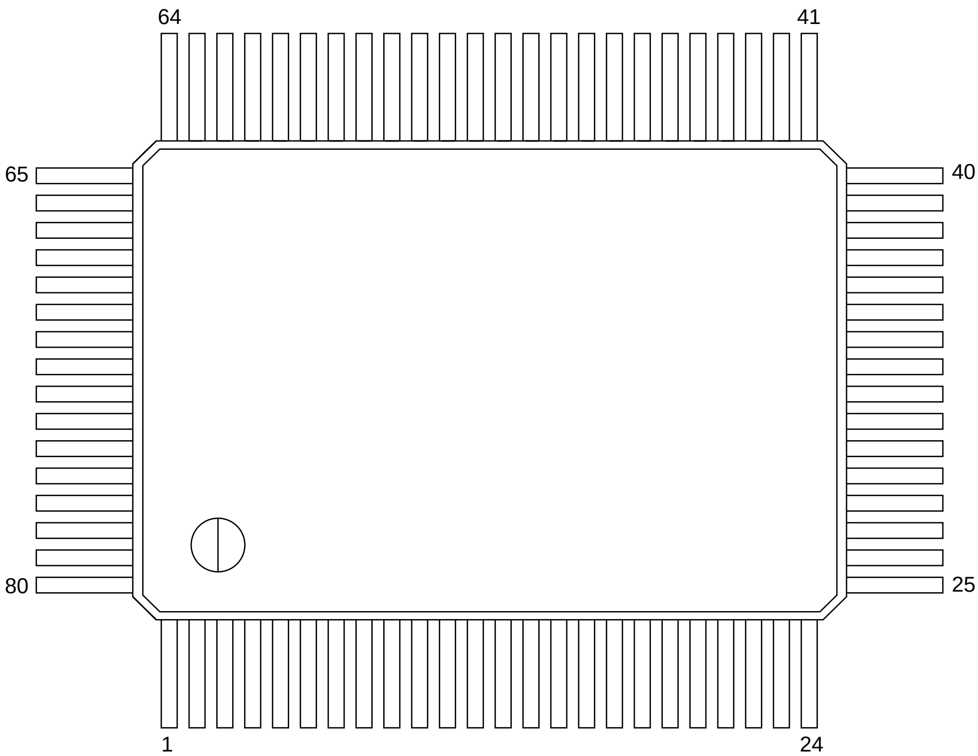
(Compatible with HD 44780 and HD 66780 by Hitachi Limited)

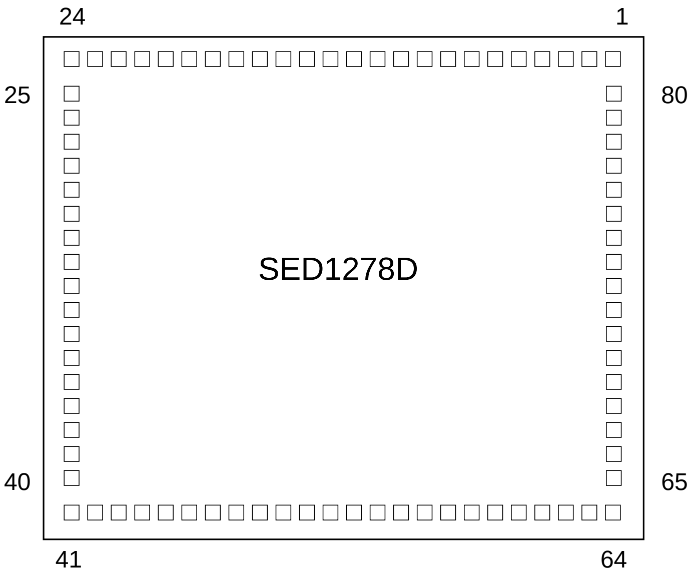
The SED1278 is equivalent to the HD 44780 and HD 66780 by Hitachi Limited. Before use, make sure that there is no problem for practical use. It should be noted that this is not intended to guarantee enforcement of industrial property and other rights, or to grant license for the use of this product.

BLOCK DIAGRAM



PACKAGE OUTLINE





PINOUT

Pin		Pin		Pin		Pin	
Number	**Name**	**Number**	**Name**	**Number**	**Name**	**Number**	**Name**
1	SEG22	21	SEG2	41	DB2	61	COM15
2	SEG21	22	SEG1	42	DB3	62	COM16
3	SEG20	23	GND	43	DB4	63	SEG40
4	SEG19	24	OSC1	44	DB5	64	SEG39
5	SEG18	25	OSC2	45	DB6	65	SEG38
6	SEG17	26	V_1	46	DB7	66	SEG37
7	SEG16	27	V_2	47	COM1	67	SEG36
8	SEG15	28	V_3	48	COM2	68	SEG35
9	SEG14	29	V_4	49	COM3	69	SEG34
10	SEG13	30	V_5	50	COM4	70	SEG33
11	SEG12	31	LP	51	COM5	71	SEG32
12	SEG11	32	XSCL	52	COM6	72	SEG31
13	SEG10	33	V_{DD}	53	COM7	73	SEG30
14	SEG9	34	FR	54	COM8	74	SEG29
15	SEG8	35	DO	55	COM9	75	SEG28
16	SEG7	36	RS	56	COM10	76	SEG27
17	SEG6	37	R/W	57	COM11	77	SEG26
18	SEG5	38	E	58	COM12	78	SEG25
19	SEG4	39	DB0	59	COM13	79	SEG24
20	SEG3	40	DB1	60	COM14	80	SEG23

PIN DESCRIPTION

MPU Interface

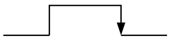
RS Register select signal input. Selects between the data and instruction registers during CPU access.
RS = 0: Instruction register access cycle
RS = 1: Data register access cycle

R/W This input selects between SED1278 register read and write cycles.
R/W = 0: Register write cycle
R/W = 1: Register read cycle

E Read/write execute signal input.

DB0 to DB7 TTL level data input/output lines, for connection to the system MPU data bus.

TABLE 1 The Function of the E Signal

RS	R/W	E	Operation
0	0		Instruction write cycle
0	1	1	Busy flag read cycle Address counter read cycle
1	0		DDRAM or CGRAM data write cycle
1	1	1	DDRAM or CGRAM data read cycle

LCD Panel Interface

COM1 to COM16 Common driver outputs to the LCD panel.

SEG1 to SEG40 Segment driver outputs to the LCD panel.

OSC1 If the internal RC oscillator is used to generate the LCD drive signals, the feedback resistor, R_f, is connected to this pin. If an external clock source is used, the clock is connected to this pin.

OSC2 If the internal RC oscillator is used to generate the LCD drive signals, the feedback resistor, R_f, is connected to this pin. If an external clock source is used, this pin is left open.

External Segment Driver Interface

LP Data latch pulse output for an external X-driver.

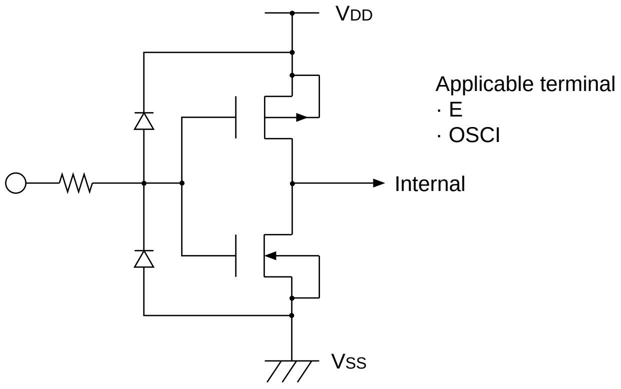
XSCL Data shift clock output for an external X-driver.

FR LCD AC-drive waveform for an external X-driver.

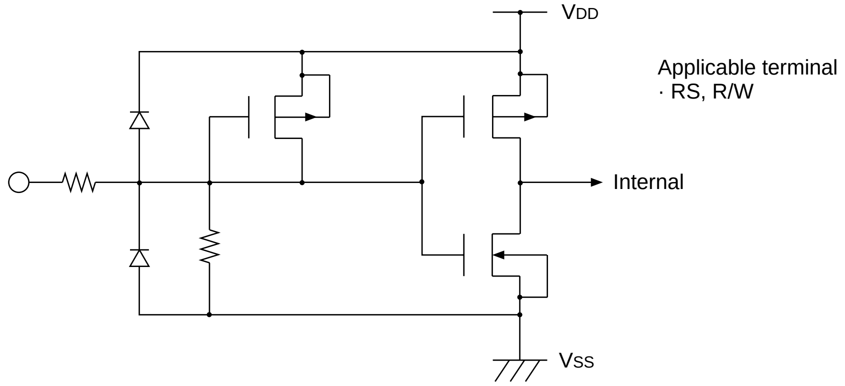
DO Display data output for an external X-driver.

TERMINAL CONFIGURATION

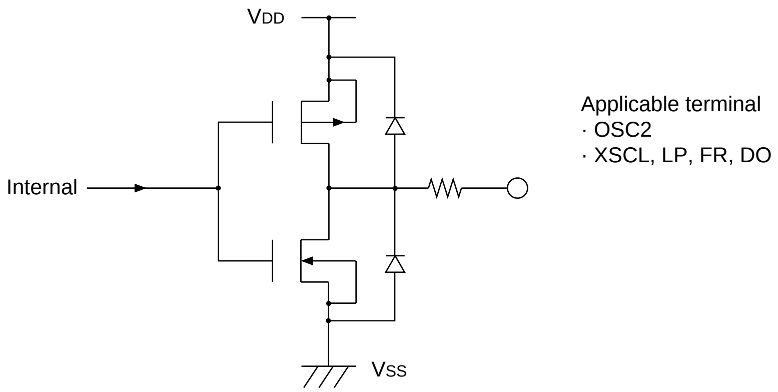
1. Input terminal configuration (1)



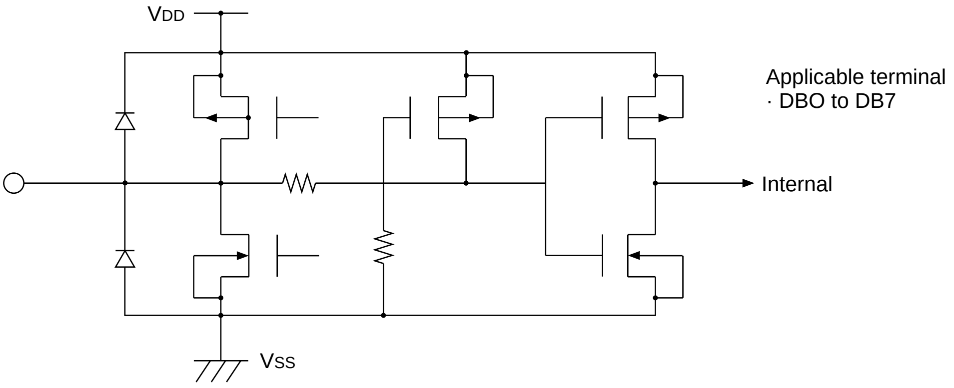
2. Input terminal configuration (2)
With pull-up MOS resistor



3. Output terminal configuration



4. Input/Output terminal configuration



INSTRUCTION DESCRIPTION

Instruction Summary

Instruction	Code										Description	Cycle Time (max.)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display data and sets DDRAM address 0 in the address counter.	410 clocks
Return Home	0	0	0	0	0	0	0	0	1	*	Set DDRAM address 0 in the address counter. Also returns any shifted data to home. The contents of DDRAM remain unchanged.	410 clocks
Entry Mode Set	0	0	0	0	0	0	0	1	I/$\overline{D}$	S	Specifies the direction in which the cursor moves and whether the display is to be shifted or not, when data is writen to or read from memory	10 clocks
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Sets all display on/off (D) cursor on/off (C), and character blinking in the cursor position (B).	10 clocks
Cursor or Display Shift	0	0	0	0	0	1	S/$\overline{C}$	R/$\overline{L}$	*	*	Moves the cursor and shifts the display without changing the contents of DDRAM.	10 clocks
System Set	0	0	0	0	1	IF	N	F	*	*	Sets the interface data length (IF), number of characters to be displayed (N), and character font (F).	10 clocks
Set CGRAM Address	0	0	0	1	ACG						Set CGRAM addresses, followed by transfer of CGRAM data.	10 clocks
Set DDRAM Address	0	0	1	ADD							Sets DDRAM address, followed by transfer of DDRAM data.	10 clocks
Read Busy Flag and Address	0	1	BF	ACC							Reads the busy flag (BF) which indicates internal operation and the contents of the address counter.	0
Write Data to CG or DDRAM	1	0	Write Data								Writes data to DDRAM or CGRAM.	10 clocks
Read Data from CG or DDRAM	1	1	Read Data								Reads data from DDRAM or CGRAM.	10 clocks

* Don’t care

Write Only Instructions

Clear Display

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	01H

RS = 0

This instruction

1. loads all locations in the display data (DD) RAM with 20H.
2. clears the contents of the address counter to 0H.
3. sets the display for zero character shift.
4. sets the address counter to point to the DDRAM.
5. , if the cursor is displayed, moves the cursor to the left most character in the display or, if a two line display is used, moves the cursor to the leftmost character in the top line (line 1).
6. sets the address counter to increment on each access of DDRAM or CGRAM.

Cursor Home

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	1	*	02H, 03H

RS = 0

This instruction

1. clears the contents of the address counter to 0H.
2. sets the address counter to point to the DDRAM.
3. sets the display for zero character shift.
4. , if the cursor is displayed, moves the cursor to the left most character in the display or, if a two line display is used, the left most character in the top line (line 1).

Entry Mode Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	I/$\overline{D}$	S	04H to 07H

RS = 0

- The I/$\overline{D}$ bit selects the way in which the contents of the address counter are modified after every access to DDRAM or CGRAM.
  - I/$\overline{D}$ = 1: The address counter is incremented.
  - I/$\overline{D}$ = 0: The address counter is decremented.
- The S bit enables display shift, instead of cursor shift, after each write or read to the DDRAM.
  - S = 1: Display shift enabled.
  - S = 0: Cursor shift enabled.

  The direction in which the display is shifted is opposite in sense to that of the cursor. For example if S = 0 and I/$\overline{D}$ = 1 the cursor would shift one character to the right after an MPU write to DDRAM. However if S = 1 and I/$\overline{D}$ = 1, the display would shift one character to the left and the cursor would maintain its position on the panel.

  The cursor will already be shifted in the direction selected by I/$\overline{D}$ during reads of the DDRAM, irrespective of the value of S. Similarly reading and writing the CGRAM always shifts the cursor. Note that if a two line display is used both lines will be shifted simultaneously.

Display ON/OFF

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	D	C	B	08H to 0FH

RS = 0

This instruction controls various features of the display.

- The D bit turns the entire display on or off.
  - D = 1: Display on
  - D = 0: Display off
- The C bit turns the cursor on or off.
  - C = 1: Cursor on
  - C = 0: Cursor off
- The B bit enables blinking of the character the cursor coincides with.
  - B = 1: Blinking on
  - B = 0: Blinking off

  Blinking is achieved by alternating between a normal and all dark display of a character. The blinking period is set at 204800 f_{OSC}. For example if f_{OSC} = 250 kHz the cursor will blink with a period of 0.8192 seconds, or about 1.2 Hz.

Cursor/Display Shift

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	S/$\overline{C}$	R/$\overline{L}$	*	*	10H to 1FH

RS = 0

This instruction shifts the display and/or moves the cursor, on character to the left or right, regardless of a DDRAM ready/write.

- The S/$\overline{C}$ bit selects movement of the cursor or movement of both the cursor and the display.
  - S/$\overline{C}$ = 1: Shift both cursor and display
  - S/$\overline{C}$ = 0: Shift cursor only
- The R/$\overline{L}$ bit selects leftward or rightward movement of the display and/or cursor.
  - R/$\overline{L}$ = 1: Shift one character right
  - R/$\overline{L}$ = 0: Shift one character left

System Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	1	IF	N	F	*	*	20H to 3FH

RS = 0

This instruction initializes the system, and must be the first instruction executed after power-on.

- The IF bit selects between an 8-bit or a 4-bit MPU interface.
  - IF = 1: 8-bit MPU interface using DB7 to DB0.
  - IF = 0: 4-bit MPU interface using DB7 to DB4.
- The N and F bits select the number of display lines and the corresponding duty cycle, as listed in table 2.

TABLE 2 Combinations of Display Lines and Duty Cycle

N	F	Number of Line	Duty Ratio	Common Output Signal	Non-Selected Common Output Signal
0	0	1 line	1/8	COM1 to COM8	COM9 to COM16
0	1	1 line	1/11	COM1 to COM11	COM12 to COM16
1	*	2 lines	1/16	COM1 to COM16	—

Set CGRAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	ACR						40H to 7FH

RS = 0

This instruction
1. loads a new 6-bit address into the address counter.
2. sets the address counter to address CGRAM.

Once "Set CGRAM Address" has been executed, the contents of the address counter will be automatically modified after every access of CGRAM, as determined by the "Entry Mode Set" instruction.

If the "Set CGRAM Address" instruction is issued by the system MPU while the display is enabled, and if either the cursor is on or blink is on, pseudo-cursor or pseudo-blink appears. To prevent this, turn both the cursor and display blink off before loading a new CGRAM address.

The active width of the address counter, when it is addressing CGRAM, is 6-bits so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CGRAM.

Set DDRAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	ADD						

RS = 0

80H to CFH … 1 line
80H to A7H line 1 … 2 line
C0H to E7H line 2 … 2 line

This instruction
1. loads a new 7-bit address into the address counter.
2. sets the address counter to point to the DDRAM.

Once the "Set DDRAM Address" instruction has been executed, the contents of the address counter will be automatically modified after each access of DDRAM, as selected by the "Entry Mode Set" instruction.

The SED1278 has only 80 DDRAM locations. The valid address spaces for various display configurations are listed in table 3.

TABLE 3 Valid CGRAM Address Ranges

Number of Lines		Characters	ADR
1-line		80	00H to 4FH
2-line	1st line	40	00H to 27H
	2nd line	40	40H to 67H

Write Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DATA							

RS = 1

This instruction writes the data in DB7 to DB0 into either the CGRAM or the DDRAM. The RAM space (CG or DD), and the address in that space, that is accessed depends on whether a "Set CGRAM Address" or a "Set DDRAM Address" instruction was last executed, and on the parameters of that instruction.

The contents of the address counter will be automatically modified after each "Write Data", as determined by "Entry Mode Set". When data is written to the CGRAM, the DB7, DB6 and DB5 bits are not displayed directly as characters.

Read Only Instructions

Read Busy Flag/Address Counter

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BF	ACC						

RS = 1

Reading the instruction register yields the current value of the address counter and the busy flag. This instruction must be executed prior to any other instructions.

- ACC, the address counter value, will point to a location in either CGRAM or DDRAM, depending on the type of "Set RAM Address" instruction last sent.
  In "Busy Flag Check" immediately after executing "RAM Address Set" instruction, a valid address counter value can be read 5 clock cycles after the busy flag (BF) goes low.
  In "Busy Flag Check" immediately after executing "Write Data" instruction, a valid address counter value can be ready as soon as BF goes low.
- The BF bit shows the status of the busy flag.
  - BF = 1: SED1278 busy.
  - BF = 0: SED1278 ready for next instruction.

Read Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DATA							

RS = 1

This instruction reads data from either CGRAM or DDRAM, depending on the type of "Set RAM Address" instructions last sent. The address in that space depends on the "Set RAM Address" instructions parameters. Immediately before executing "Read Data", "Set CGRAM Address" or "Set DDRAM Address" must be executed.

The contents of the address counter are modified after each "Read Data", as determined by "Entry Mode Set". Display shift is not executed, independently of "Entry Mode Set".

SED1278

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–3 to +7.0	V
Supply voltage (2)*	V_1 to V_5	–0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature × time**	T_{sol}	260, 10	°C, s
Power dissipation	P_D	300	mW

Notes:
1. $V_{DD} > V_1 > V_2 > V_3 > V_4 > V_5 > V_{SS}$
2. A flat package product can become less resistant to moisture if exposed to extreme temperatures. When mounting this package on a printed circuit board, use a soldering technique which avoids excessive thermal loading of the package resin.
3. All voltages assume V_{SS} = 0 V.

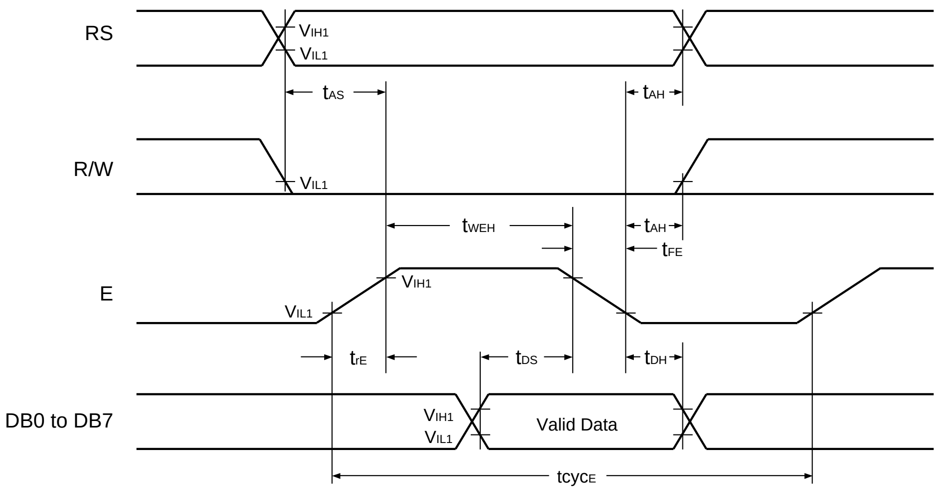
DC Characteristics

(V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Rating			Unit	Applicable Pins
			min	typ	max		
"H" level input voltage (1) (TTL)	V_{IH1}		2.0	—	V_{DD}	V	DB0 to DB7, RS, R/$\overline{W}$, E
"L" level input voltage (1) (TTL)	V_{IL1}		V_{SS}	—	0.8	V	
"H" level input voltage (2) (CMOS)	V_{IH2}		V_{DD}–1.0	—	V_{DD}	V	OSC1
"L" level input voltage (2) (CMOS)	V_{IL2}		V_{SS}	—	1.0	V	
"H" level output voltage (1) (TTL)	V_{OH1}	$-I_{OH}$ = 0.205 mA	2.4	—	—	V	DB0 to DB7
"L" level output voltage (1) (TTL)	V_{OL1}	I_{OL} = 1.6 mA	—	—	0.4	V	
"H" level output voltage (2) (CMOS)	V_{OH2}	$-I_{OH}$ = 0.04 mA	0.9V_{DD}	—	—	V	XSCL, LP, DO
"L" level output voltage (2) (CMOS)	V_{OL2}	I_{OL} = 0.04 mA	—	—	0.1V_{DD}	V	
Driver-on resistor (COM)	R_{COM}	$\lvert V_{COM}–V_n \rvert$ = 0.5 V	—	2	10	kΩ	COM1 to COM16
Driver-on resistor (SEG)	R_{SEG}	$\lvert V_{SEG}–V_n \rvert$ = 0.5 V	—	2.5	10	kΩ	SEG1 to SEG40
I/O leakage current	I_{IL}	V_{IN} = 0 to V_{DD}	—	—	1	µA	
Pull-up MOS current	–IP	V_{DD} = 5 V	50	125	250	µA	DB0 to CB7, RS, R/$\overline{W}$
Supply current	I_{OP}	Rf oscillation, from external clock V_{DD} = 5 V, f_{OSC} = f_{CP} = 270 kHz	—	0.5	0.8	mA	V_{DD}

AC Characteristics

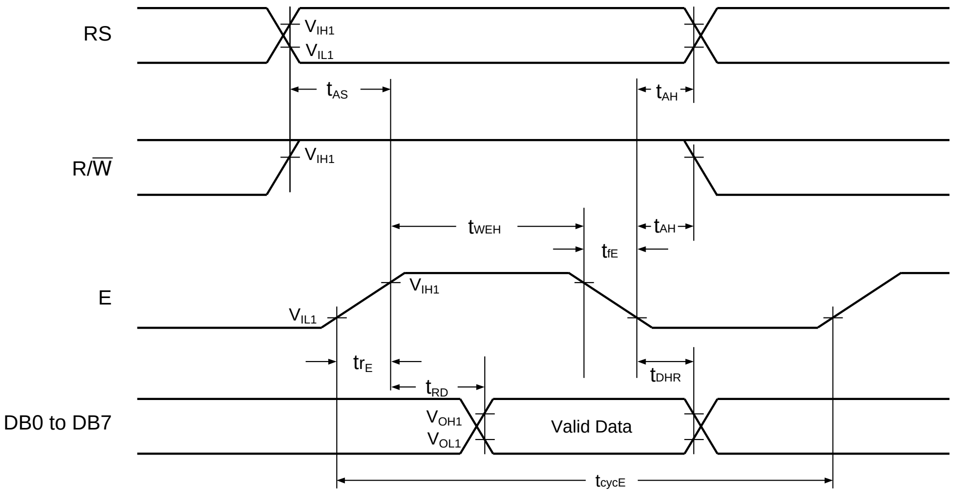
• MPU write cycle timing (write to SED1278)



(VDD = 5.0 V ± 10%, VSS = 0 V, Ta = –20 to 70°C)

Parameter	Symbol	Condition	Rating		Unit
			min	max	
Enable cycle time	t_{cycE}		500	—	ns
Enable “H” level pulsewidth	t_{WEH}		220	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	25	ns
RS, R/$\overline{W}$ setup time	t_{AS}		40	—	ns
RS, R/$\overline{W}$ address hold time	t_{AH}		10	—	ns
Data setup time	t_{DS}		60	—	ns
Write data hold time	t_{DH}		10	—	ns

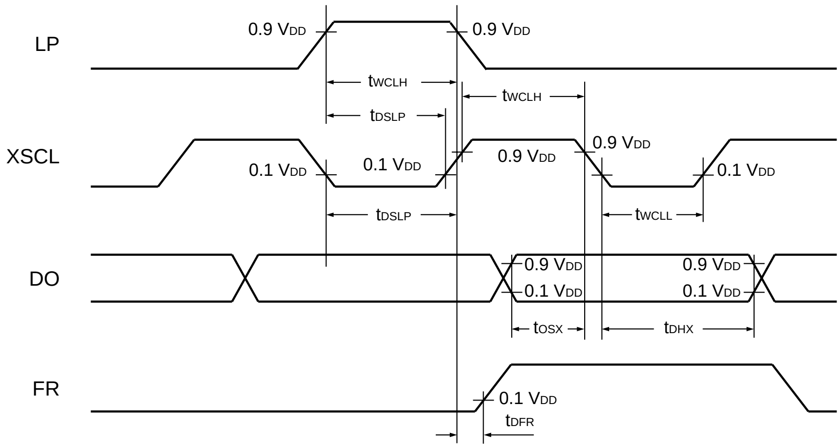
• MPU read cycle timing (read from SED1278)



(V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = –20 to 75°C)

Parameter	Symbol	Condition	Rating		Unit
			min	max	
Enable cycle time	t_{cycE}		500	—	ns
Enable “H” level pulsewidth	t_{WEH}		220	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	25	ns
RS, R/$\overline{W}$ setup time	t_{AS}		40	—	ns
RS, R/$\overline{W}$ address hold time	t_{AH}		10	—	ns
Read data setup time	t_{RD}	C_L = 100 pF	—	120	ns
Read data hold time	t_{DHR}		20	—	ns

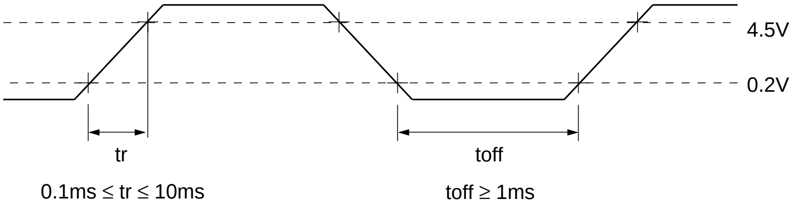
• External segment driver signal timing



(V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = –20 to 70°C)

Parameter	Symbol	Condition	Rating		Unit
			min	max	
Clock pulsewidth: High level	t_{WCLH}		0.8/2f_{OSC}	—	ns
Clock pulsewidth: Low level	t_{WCLL}		0.8/2f_{OSC}	—	ns
Latch pulse setup time	t_{DSLP}		0.7/2f_{OSC}	—	ns
Data setup time	t_{OSX}		0.7/2f_{OSC}	—	ns
Data hold time	t_{DHX}		0.7/2f_{OSC}	—	ns
FR delay	t_{DFR}		–1000	1000	ns

- Power-on reset timing



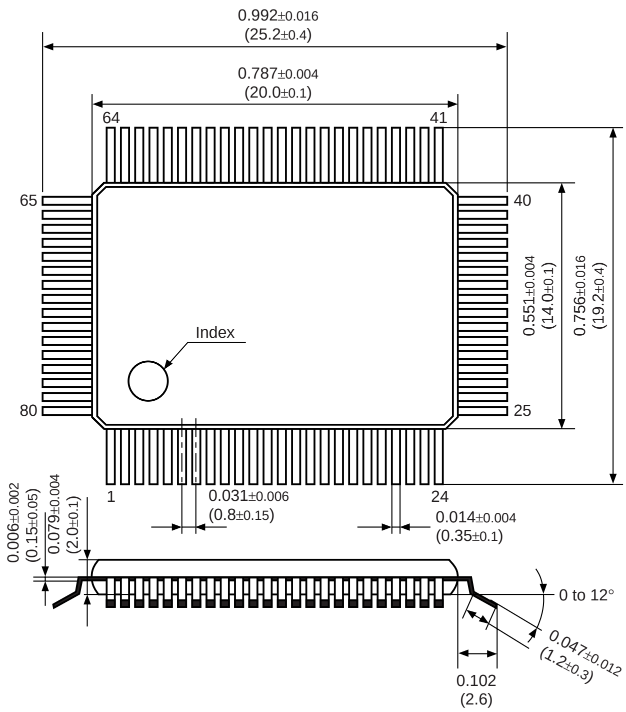
(Ta = –20 to 75 deg. C)

LCD Drive Voltages

Pin	Duty 1/8 or 1/11	Duty 1/16
V_1	3/4 (V_{DD} – V_5)	4/5 (V_{DD} – V_5)
V_2	2/4 (V_{DD} – V_5)	3/5 (V_{DD} – V_5)
V_3	2/4 (V_{DD} – V_5)	2/5 (V_{DD} – V_5)
V_4	1/4 (V_{DD} – V_5)	1/5 (V_{DD} – V_5)
V_5	V_5	V_5

Mechanical Specifications

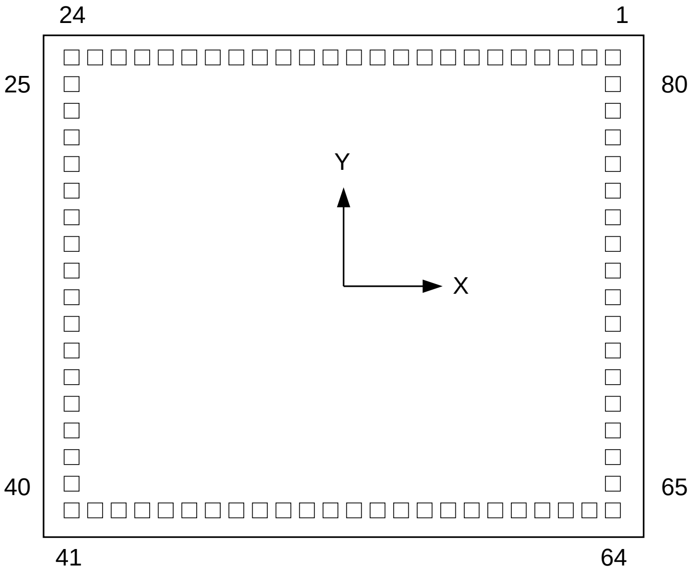
SED1278F Package Dimensions



SED1278

SED1278D Package Dimensions

Chip size:	4.50 mm × 3.67 mm
Chip thickness:	400 µm
Pad size:	109 µm × 109 µm
Pad pitch:	182 µm



Pad		X (μm)	Y (μm)
Number	Name		
1	SEG22	2087	1671
2	SEG21	1905	1671
3	SEG20	1723	1671
4	SEG19	1541	1671
5	SEG18	1359	1671
6	SEG17	1177	1671
7	SEG16	995	1671
8	SEG15	814	1671
9	SEG14	633	1671
10	SEG13	452	1671
11	SEG12	272	1671
12	SEG11	91	1671
13	SEG10	–91	1671
14	SEG9	–272	1671
15	SEG8	–452	1671
16	SEG7	–633	1671
17	SEG6	–814	1671
18	SEG5	–995	1671
19	SEG4	–1177	1671
20	SEG3	–1359	1671
21	SEG2	–1541	1671
22	SEG1	–1723	1671
23	GND	–1905	1671
24	OSC1	–2087	1671
25	OSC2	–2087	1365
26	V_1	–2087	1183
27	V_2	–2087	1001
28	V_3	–2087	819
29	V_4	–2087	637
30	V_5	–2087	455
31	LP	–2087	273
32	XSCL	–2087	91
33	V_{DD}	–2087	–91
34	FR	–2087	–273
35	DO	–2087	–455
36	RS	–2087	–637
37	R/$\overline{W}$	–2087	–819
38	E	–2087	–1001
39	DB0	–2087	–1183
40	DB1	–2087	–1365

Pad		X (μm)	Y (μm)
Number	Name		
41	DB2	–2087	–1671
42	DB3	–1905	–1671
43	DB4	–1723	–1671
44	DB5	–1541	–1671
45	DB6	–1359	–1671
46	DB7	–1177	–1671
47	COM1	–995	–1671
48	COM2	–814	–1671
49	COM3	–633	–1671
50	COM4	–452	–1671
51	COM5	–272	–1671
52	COM6	–91	–1671
53	COM7	91	–1671
54	COM8	272	–1671
55	COM9	452	–1671
56	COM10	633	–1671
57	COM11	814	–1671
58	COM12	995	–1671
59	COM13	1177	–1671
60	COM14	1359	–1671
61	COM15	1541	–1671
62	COM16	1723	–1671
63	SEG40	1905	–1671
64	SEG39	2087	–1671
65	SEG38	2087	–1365
66	SEG37	2087	–1183
67	SEG36	2087	–1001
68	SEG35	2087	–819
69	SEG34	2087	–637
70	SEG33	2087	–455
71	SEG32	2087	–273
72	SEG31	2087	–91
73	SEG30	2087	91
74	SEG29	2087	273
75	SEG28	2087	455
76	SEG27	2087	637
77	SEG26	2087	819
78	SEG25	2087	1001
79	SEG24	2087	1183
80	SEG23	2087	1365

OPERATION

The Busy Flag

The SED1278 takes between 10 and 410 clock cycles to execute instructions. During that period additional instructions should not be issued. The device is provided with a busy flag to let the user check the internal state of the chip. BF should be 0 before another instruction is issued.
If the busy flag is not checked between instructions the user must arrange for a guaranteed delay of more than the instruction execution time, before issuing the next instruction.

4-Bit MPU Interface

If a "System Set" instruction is issued with bit 4 set to 0, then the SED1278 will operate with a 4-bit MPU data bus interface.
If a 4-bit interface is used, the 8-bit instructions are written nibble by nibble; the high-order nibble being written first, followed by the low-order nibble. It is not necessary to check the busy flag between writing separate nibbles of individual instructions.
Reading the Busy Flag/Address Counter yields the high-order nibble first, followed by the low-order nibble.

System Initialization

Power-on reset

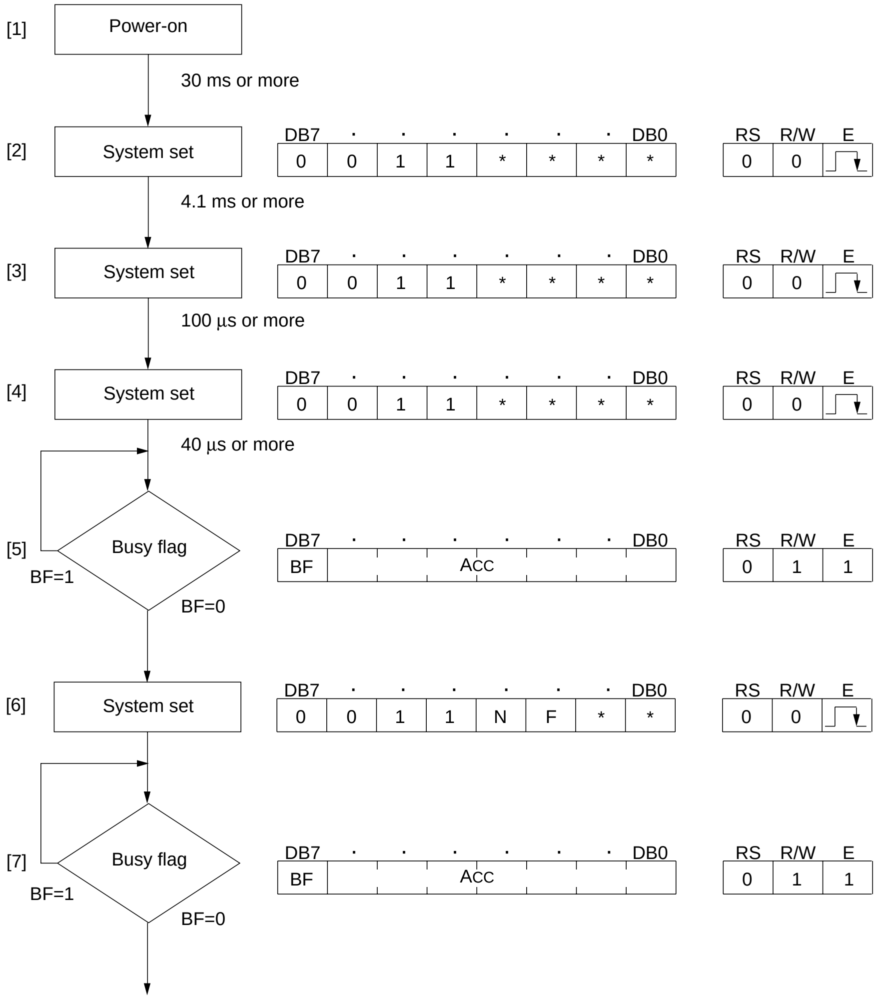
Although the SED1278 has no external reset input, it will automatically reset on system power-on. The sequence starts once $V_{DD} < 4.5$ V.
While the SED1278 is resetting the busy flag is set to 1. The reset takes about 3,750 clock cycles. For example if $f_{OSC} = 250$ kHz, the reset sequence takes about 30 ms.
Reset places the SED1278 in a state where

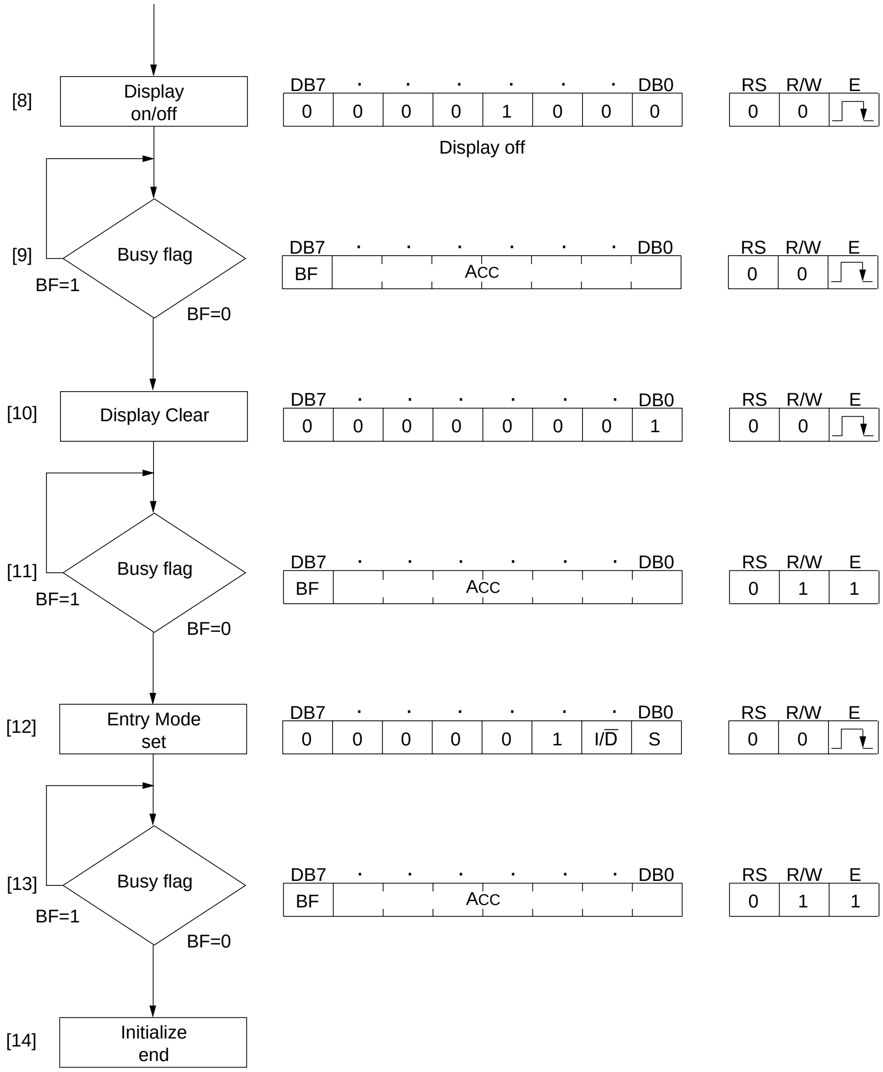
- the display is clear.
- the system configuration corresponds to
  - IF = 1: 8-bit MPU interface
  - N = 0: 1-line display
  - F = 0: 1/8 duty cycle
- the display configuration corresponds to
  - D = 0: Display off
  - C = 0: Cursor off
  - B = 0: Blink off
- the entry mode is set to
  - $I/\overline{D} = 1$: Increment
  - S = 1: No display shift

Software initialization

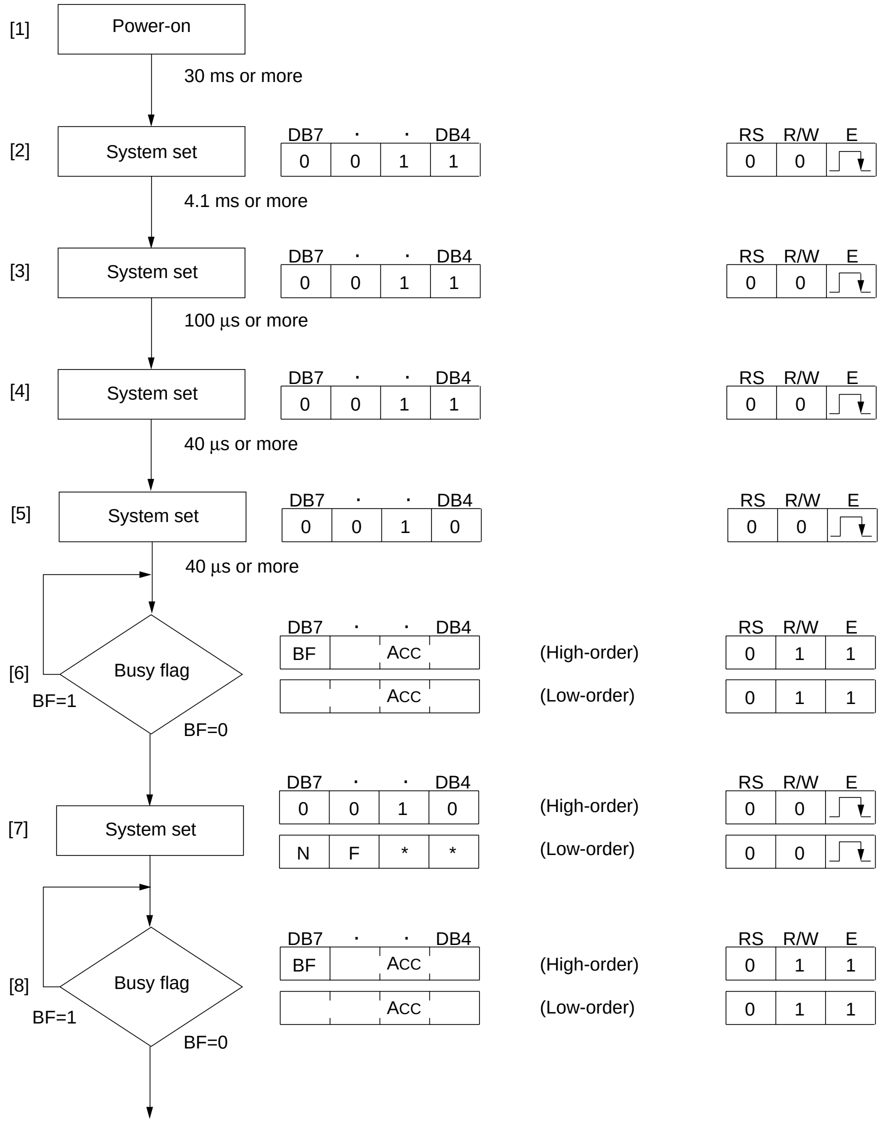
Initialization during power-on reset involves several unstable factors related to power-supply output fluctuations. For this reason it is strongly recommended that a software initialization sequence is followed.

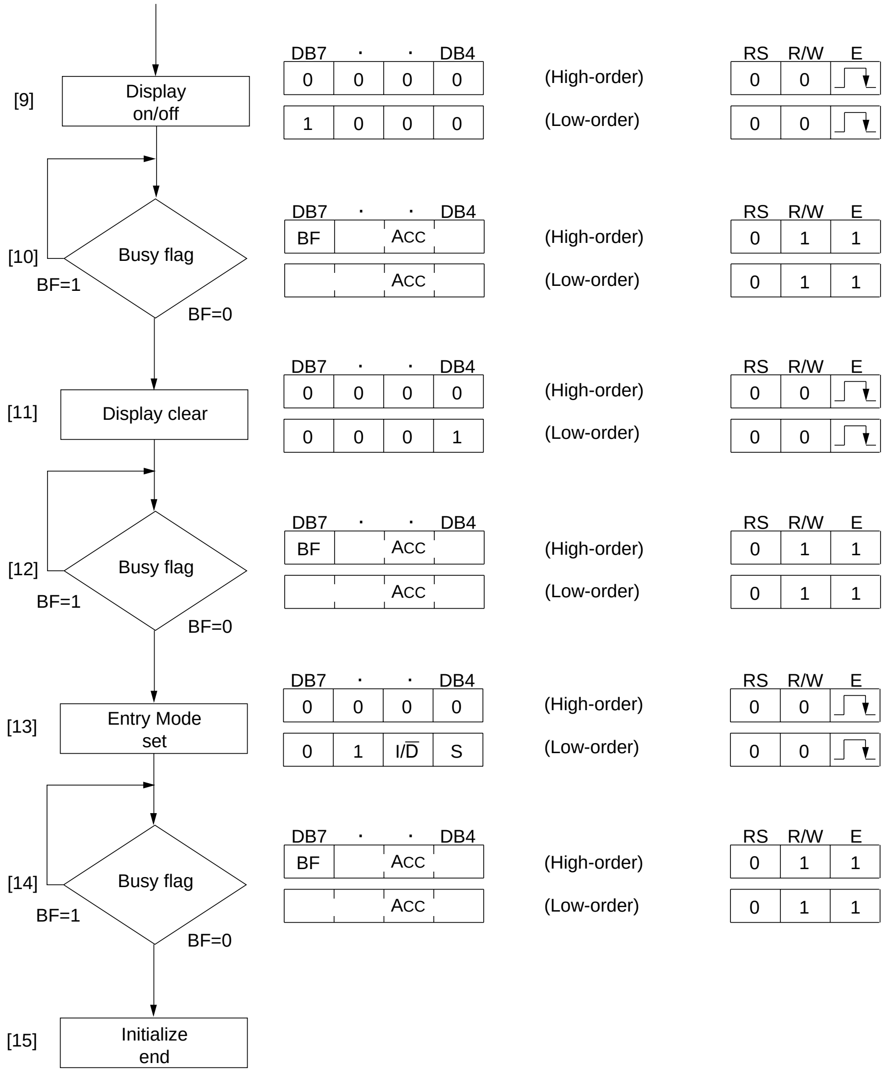
- Software Initialization (8-bit MPU bus, f_{OSC} = 250 kHz)




[8]
Display on/off
DB7 DB0
0 0 0 0 1 0 0 0
RS R/W E
0 0
Display off
[9]
Busy flag
BF=1
BF=0
DB7 DB0
BF ACC
RS R/W E
0 0
[10]
Display Clear
DB7 DB0
0 0 0 0 0 0 0 1
RS R/W E
0 0
[11]
Busy flag
BF=1
BF=0
DB7 DB0
BF ACC
RS R/W E
0 1 1
[12]
Entry Mode set
DB7 DB0
0 0 0 0 0 1 I/D S
RS R/W E
0 0
[13]
Busy flag
BF=1
BF=0
DB7 DB0
BF ACC
RS R/W E
0 1 1
[14]
Initialize end

• Software Initialization (4-bit MPU bus, fOSC = 250 kHz)




[9]
Display on/off
DB7 · · DB4
0 0 0 0 (High-order)
1 0 0 0 (Low-order)
RS R/W E
0 0
0 0
[10]
Busy flag
BF=1
BF=0
BF ACC (High-order)
ACC (Low-order)
0 1 1
0 1 1
[11]
Display clear
0 0 0 0 (High-order)
0 0 0 1 (Low-order)
[12]
Busy flag
[13]
Entry Mode set
0 0 0 0 (High-order)
0 1 I/D̄ S (Low-order)
[14]
Busy flag
[15]
Initialize end

THE CHARACTER GENERATOR

Character Generator ROM (CGROM)

The SED1278 contains a 240 character, masked CGROM. Each character is 5×10 pixels, for 1/11 duty cycle compatibility. Refer to Appendix A for available codes and their corresponding fonts.

Because the CGROM is masked, customers may arrange to have their own CGROM masks made.

A custom mask allows the user to have

- their own character set.
- a character set of up to 256 characters.

Please contact the SEIKO EPSON Marketing Department for further information.

If a custom CGROM is used, two things should be noted.

1. The “Clear Display” instruction relies on the character whose code is 20H being a blank.
2. If more than 240 ROMed characters are specified, then the number of CGRAM characters available is correspondingly reduced. The physical RAM space is still available, and is available for use as memory, however it will no longer have an associated character code.
3. The character ROM implemented in a particular chip is indicated by a two character suffix attached to the device number, for example SED1278F0A.

Character Generator RAM (CGRAM)

The SED1278 has 64 bytes of CGRAM, allowing the user to program up to 8 characters.

5×8 pixel font (1/8 or 1/16 duty cycle)

The maximum character height is 8 pixels, however if a cursor is used row 7 should be all zeros. 8 such characters are available to the user.

The CGRAM address is made up of the following components.

- The least significant three bits, a_2 to a_0, specify the row number of the character data.
- Bits a_5 to a_3 are made up of the least significant three bits of the character code.
- The most significant bit, a_7, is ignored.
  Figure 1 shows an example 5×8 pixel font.

CGRAM address						CGRAM data (Character pattern)							
A5	·	·	·	·	A0	DB7	·	·	·	·	·	·	DB0
0	0	0	0	0	0	*	*	*	0	0	0	0	1
0	0	0	0	0	1	*	*	*	0	0	0	0	1
0	0	0	0	1	0	*	*	*	0	1	0	0	1
0	0	0	0	1	1	*	*	*	1	1	1	1	1
0	0	0	1	0	0	*	*	*	0	1	0	0	0
0	0	0	1	0	1	*	*	*	0	0	0	0	0
0	0	0	1	1	0	*	*	*	0	0	0	0	0
0	0	0	1	1	1	*	*	*	0	0	0	0	0

Figure 1 A 5×8 Pixel Font

5×11 pixel font (1/11 duty cycle)

The maximum character height is 11 pixels, however if a cursor is used row 10 must be left blank.

The SED1278 requires that, although the maximum character height is 11 rows, each character is allocated 16 rows (bytes) of address space. The last five bytes are ignored.

The CGRAM address is made up of the following components.

- The least significant 4 bits, a_3 to a_0, specify the row number of the character data.
- Bits a_5 and a_4 correspond to bits 2 and 3, respectively, of the character code.
- The most significant bit, a_7, is ignored.

Figure 2 shows an example 5×11 pixel font.

CGRAM address						CGRAM data							
A5	·	·	·	·	A0	DB7	·	·	·	·	·	·	DB0
0	0	0	0	0	0	*	*	*	0	0	0	0	1
0	0	0	0	0	1	*	*	*	0	0	0	0	1
0	0	0	0	1	0	*	*	*	0	0	0	0	1
0	0	0	0	1	1	*	*	*	0	0	1	0	1
0	0	0	1	0	0	*	*	*	0	1	0	0	1
0	0	0	1	0	1	*	*	*	1	1	1	1	1
0	0	0	1	1	0	*	*	*	0	1	0	0	0
0	0	0	1	1	1	*	*	*	0	0	1	0	0
0	0	1	0	0	0	*	*	*	0	0	0	0	0
0	0	1	0	0	1	*	*	*	0	0	0	0	0
0	0	1	0	1	0	*	*	*	0	0	0	0	0
0	0	1	0	1	1	*	*	*	*	*	*	*	*
0	0	1	1	0	0	*	*	*	*	*	*	*	*
0	0	1	1	0	1	*	*	*	*	*	*	*	*
0	0	1	1	1	0	*	*	*	*	*	*	*	*
0	0	1	1	1	1	*	*	*	*	*	*	*	*

Figure 2 A 5×11 Pixel Font

LCD INTERFACE

LCD Drive Voltages

The SED1278 generates segment and common drive signals using the voltages supplied to pins V_1, V_2, V_3, V_4 and V_5. The voltage levels at these pins depend on the duty cycle of the display. The specifications of these voltages.

The simplest way of producing these voltages is to use a resistive dividing network.

Figures 3 and 4 show examples of networks for 1/8, or 1/11, and 1/16 duty cycles respectively.

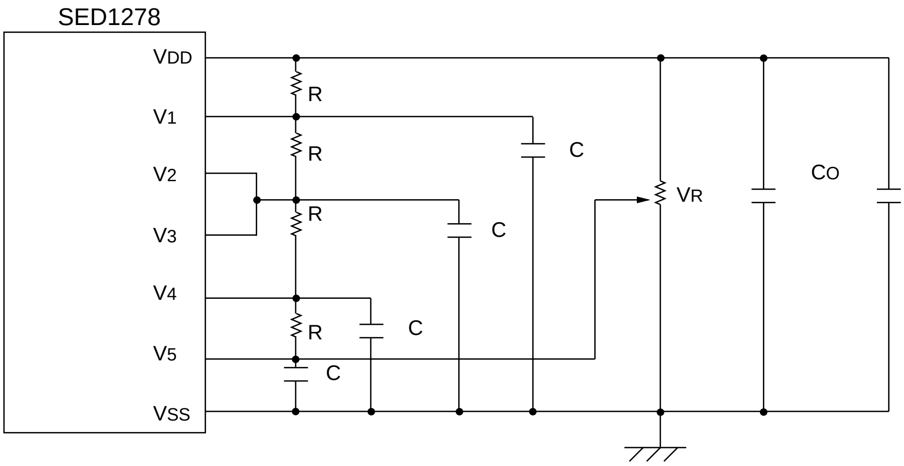


Figure 3 LCD Drive Voltage Network – 1/8 or 1/11 Duty Cycle

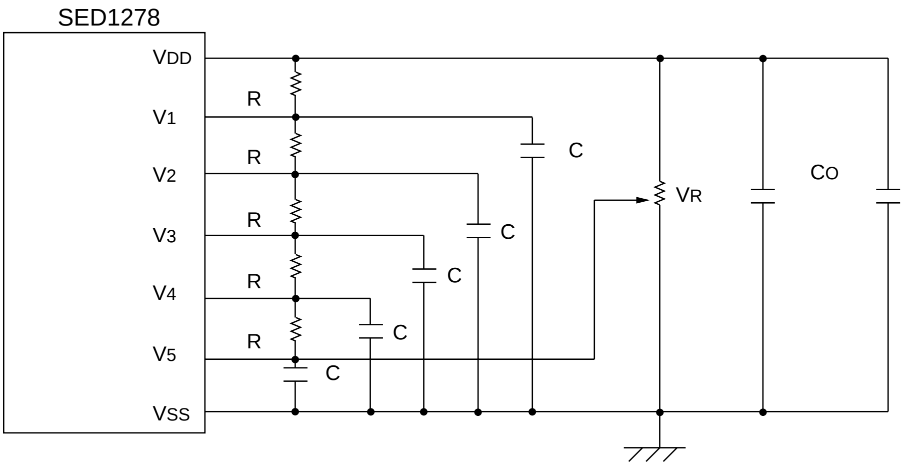


Figure 4 LCD Drive Voltage Network – 1/16 Duty Cycle

Notes: 1. V_5 is set using a potentiometer and (V_{DD}–V_{SS}).

2. The power supply to the SED1278 should be bypassed with a capacitor, C_O, of at least 0.1 μF placed as close to the chip as possible.

LCD Drive Signal Waveforms

The segment and common drive waveforms generated by the SED1278, for various duty cycle ratios, are shown in figures 5, 6 and 7.

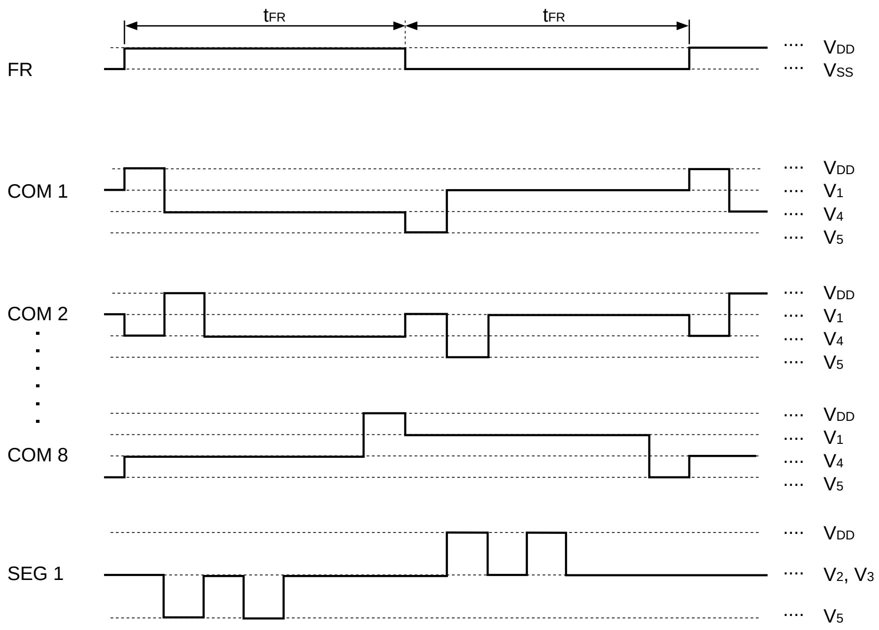


Figure 5 1/8 Duty Cycle Drive Waveforms

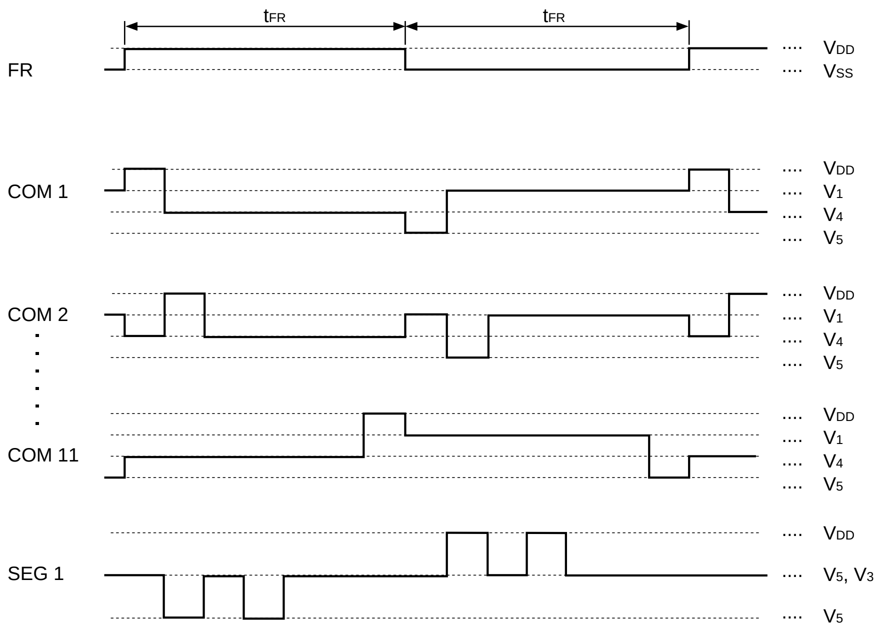


Figure 6 1/11 Duty Cycle Drive Waveforms

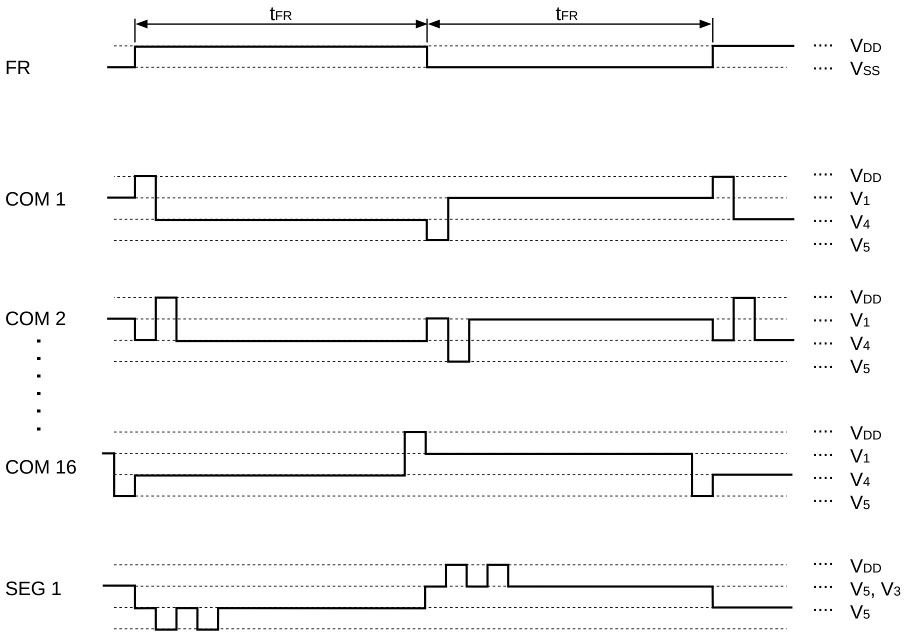
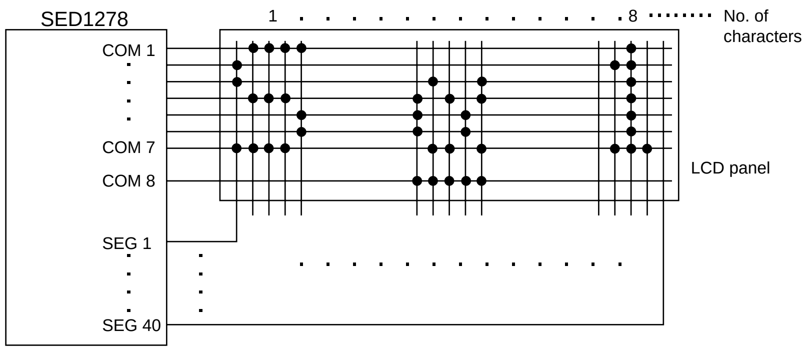


Figure 7 1/16 Duty Cycle Drive Waveforms

LCD Interface Configurations

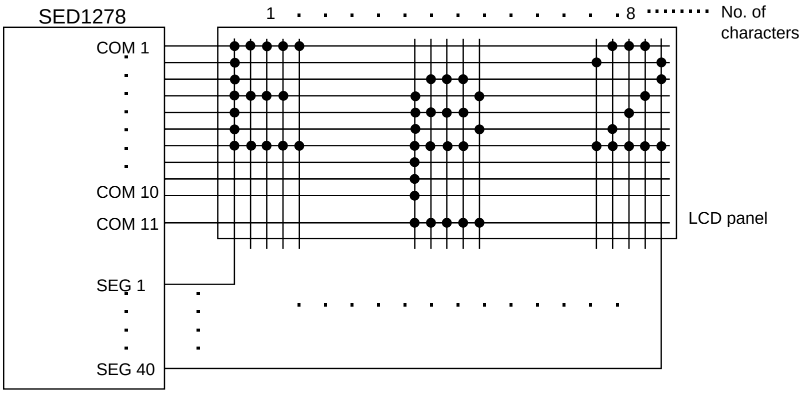
The SED1278 has 16 common and 40 segment drive outputs, enabling the chip to drive up to 16 characters by itself. The drive capability can be expanded to 80 characters, by using SED1181FLA external segment drivers.

- 1 line
- 8 characters
- 5×7 pixels + cursor
- 1/8 duty cycle
- System set: N = 0, F = 0

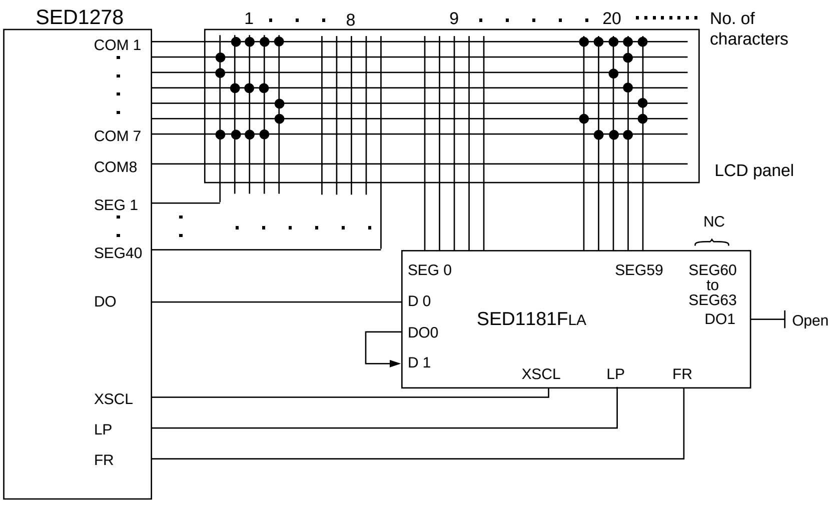


SED1278

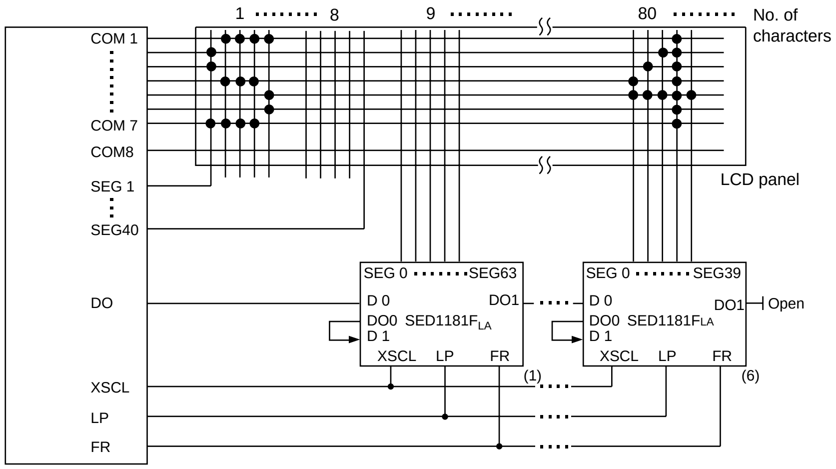
- 1 line
- 8 characters
- 5×10 pixels + cursor
- 1/11 duty cycle
- System set: N = 0, F = 1



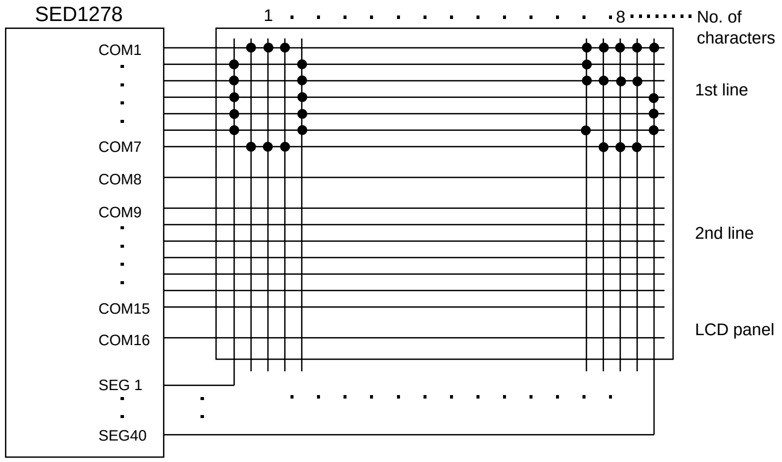
- 1 line
- 20 characters
- 5×7 pixels + cursor
- 1/8 duty cycle
- System set: N = 0, F = 0



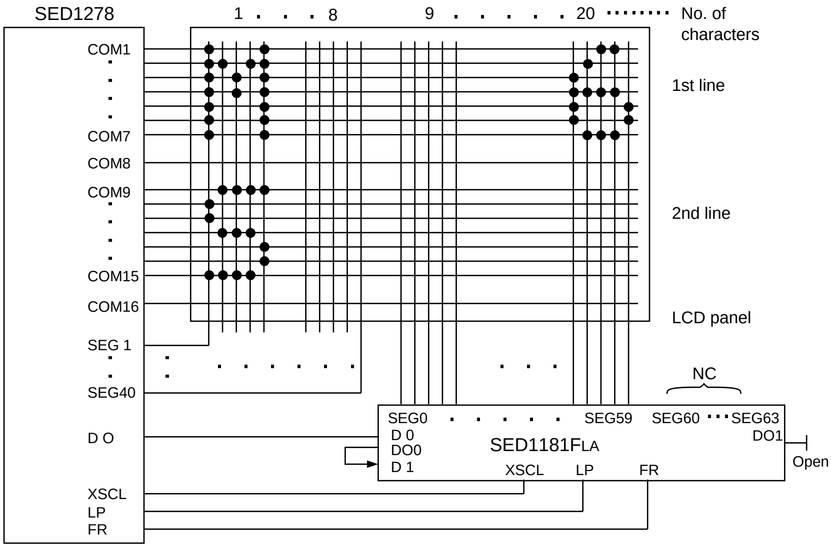
- 1 line
- 80 characters
- 5×7 pixels + cursor
- 1/8 duty cycle
- System set: N = 0, F = 0



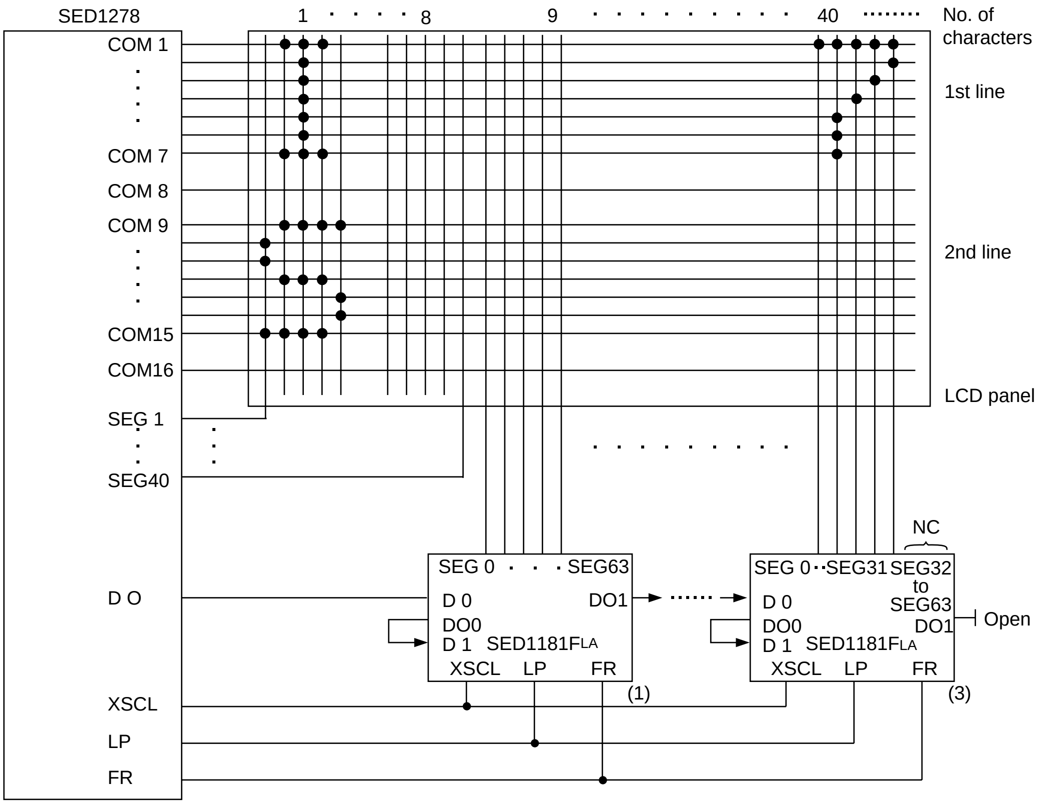
- 2 line
- 8 characters
- 5×7 pixels + cursor
- 1/16 duty cycle
- System set: N = 1, F = don't care



- 2 line
- 20 characters
- 5×7 pixels + cursor
- 1/16 duty cycle
- System set: N = 1, F = don't care



- 2 line
- 40 characters
- 5×7 pixels + cursor
- 16 duty cycle
- System set: N = 1, F = don't care



MPU INTERFACE

The SED1278 has selectable 8- or 4-bit MPU interface. An example of a typical 8-bit MPU interface is shown figure 8.

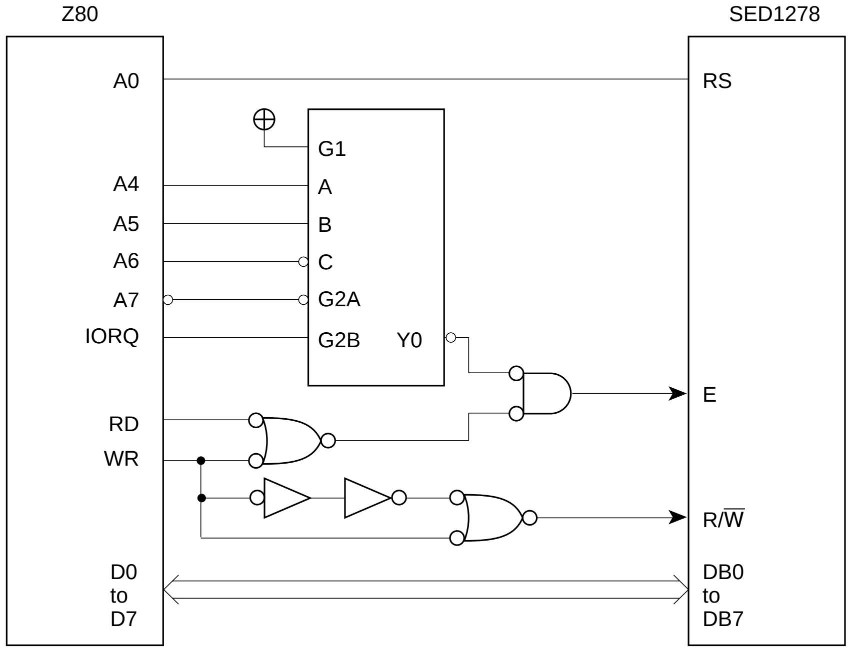


Figure 8 Interfacing the SED1278 to the Zilog Z80®

COMPARISON WITH HD44780 BY HITACHI

Item	HD44780 (Hitachi)	SED1278
Data display RAM	80 bytes	←
Character generator ROM Character font	192 types 5 × 7: 160 types 5 × 10: 32 types	240 types 5 × 10: 240 types
Character generator RAM	64 bytes	←
LCD drive output	16 common driver outputs 40 segment drive outputs	←
Character font (with cursor)	5 × 8 dots (1/8 and 1/16 duty) 5 × 11 dots (1/1 duty)	←
Conversion to duty	1/8, 1/11, 1/16	←
LCD drive voltage (V_{DD}–V_5)	Max. 13.5 V Min. 4.6 V	Max. 1 V_{DD} Min. 3 V
LCD drive waveform	Waveform A (Single frame AC drive)	Waveform D (Dual frame AC drive)
E pulse width	450 nsec	220 nsec
Timing to change the address counter subsequent to CGRAM and DDRAM data writing and reading	The contents of address counter are determined 1.5 clock after release of busy state (6 microseconds at f_{OSC} = 250 kHz).	The contents of address counter are determined immediately after release of busy state.
No. of instructions	11	←
Reset terminal	Not provided	←
Chip selector terminal	Not provided	←
Power-on reset terminal	Provided	←
Extension segment driver	Hitachi HD44100: 40 outputs SED1181FLA: 64 outputs	←
Package	80-pin plastic flat package	←
Pin layout		Pin compatible

APPENDIX A: CHARACTER CODES AND FONTS

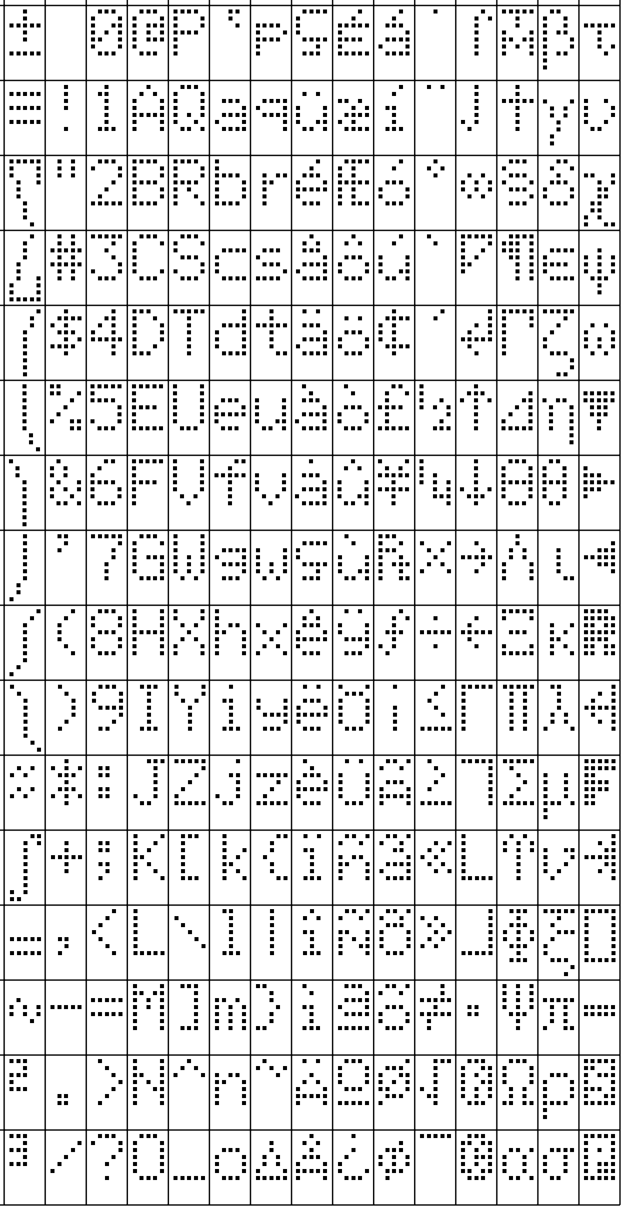
SED1278F0A/SED1278D0A

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	CG RAM (1)			0	@	P	`	p				ｰ	ﾀ	ﾐ	α	p
	1	CG RAM (2)		!	1	A	Q	a	q			｡	ｱ	ﾁ	ﾑ	ä	q
	2	CG RAM (3)		"	2	B	R	b	r			｢	ｲ	ﾂ	ﾒ	β	θ
	3	CG RAM (4)		#	3	C	S	c	s			｣	ｳ	ﾃ	ﾓ	ε	∞
	4	CG RAM (5)		$	4	D	T	d	t			､	ｴ	ﾄ	ﾔ	μ	Ω
	5	CG RAM (6)		%	5	E	U	e	u			･	ｵ	ﾅ	ﾕ	σ	ü
	6	CG RAM (7)		&	6	F	V	f	v			ｦ	ｶ	ﾆ	ﾖ	ρ	Σ
	7	CG RAM (8)		'	7	G	W	g	w			ｧ	ｷ	ﾇ	ﾗ	g	π
	8	CG RAM (1)		(	8	H	X	h	x			ｨ	ｸ	ﾈ	ﾘ	√	x̄
	9	CG RAM (2)		)	9	I	Y	i	y			ｩ	ｹ	ﾉ	ﾙ	$^{-1}$	y
	A	CG RAM (3)		*	:	J	Z	j	z			ｪ	ｺ	ﾊ	ﾚ	j	千
	B	CG RAM (4)		+	;	K	[	k	{			ｫ	ｻ	ﾋ	ﾛ	ˣ	万
	C	CG RAM (5)		,	<	L	¥	l	|			ｬ	ｼ	ﾌ	ﾜ	¢	円
	D	CG RAM (6)		-	=	M	]	m	}			ｭ	ｽ	ﾍ	ﾝ	£	÷
	E	CG RAM (7)		.	>	N	^	n	→			ｮ	ｾ	ﾎ	ﾞ	ñ	
	F	CG RAM (8)		/	?	O	_	o	←			ｯ	ｿ	ﾏ	ﾟ	ö	█

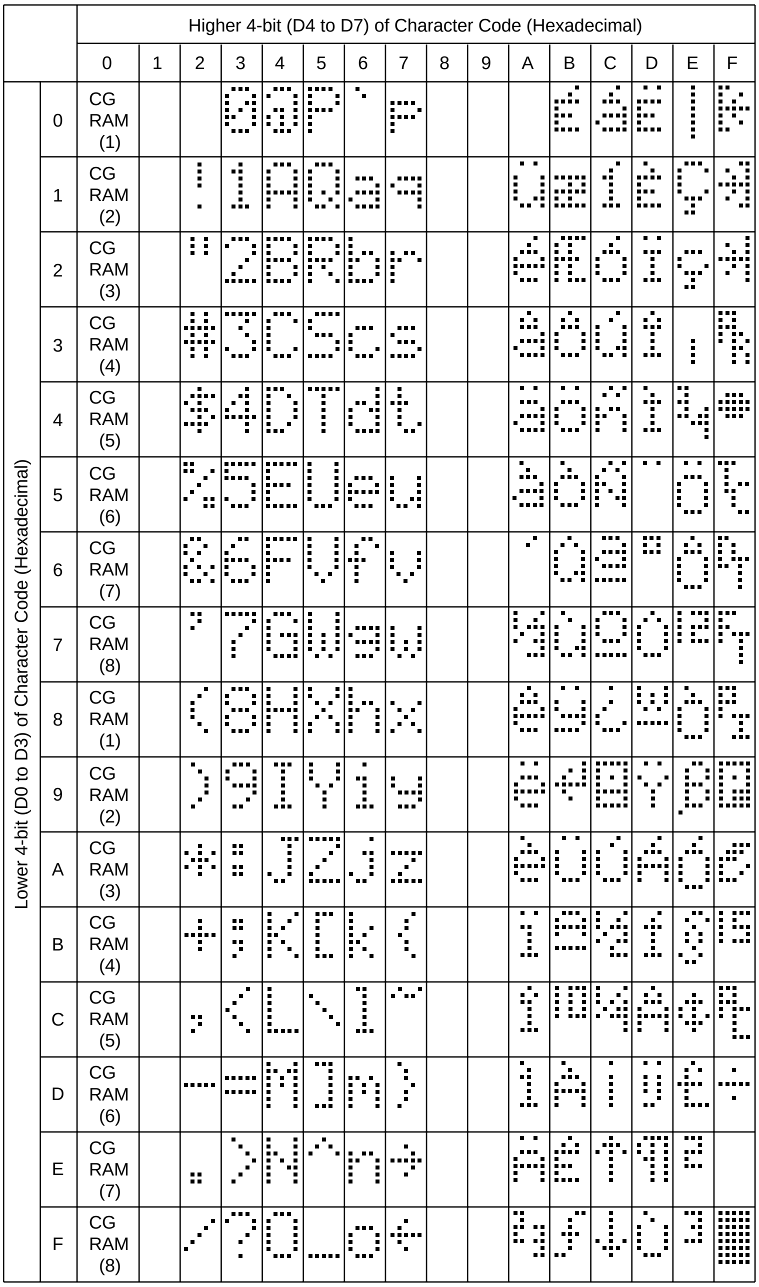
SED1278F0B/SED1278D0B

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal) / Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)

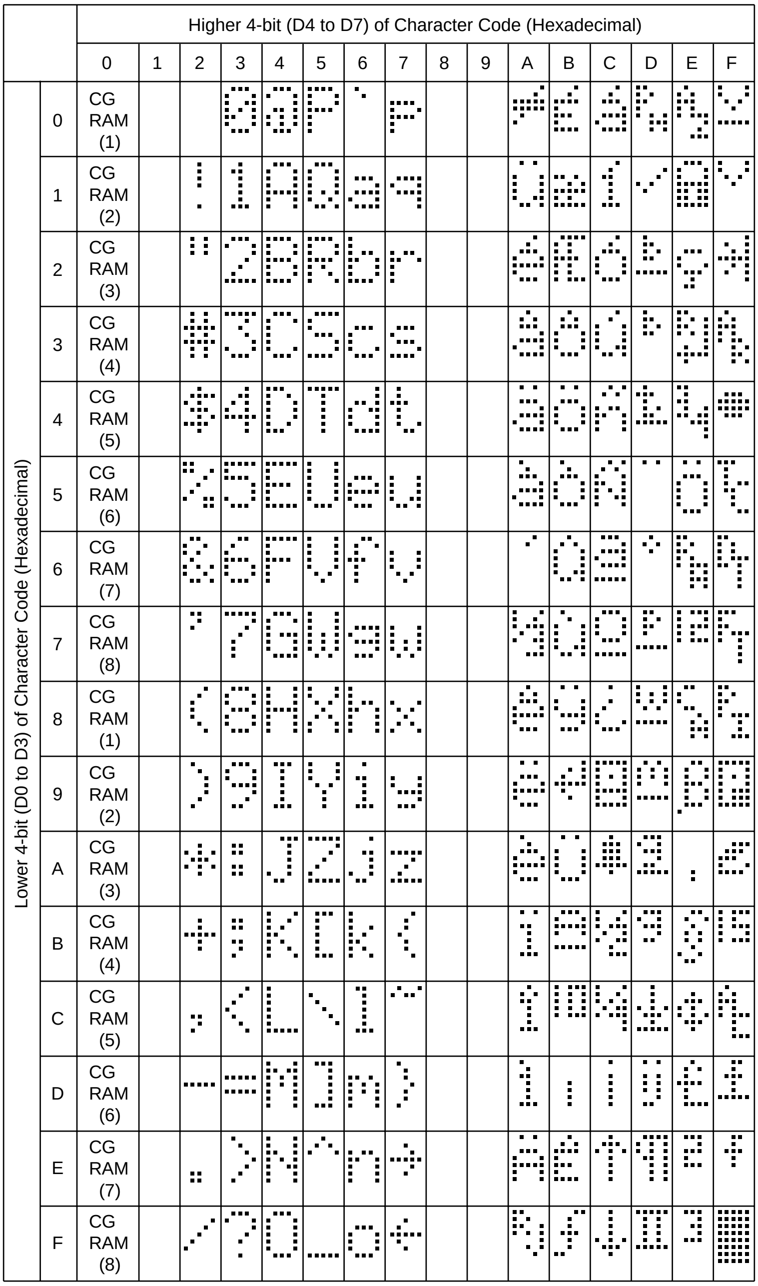
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															



SED1278F0C/SED1278D0C



SED1278F0E/SED1278D0E

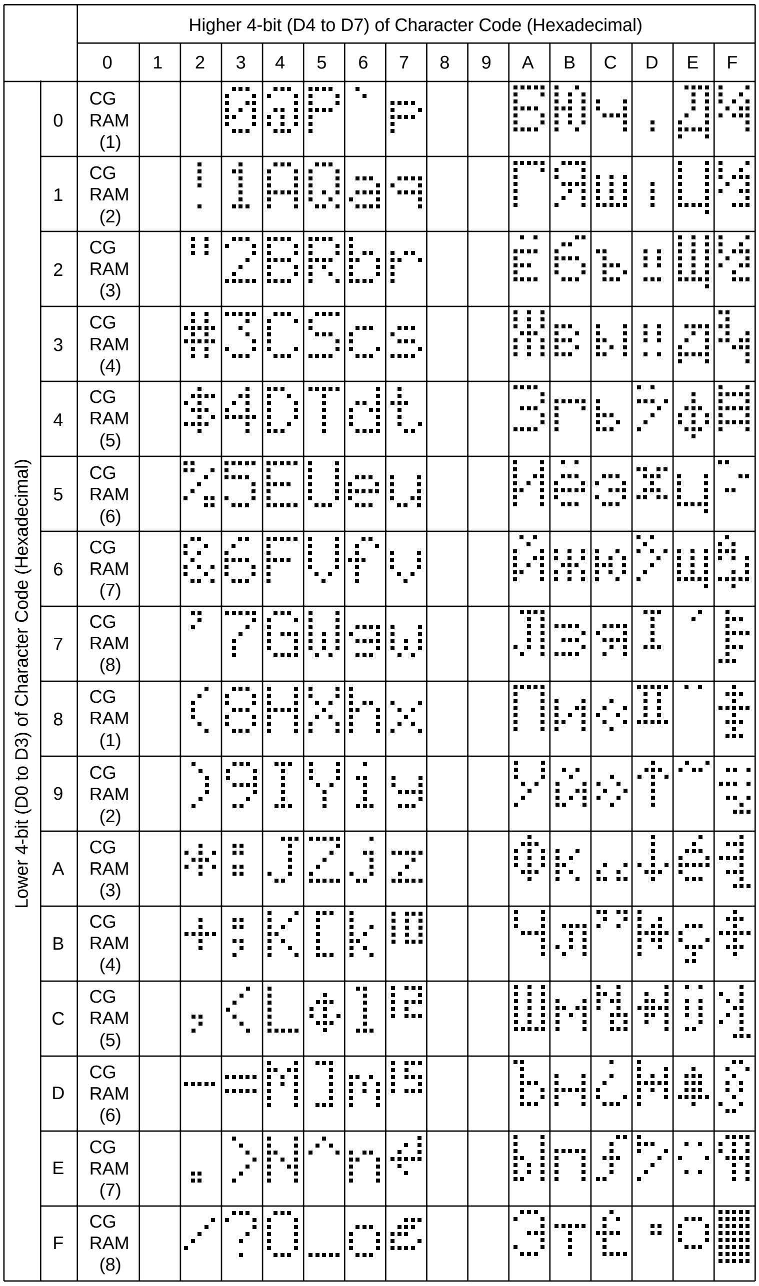


SED1278

SED1278F0G/SED1278D0G



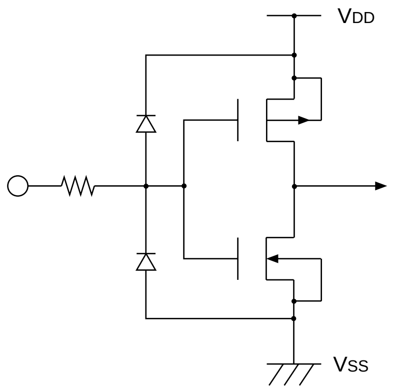
SED1278F0H/SED1278D0H



APPENDIX B: PIN CONSTRUCTION

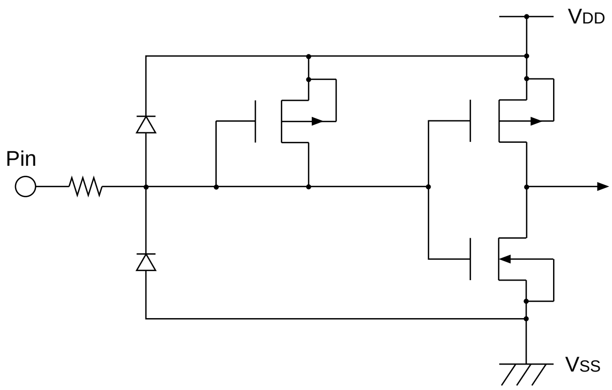
Input Pin Type 1

- E
- OSC1



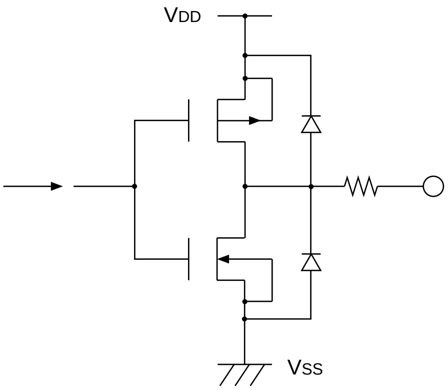
Input Pin Type 2

- RS
- R/$\overline{W}$



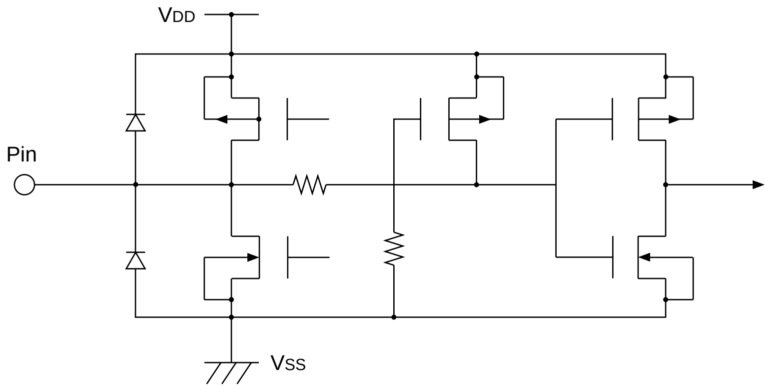
Output Pin

- OSC2
- XSCL, LP, FR, DO



I/O Pin

- DB0 to DB7



SED1280
Dot-Matrix LCD Controller

Technical Manual

Contents

OVERVIEW

The SED1280 is an enhanced version of the SED1278 dot-matrix LCD controller. In addition to the SED1278 functionality, the SED1280 also incorporates a key-matrix controller, LED drivers and additional input and output ports.

The SED1280 comprises the SED1278 core, display data and character generator RAM, character generator ROM, LCD segment and common drivers, LED-matrix and key-matrix inputs and outputs, extended input and output ports and a serial microcontroller interface. The SED1280 operates from a 5 V supply and is available in 100-pin QFP5s.

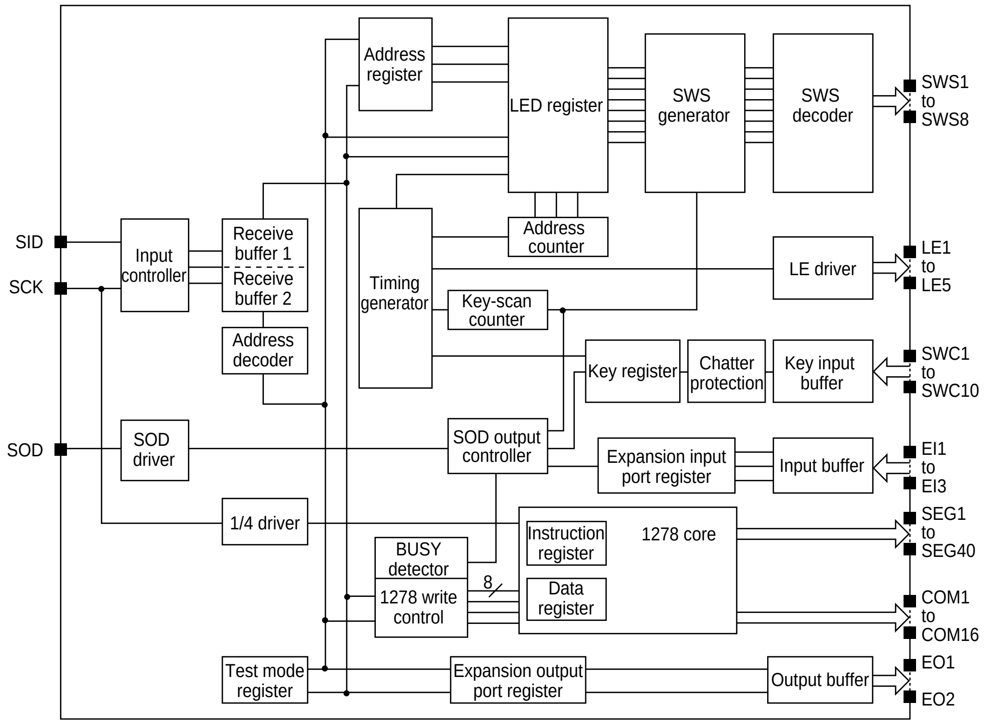
FEATURES

- LCD controller
  - 80-byte, 80-character display data RAM
  - Character generator ROM
    - 240, 5 × 10-pixel characters
  - Character generator RAM
    - 64 bytes
    - Eight selectable 5 × 7-pixel or 5 × 8-pixel characters.
    - Four selectable 5 × 10-pixel or 5 × 11-pixel characters
  - Outputs
    - 40 segment outputs
    - 16 common outputs
  - Modes

Display type	Duty	Number of SED1181F common drivers	Character configuration (columns × rows)
One line	1/8 or 1/11	0	8 × 1
		6	80 × 1
Two lines	1/16	0	8 × 2
		3	40 × 4

- Key matrix scan controller
  - Eight key-scan outputs
  - Ten key-scan inputs
  - Can control an 8 × 10 key matrix.
- LED controller
  - Five LED driver outputs
  - Eight LED driver commons
  - Can control a 5 × 8-LED matrix
- I/O ports
  - Three input ports
  - Two output ports
- Serial microcontroller interface
- Single 5 V supply
- 100-pin QFP5

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	VSS	Ground
2 to 6	V1 to V5	LCD controller power supply inputs
7	LP	Data latch pulse output
8	XSCL	Data transfer clock
9	VDD	5 V supply
10	FR	LCD AC controller output
11	DO	Serial data output
12	SCK	1 MHz system clock input
13	SID	Serial data input
14	RST	Reset input
15 to 24	SWC10 to SWC1	Key-scan inputs
25 to 30, 32, 33	SWS8 to SWS1	Multiplexed key-scan and LED output ports
34 to 36	EI3 to EI1	Expanded input ports
37 to 41	LE5 to LE1	LED controller outputs
42	SOD	Key- and expanded-input port status serial data output
43, 44	EO2, EO1	Expanded output ports
45 to 60	COM1 to COM16	Common driver outputs
61 to 100	SEG40 to SEG1	Segment driver outputs

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
	V_1 to V_5	–0.3 to V_{DD}+0.3	V
Input voltage range	V_I	–0.3 to V_{DD}+0.3	V
Operating temperature range	T_{opg}	–20 to 75	°C
Storage temperature range	T_{stg}	–65 to 150	°C

Note: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{SS} = 0$ V

Recommended Operating Conditions

Ta = 25°C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	4.5 to 5.5	V

DC Electrical Characteristics

V_{DD} = 5.0 V, V_{SS} = 0 V, Ta = –20 to 75°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{OP}		–	–	1	mA
SCK and SID LOW-level input voltage	V_{IL1}		–	–	0.8	V
EI1 to EI3 LOW-level input voltage	V_{IL2}		Vss	–	1.0	V
SCK and SID HIGH-level input voltage	V_{IH1}		2.0	–	–	V
EI1 to EI3 HIGH-level input voltage	V_{IH2}		V_{DD}–1.0	–	V_{DD}	V
EI1 to EI3 hysteresis voltage	V_{HYS}		1	–	–	V
XSCL, LP and DO LOW-level output voltage	V_{OL1}	I_{OL} = 0.04 mA	–	–	0.1V_{DD}	V
SWS1 to SWS8 LOW-level output voltage	V_{OL2}	I_{OL} = 25 mA	–	–	1.25	V
LE1 to LE5 LOW-level output voltage	V_{OL3}	I_{OL} = 2.0 mA	–	–	0.4	V
SOD, EO1 and EO2 LOW-level output voltage	V_{OL4}	I_{OL} = 2.0 mA	–	–	0.4	V
XSCL, LP and DO HIGH-level output voltage	V_{OH1}	I_{OH} = –0.04 mA	0.9V_{DD}	–	–	V
SWS1 to SWS8 HIGH-level output voltage	V_{OH2}	I_{OH} = –200 µA	4.0	–	–	V
LE1 to LE5 HIGH-level output voltage	V_{OH3}	I_{OH} = –200 µA	2.4	–	–	V
SOD, EO1 and EO2 HIGH-level output voltage	V_{OH4}	I_{OH} = –200 µA	2.4	–	–	V
SWC1 to SWC10 pull-up resistance	R_{UP1}		5	10	20	kΩ
RST pull-up resistance	R_{UP2}		50	100	200	kΩ
COM1 to COM16 driver ON resistance	R_{COM}	IV_{SEG}–VnI = 0.5 V	–	2	10	kΩ
SEG1 to SEG40 driver ON resistance	R_{SEG}	IV_{SEG}–VnI = 0.5 V	–	2.5	10.0	kΩ
SCK frequency	f_{SCK}		0.5	1.0	1.4	MHz
SCK duty cycle	Duty		45	50	55	%
SCK rise time	t_r		–	–	200	ns
SCK fall time	t_f		–	–	200	ns
SWC1 to SEC10 input debounce time	t_{KIN}		16	–	–	µs
SWS1 to SWS8 instantaneous output current	I_{SWS}		–	–	25	mA
SWS1 to SWS8 total output current	ΣI_{SWS}		–	–	100	mA
LCD driver output voltage	V_{LCD}	V_{LCD} = V_{DD}–V5	3.0	–	V_{DD}	V

Latch-up endurance

V_{DD} = 5 V, Ta = 25°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input DC trigger current	I_{TI}		–40	–	40	mA
Output DC trigger current	I_{TO}		–40	–	40	mA

Static breakdown resistance

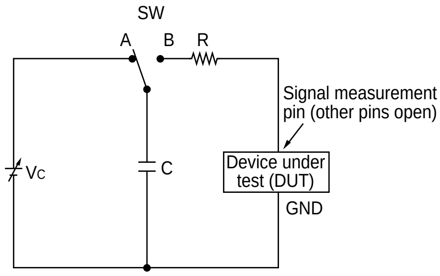
V_{DD} = 5 V, Ta = 25°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input terminal breakdown voltage	V_{SI}	C = 200 pF, R = 0 Ω	–250	–	250	V
Output terminal breakdown voltage	V_{SO}	C = 200 pF, R = 0 Ω	–250	–	250	V
V_{DD}, V_{SS} and V_1 to V_5 breakdown voltage	V_S	C = 200 pF, R = 0 Ω	–250	–	250	V

Measurement conditions

The measurement circuit is shown in the following figure. The switch is in position A until capacitor C charges to V_C volts. It then switches to position B and the capacitor discharges through the device under test (DUT), applying a surge voltage to the test pin. All other pins are left open.

The supply voltages, V_C, increases in 50 V steps from 50 V to a maximum of 1 kV, or until the device breaks down. Breakdown has occurred if the leakage current between the test pin and the GND pin increases by 0.1 μA when the absolute maximum rated voltage is applied to the test pin.

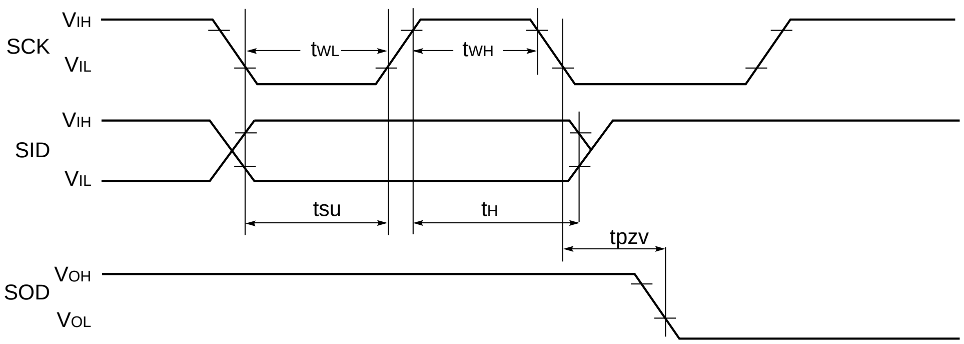


AC Electrical Characteristics

Serial data timing

V_{DD} = 5 V, V_{SS} = 0 V, Ta = –20 to 75°C

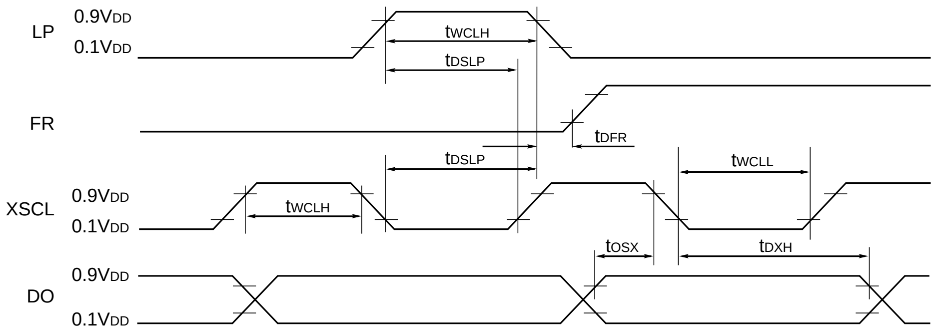
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
SCK LOW-level pulsewidth	t_{WL}		0.35	–	0.65	μs
SCK HIGH-level pulsewidth	t_{WH}		0.35	–	0.65	μs
Data setup time	t_{SU}		200	–	–	ns
Data hold time	t_H		200	–	–	ns
Output delay time	t_{PZY}		–	–	200	ns



Expanded segment output timing

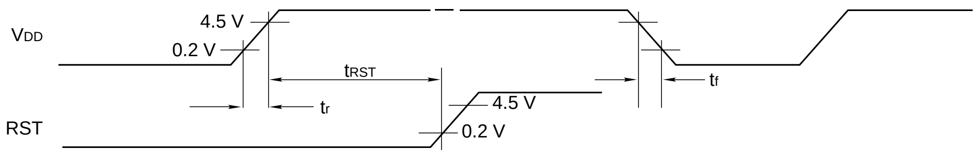
V_{DD} = 5.0 V, V_{SS} = 0 V, Ta = –20 to 75°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LP and XSCL LOW-level pulsewidth	t_{WCLL}		0.8×2/fc	–	–	ns
LP and XSCL HIGH-level pulsewidth	t_{WCLH}		0.8×2/fc	–	–	ns
XSCL to LP and LP to XSCL setup time	t_{DSLP}		0.7×2/fc	–	–	ns
DO to XSCL setup time	t_{OSX}		0.7×2/fc	–	–	ns
XSCL to DO hold time	t_{DHX}		0.7×2/fc	–	–	ns
FR delay time	t_{DFR}		–1	–	1	μs



Reset timing

V_{DD} = 5.0 V, V_{SS} = 0 V, Ta = –20 to 75°C



Note: 0.1 ms ≤ t_r ≤ 10 ms, t_f ≥ 1 ms, t_{RST} ≥ 30 ms.

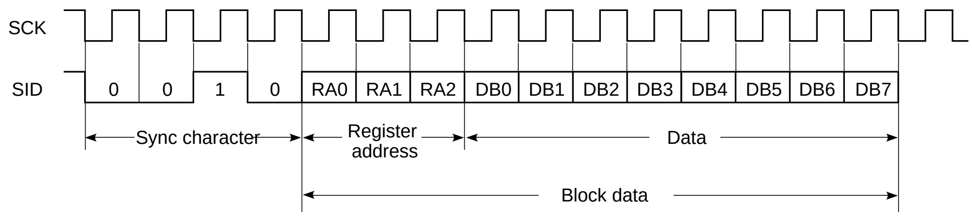
FUNCTIONAL DESCRIPTION

Serial Data Communication

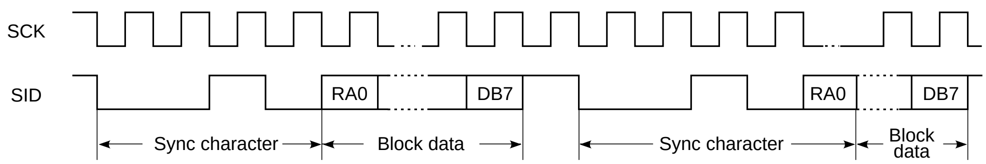
The SED1280 uses a synchronous serial data system, with all timing referenced to SCK. Data communication uses a 4-bit synchronization pattern.

Serial data reception

Data input on SID is clocked into the receiver buffer on the falling edge of SCK as shown in the following figure.



As the buffer state is undefined after power-ON, $\overline{RST}$ should be momentarily held LOW after power-ON to set all bits of the buffer to 1.
Data loaded into the buffer is compared with the synchronization pattern. If a match is detected, the next bit is treated as the start of the data block. The synchronization pattern should be repeated between consecutive blocks as shown in the following figure.

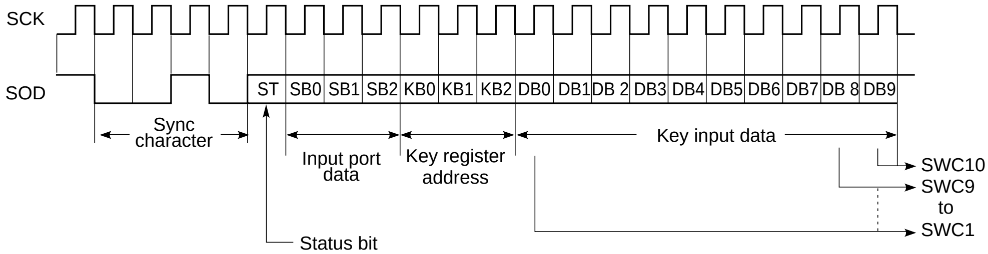


Data reception limits

The receiver incorporates two data buffers—buffer 1 and buffer 2. When continuously receiving data, buffer 1 fills first, then buffer 2. New data blocks are only received when both buffers are empty. New data is lost if it is sent while the controller is processing data in one or both buffers. The busy status bit, ST1, is set to 1 while the controller is processing data.
Note that new data cannot be recieved while data is being transmitted, and that two data blocks received consecutively are treated as a single block.

Serial data transmission

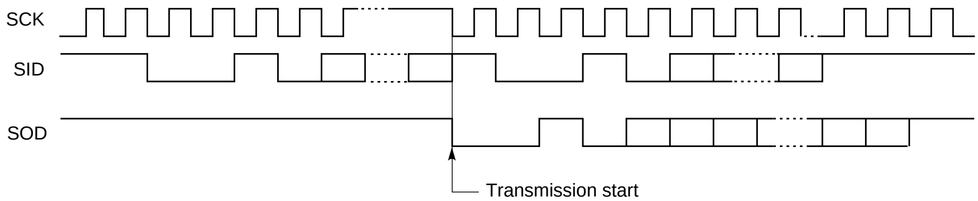
SWC1 to SWC10 and EI1 to EI3 are scanned and their input logic levels transmitted serially from SOD as shown in the following figure. Data is clocked out on the falling edge of SCK.



As the state of SOD is undefined after power-ON, $\overline{RST}$ should be momentarily held LOW after pow-ON to set SOD HIGH. SOD remains HIGH until the first command from the host is received and returns HIGH when data transmission is complete.

Data transmission and reception timing

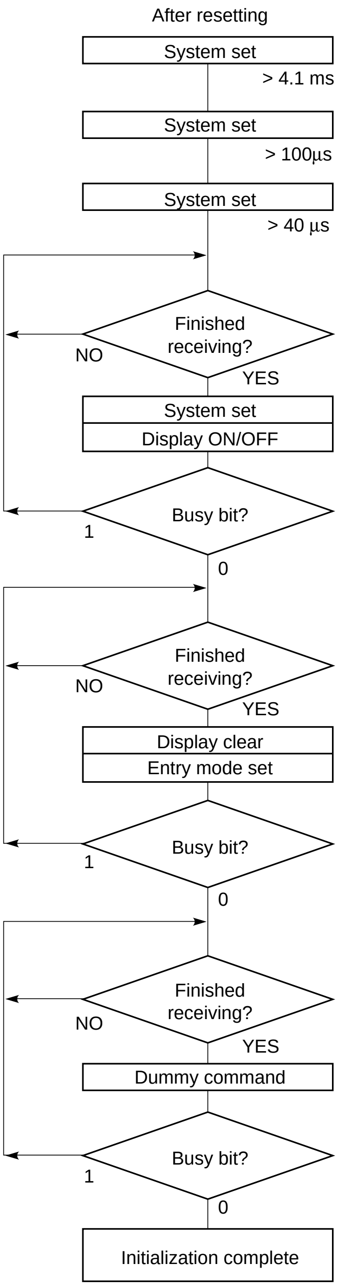
Data transmission starts from the first falling edge of SCK after a block of data has been received. If two blocks of data are received consecutively, data transmission starts from the first falling edge of SCK after the first block has been received, as shown in the following figure.



Status bit

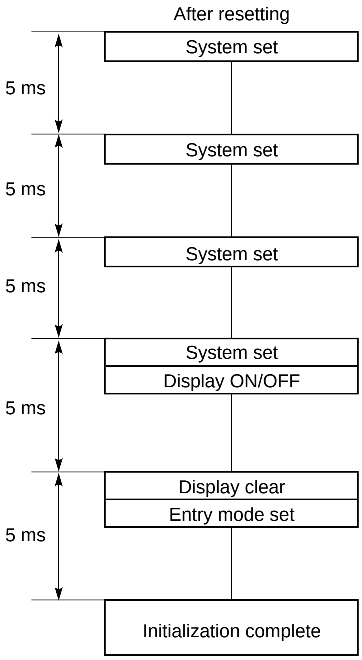
The ST1 status bit indicates that the controller is processing received data and cannot receive new data. When ST1 is HIGH, data is being processed and the host should not transmit new data until ST1 is LOW.
The host shoulld begin checking ST1, as shown in the following figure, as soon as it transmits new data.

SED1280



Register address	DB7			to				DB0
0	0	0	1	1	X	X	X	X
0	0	0	1	1	X	X	X	X
0	0	0	1	1	X	X	X	X
0	0	0	1	1	N	F	X	X
0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	1/D	S
2	X	X	X	X	X	X	X	X

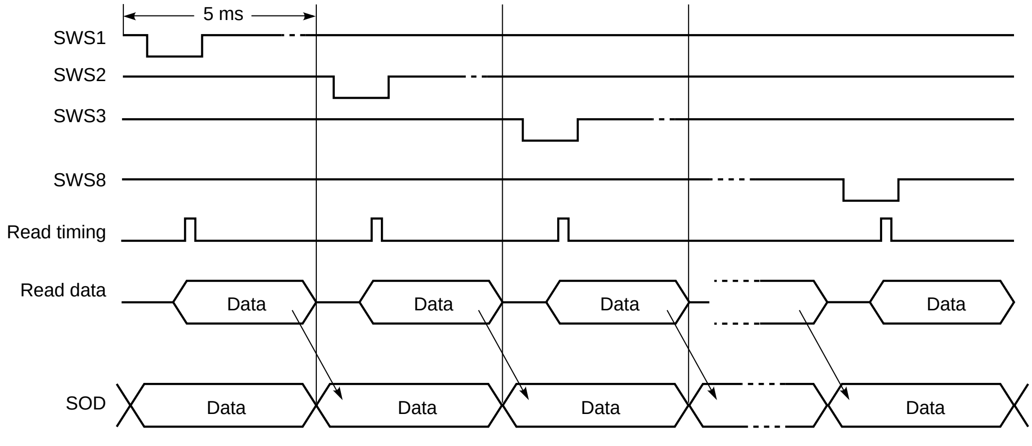
If the host does not check ST1, it should determine when to send new data by calculating the processing time of each data block as shown in the following figure.



Register address	DB7			to				DB0
0	0	0	1	1	X	X	X	X
0	0	0	1	1	X	X	X	X
0	0	0	1	1	X	X	X	X
0	0	0	1	1	N	F	X	X
0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	1/D	S

Key switch and input data

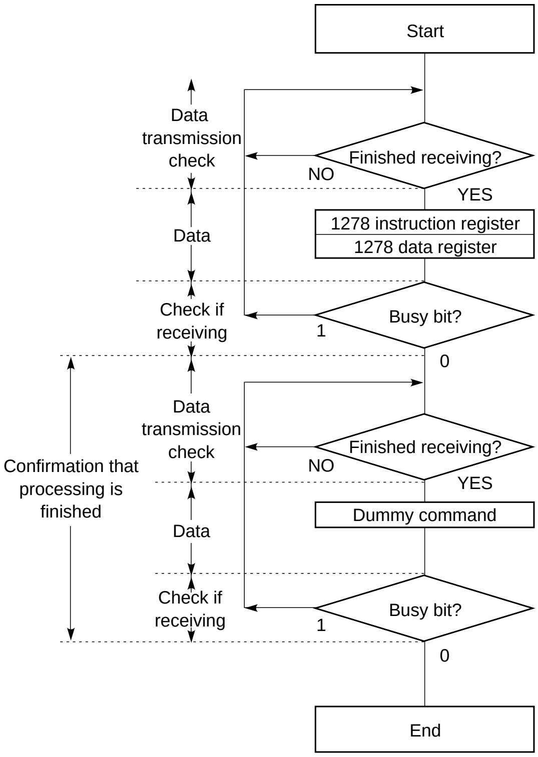
The SED1280 scans the key inputs and expanded input ports once every 5 ms. The scanned data is then output on SOD as shown in the following figure. The status bit is updated each time data is transmitted.



Data transmission flow charts

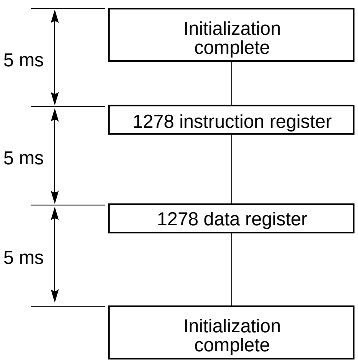
The following figures show the 1278 core display data RAM processing when data is transferred from the host to the SED1280.

Transmission using the busy bit



Register address	DB7			to				DB0
0	1	Address data						
1	DDRAM write data							
2	X	X	X	X	X	X	X	X

Timed access transmission



Register address	DB7			to				DB0
0	1	Address data						
1	DDRAM write data							

System Registers

The system registers access the data display RAM, character generator RAM and LED display RAM. These write-only registers are addressed using RA0 to RA2 as shown in the following table.

Address			Name	Function
RA2	RA1	RA0		
0	0	0	1278 instruction register	Sets the 1278 core command and RAM address.
0	0	1	1278 data register	Writes to the 1278 character generator RAM and display data RAM.
0	1	0	Not used	
1	1	0	Not used	
1	0	0	LED address register	Sets the LED display register address.
1	0	1	LED data register	Writes to the LED display address.
1	1	0	Expanded output port register	Controls the expanded output ports.
1	1	1	Test mode register	Used for factory inspection prior to delivery.

LED address and data registers

These five, 8-bit registers control an external 5 × 8-LED display. When a display data bit is set, the corresponding LED is ON. The following table shows the relationships between the registers, the LED output drivers and the output ports associated with each LED.

LED address register			LED data register								Row output pin
DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0									LE1
0	0	1									LE2
0	1	0									LE3
0	1	1									LE4
1	0	0									LE5
Column output pin			SWS8	SWS7	SWS6	SWS5	SWS4	SWS3	SWS2	SWS1	

Note: LED address register bits DB3 to DB7 are ignored.

For example, the following table shows the address and data sequence to turn ON the two LEDs connected between LE3 and SW3, and LE3 and SW7.

Step	Address			Data							
	RA2	RA1	RA0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	0	0	×	×	×	×	×	0	1	0
2	1	0	1	0	1	0	0	0	1	0	0

Note: × = don't care

When LED data is written continuously, the LED address register increments automatically.

Expanded output port register

This 2-bit register contains the data output on the EO1 and EO2 expanded output ports as shown in the following table.

Expanded output port data register							
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
×	×	×	×	×	×	EO2	EO1

Note: × = don't care

For example, the following table shows the address and data to set EO1 to LOW and EO2 to HIGH.

Address			Data							
RA2	RA1	RA0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	0	×	×	×	×	×	×	1	0

Note: × = don't care

Test mode register

This register is used to factory test the SED1280 prior to delivery. It is initialized by momentarily holding $\overline{RST}$ LOW.

1278 instruction register

The following table shows the 1278 instructions.

Instruction	Code								Cycles	Description
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	1	1640	Clears the entire display and resets the display data RAM address counter.
Cursor Home	0	0	0	0	0	0	1	×	1640	Resets the display data RAM address counter and returns a shifted display to its original position. The RAM contents are not changed.
Set Entry Mode	0	0	0	0	0	1	I/D	S	40	Enables the display shift and sets the display shift direction.
Display Attributes	0	0	0	0	1	D	C	B	40	Bit D enables/disables the entire screen, bit C enables/disables the cursor and bit B enables/ disables character blinking at the cursor position.
Cursor/display Shift	0	0	0	1	S/C	R/L	×	×	40	Shifts the display when a cursor move that does not alter the display data RAM occurs.
System Setup	0	0	1	IF	N	F	×	×	40	Bit iF sets the interface data length, bit N the number of display rows, and bit F, the font.
Select CGRAM	0	1	Character generator RAM address						40	Sets. the CGRAM address. Successive write instructions will address CGRAM.
Select DDRAM	1	Display data RAM address							40	Sets the DDRAM address. Successive write instructions will address DDRAM.

Note: × = don't care

The control bit functions are shown in the following table.

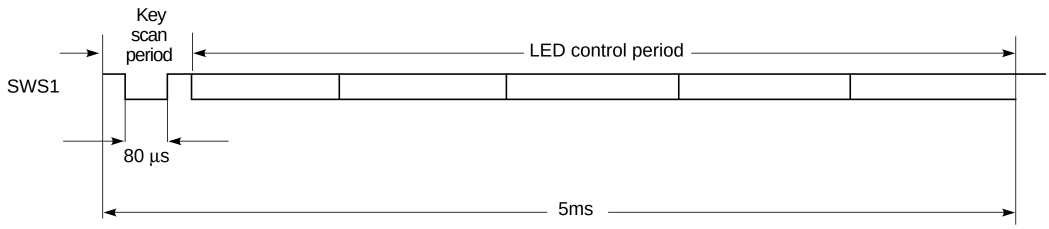
Control bit	Function	
	0	1
I/D	Decrement	Increment
S	No display shift	Disply shift
S/C	Cursor movement	Display shift
R/L	Left shift	Right shift
IF	4-bit interface	8-bit interface
N	One row	Two rows
F	5 × 7 pixels	5 × 10 pixels

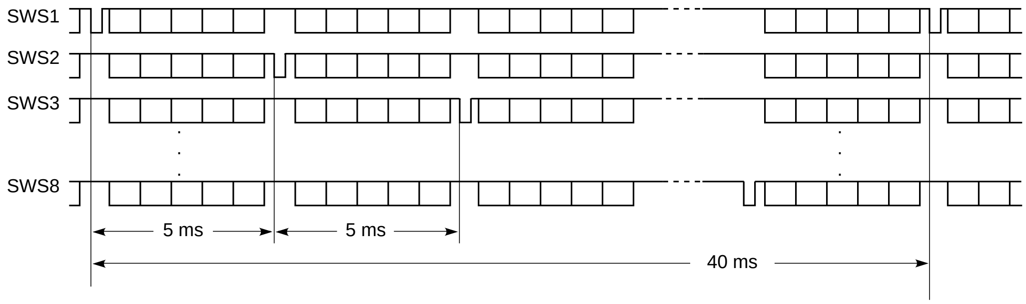
1278 data register

This register is used for writing data to the 1278 display data (DD) RAM and character generator (CG) RAM. Data is written to DDRAM when a Select DDRAM instruction is executed before a Select CGRAM instruction, and written to CGRAM when a Select CGRAM instruction is executed.

Key Scanning

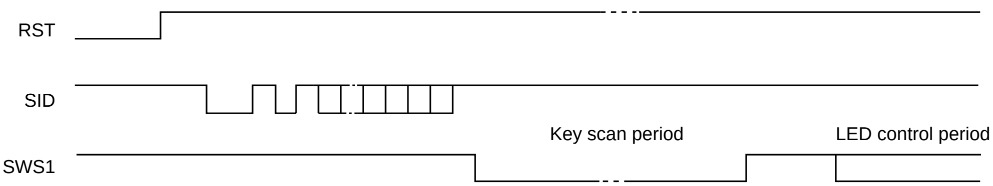
An 8 × 10-key matrix can be scanned using SWS1 to SWS8 scan outputs and SWC1 to SWC10 scan inputs. The SWS1 timing during one scan interval and SWS1 to SWS8 timing during several scans are shown in the following figures.





Key scan initialization

A key scan starts automatically once the first block of data is received from the host, after a reset. The 5 ms scan cycle runs continuously, once started, as shown in the following figure.



Expanded Input Ports

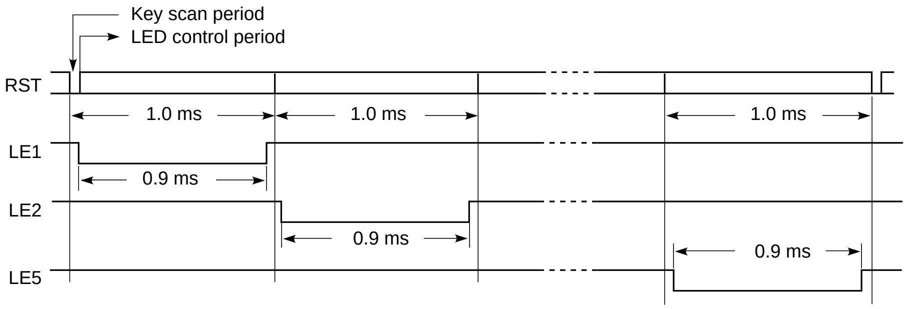
Scanning of the EO1 to EO3 expanded input ports starts automatically once the first block of data is received from the host, after a reset.

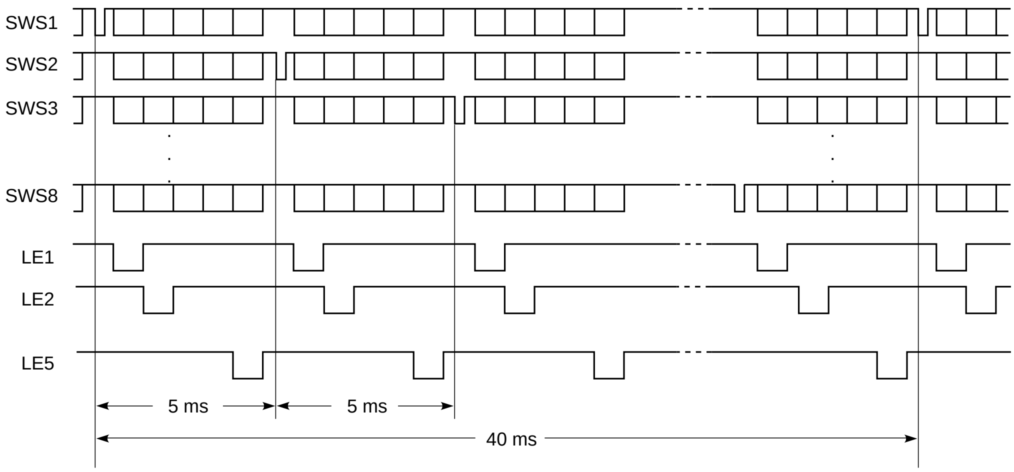
LED Controller

Up to 40 LEDs can be connected to SWS1 to SWS8 and LE1 to LE5 to form an 8 × 5 matrix.
To control the LEDs, LE1 to LE5 are connected to the based of external pnp transistors, and SWS1 to SWS8, to the LED anodes.

LED controller timing

The LED controller timing for one scan and a series of scans is shown in the following figures.





LED controller limits

Up to 25 mA can be drawn from any one of SWS1 to SWS8 with a maximum total of 100 mA for all eight pins. As the SED1280 does not current limit its outputs, the host should limit the number of LEDs that are ON simultaneously. For example, if a LED draws 5 mA, a maximum of 20 LEDs can be ON simultaneously.

DESIGN INFORMATION

Although the SED1280 contains an SED1278 core, there are some important differences. The following points should be noted when designing a system using an SED1280.

System Clock

The 1 MHz SED1280 system clock is divided by four to generate the 250 kHz clock used by the SED1278 core. Accordingly, the SED1278 requires four times as many clock cycles as the SED1280 to execute the same instruction. The system clock must be connected, even if data transfer or key scanning is not used.

Data Interface

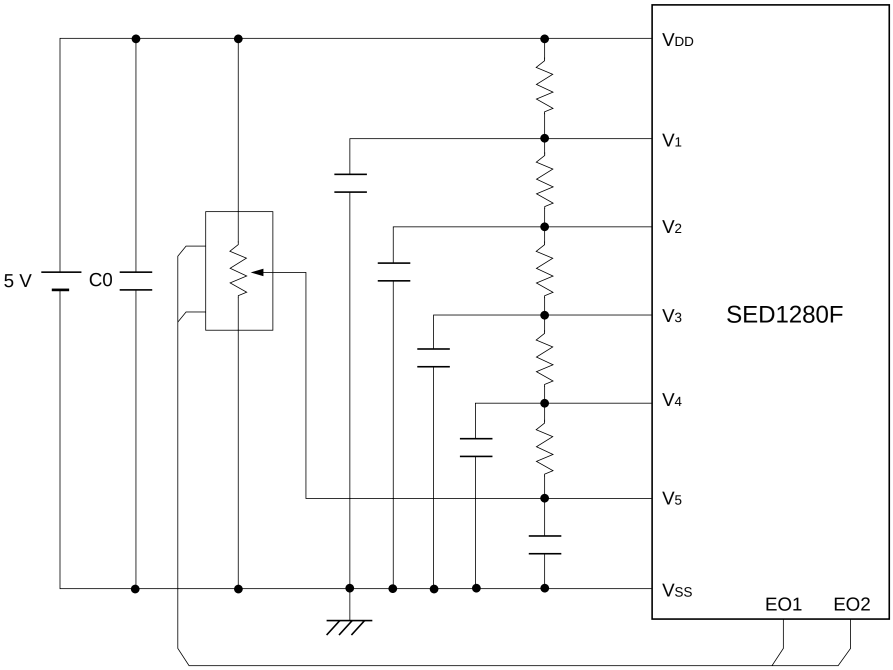
The SED1280 core data interface is eight bits wide. The SED1278 interface width is set to eight by setting the IF bit in the System Set instruction to 1.

Data Output

The SED1280 does not support the SED1278 function allowing the host to read the DDRAM and CGRAM address counter. The SED1280 does, however, provide the ST1 busy bit output, which can be read by the host.

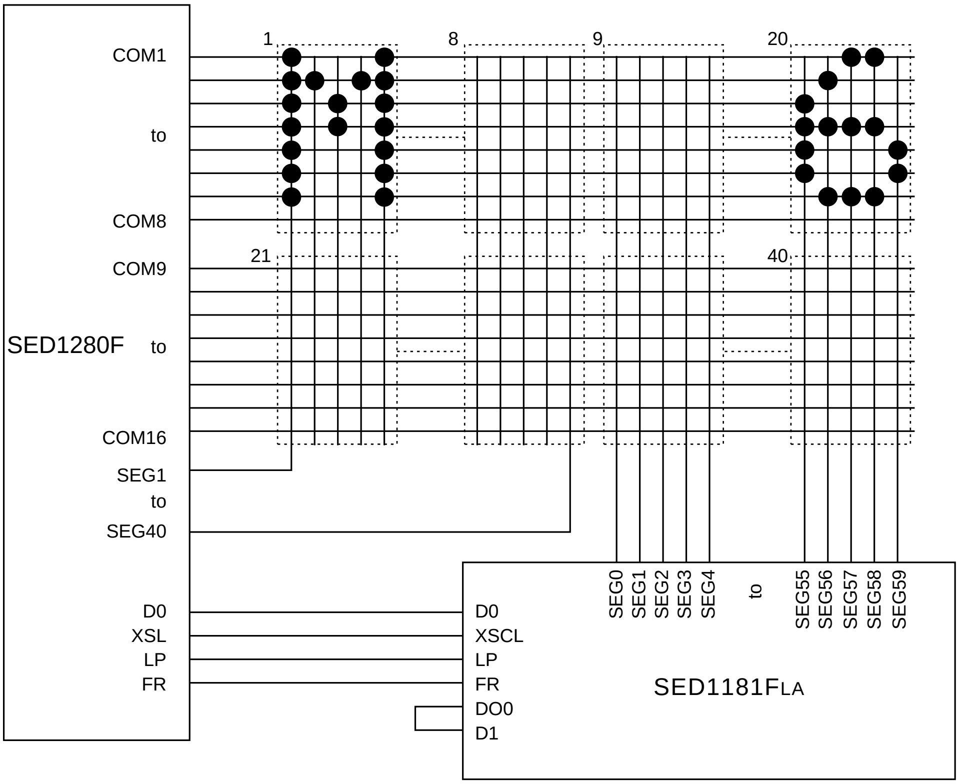
APPLICATION CIRCUITS

LCD Controller Resistor Divider



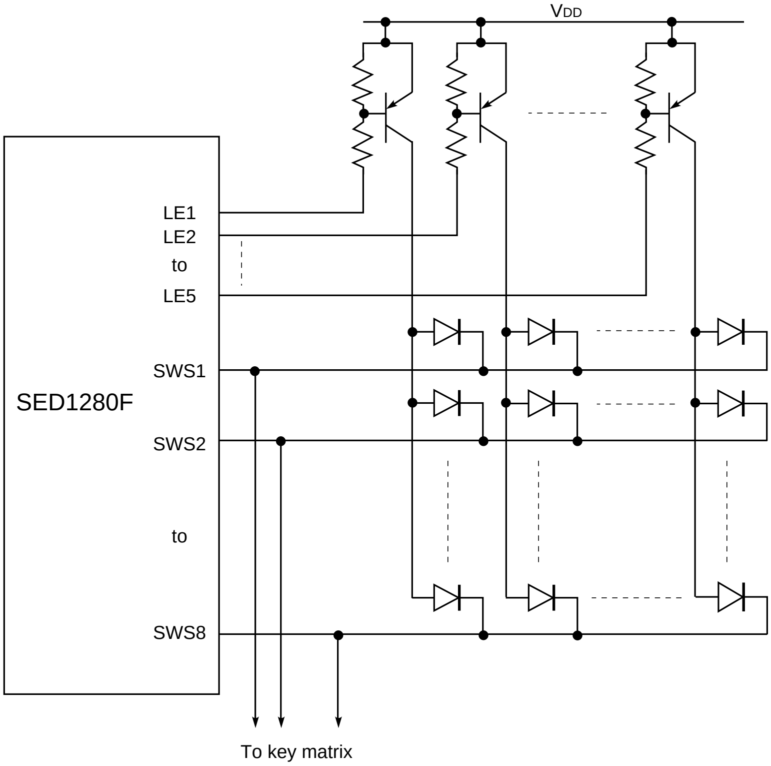
Note: C0 is connected between VDD and VSS to prevent noise, and should be 0.1 µF or greater.

LCD Connections (2 × 20 character, 5 × 7 dots/character)

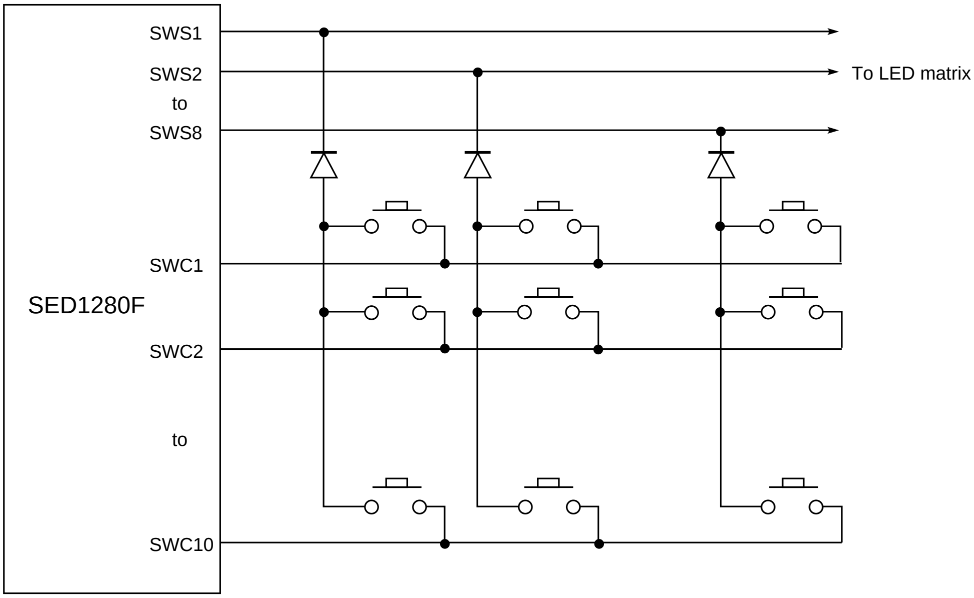


Note: SEG60 to SEG63 and DO1 are open.

LED Matrix Connections



Key Switch Matrix Connections



Note: Do not press two or more keys simultaneously.

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